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Split gate tunnel barriers in double top gated silicon metal-oxide-semiconductor nanostructures

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SPLIT GATE TUNNEL BARRIERS IN DOUBLE TOP GATED SILICON METAL-OXIDE-SEMICONDUCTOR NANOSTRUCTURES

by

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B.S., ELECTRICAL ENGINEERING, UNIVERSITY OF NEW MEXICO, 2009

THESIS

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ABSTRACT

Quantum computers hold the promise of far exceeding the computational efficiency of classical computers in a variety of applications. An immense amount of interest has grown in spin-based silicon quantum computers where an electron spin represents a quantum bit (qubit). Spin qubits in silicon are attractive because of their long coherence times due to the weak spin-orbit coupling of silicon and the ability to eliminate background nuclear spins by isotopic enrichment.

One way spin qubits can be realized in silicon is by using donor-bound electron spins. Individual donor atoms intentionally implanted into tunnel barriers of silicon have been examined using transport measurements. However, reliable interpretation of donor transport measurements depends critically on understanding the tunnel barriers separating the localized electron state from the source and drain reservoirs.

In this thesis, split gate tunnel barriers defined in a double top-gated, enhancement-mode silicon metal-oxide-semiconductor (MOS) device structure are

analyzed. Tunnel barriers implanted with a small number of antimony donor atoms and non-implanted tunnel barriers were both characterized electrically at liquid helium temperatures ($T \approx 4$ K). A tunnel barrier model is presented that uses the measured values of conductance to calculate the tunnel barrier height and width for a range of bias and gate voltages. The model provides a method to quantitatively describe how the barrier changes with bias and gate voltage and a way to compare different tunnel barriers for different devices. The model also provides insight about the binding energies of electrons in the potential well within the tunnel barrier. Thus the model can provide guidance to distinguish between high probability candidates for transport through intentionally implanted donors in contrast with transport through charge defects.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1: INTRODUCTION

Classical computers use binary digits or bits to process and store information. A binary digit or bit has two possible values or states that is either 0 or 1. The bit is physically represented by two voltage ranges; a low voltage range close to 0 V represents one state and a high voltage range close to the power supply voltage represents the other. Digital circuits use transistors to switch between binary digits 0 and 1. The transistor predominately found in the integrated circuits of today's computers is the metal-oxide-semiconductor field-effect transistor (MOSFET).

The minimum feature size on an integrated circuit has continuously decreased, from 8 μm in 1969 to a 22 nm node today with smaller nodes planned. Gordon Moore, one of the founders of Intel Corporation, is credited with correctly predicting in 1965 that the transistor size would shrink by 30% every 1-2 year [1]. The reduction in transistor size has led to highly dense chips with hundreds of millions of transistors and increased switching speeds. Consequently, the continuous reduction in transistor size has led to more powerful and faster computers capable of performing complex computations.

Continued scaling of the transistor at the same rate is increasingly difficult and will reach a likely hard stop as the size approaches atomic distances, and despite the capabilities of modern computers, many computational problems will remain intractable. There are many examples in application areas such as optimization, quantum chemistry, searching, and factoring for which classical computers would take an impractically long time to solve presently relevant problems.

In 1982 Richard Feynman suggested that a computer based on the principles of quantum mechanics could efficiently simulate quantum systems whereas a classical

computer would have essential difficulties [2]. This was one of the sparks that inspired many people to consider quantum computer based ideas, however, at the time it was unclear how to implement such an idea. In the 1990s two theoretical breakthroughs, quantum error correction [3,4] and Shor's algorithm for prime factorization [5], introduced a plausible path forward. The theory of quantum error correction proposed a way to detect and correct errors in two level systems, quantum bits (qubits) that were used for the quantum computation. Shor's algorithm showed a way that quantum bits could be combined and manipulated to achieve exponential speed-up compared to the best classical approach to factoring prime numbers. Quantum algorithms that promise speed-up for other problems have subsequently been discovered, for example, for data base search [6], quantum simulation [7], and quantum chemistry [8].

1.1 QUANTUM COMPUTATION

The fundamental concept of quantum computation is the quantum bit or qubit. Similar to a classical bit, a qubit has a state. Two possible states for a qubit are the states $|0\rangle$ and $|1\rangle$, which represent the classical bits 0 and 1. However, the key difference between a bit and a qubit is that a qubit can exist in a state that is a linear combination or superposition of the states $|0\rangle$ and $|1\rangle$ [9],

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle . \tag{1.1}$$

Here α and β are complex quantities with a magnitude and a phase. Interestingly, when a qubit is measured its quantum nature collapses and it reverts back to its classical nature. That is, when a qubit is measured, the result is either $|0\rangle$, with a probability of $|\alpha|^2$, or the result is $|1\rangle$, with a probability of $|\beta|^2$. It is natural that $|\alpha|^2 + |\beta|^2 = 1$ because

there are only two possibilities. The important point is that, prior to measurement, the qubit exists in both states $|0\rangle$ and $|1\rangle$.

The qubit is represented by a quantum two-level system. Some examples include the ground and excited states of an atom, the vertical and horizontal polarization of a single photon, and the two spin states of a spin ½ particle. The actual realization of a physical quantum computer is exceptionally demanding. The requirements include a system that is scalable, has well-defined qubits, and is well isolated from its environment. A system that is well isolated from the environment is needed to ensure long coherence times. At the same time, one must have access to the qubits for initialization, manipulation, and measurement [10]. The difficulty is in finding the perfect balance between all these requirements. It is believed that semiconductor devices, which have made modern digital computers so successful today, will also help in the realization of a quantum computer.

Two of the most prominent candidates for qubits in a quantum computer are electron spins in semiconductor quantum dots [11] and donor electron or nuclear spins in semiconductors [12,13]. Spin-based qubits in semiconductors are attractive because of their potential for long coherence times. Electron spins in gallium arsenide (GaAs) quantum dots were found to have a spin coherence time on the order of microseconds [14]. In contrast, spin qubits in silicon have coherence times that are orders of magnitude longer than in III-V semiconductors [15,16]. Silicon has a weak spin-orbit interaction and background nuclear spins can be removed because there are zero nuclear spin isotopes with which the silicon can be enriched, while none of the constituent elements of III-V semiconductors possess zero nuclear spin. Thus silicon has become an attractive platform

for spin-based solid-state quantum computers. The work in this thesis is primarily concerned with silicon device structures intended for antimony (Sb) donors to act as the potential well for a single electron spin. In the next section some previous investigations of single donor atoms in silicon are discussed.

1.2 SINGLE DONOR ATOMS IN SILICON

Dopant atoms have a well-established purpose in semiconductor device technology as sources of extrinsic free carriers for foundational devices such as diodes and transistors. Although dopants are well understood in bulk semiconductors, the details of the electronic structure and spin coherence of single donors close to an oxide-semiconductor interface in gated nanostructures has been a topic of recent research. The charge and spin states of electrons bound to single donors have been examined with transport spectroscopy. Single spin read-out of a donor [17] and coherent manipulation of the spin state have also been demonstrated recently, but this topic extends beyond the scope of this thesis.

Early transport measurements, where the charge states of a real atom with an attracting Coulomb potential were examined, used silicon nanowires (i.e. FinFETs) [18]. The device consisted of a p-type silicon nanowire connected to large source and drain electrodes. The source and drain are n-type and were implanted with arsenic. This first nanowire is used as the channel. An n-type silicon nanowire is deposited perpendicularly to the first wire and wraps around three of its sides. It is separated from the first wire by a thin oxide and acts as the gate. It is believed that arsenic donor atoms have diffused to the p-type silicon channel from the source and drain contacts. Under certain biasing conditions, the current is not carried by the entire body of the FinFET but only by its

corners. It is in these small corner regions, below the threshold of the FinFET corner channel, where resonant tunneling through single arsenic donors is believed to occur. The first and second electron states of the donor, which are called the D^0 and D^- states respectively, were identified based on resonant tunneling magneto-spectroscopy of ground and excited states that agree well with numeric predictions.

These same FinFETs were also used to study the effects of gate-induced quantum confinement transitions [19]. The main idea is that at low electric fields, the electron is localized at the donor site. However, as the electric field increases, the electron becomes delocalized between the donor's potential well and the triangular potential well induced at the oxide-semiconductor interface. This is known as hybridization. At sufficiently high electric fields, the electron is pulled completely into the triangular well. This process could allow control over the wave functions of the dopants, which is a key element in silicon quantum electronics.

Despite these groundbreaking successes, the problem with these FinFETs was the lack of control over the electron densities in the source and drain reservoirs, the number of donors in the active region, and the depth of the donors from the oxide-semiconductor interface. The only controllable device parameter was the tunnel coupling between the donor and the reservoirs, which was controlled by the FET channel length. These problems were addressed in the work done by Tan et al. [20].

In this work, a thin layer of silicon dioxide was thermally grown on top of a silicon substrate and then a layer of polymethylmethacrylate (PMMA) was deposited over the oxide and patterned into 100 nm × 200 nm apertures using electron-beam lithography (EBL). These apertures defined the implantation window where phosphorus

donors were implanted via ion implantation. The number of donors in the active region and the donor depth can be controlled by properly choosing the implantation energy and dose of the phosphorus ions. An aluminum gate is formed directly over the implanted donors and can control the donor energy levels, while an overlaying top gate can control the electron density in the source and drain reservoirs. Moreover, three independent devices can be fabricated in each sample, which increases the device yield, and masking some of devices during the implantation process can create control devices, which contain no phosphorus donors.

The device structure by Tan et al. has been used extensively to study single donors, including single spin read-out and coherent manipulation of single spins. The next step in evolution of donors for qubits is to establish a way to controllably couple and uncouple two donor-bound electron spins. A frequently cited device structure from Kane [12] is to place a gate in between the two donors, which can control the electron wavefunction overlap. The electron wavefunction is tightly bound around the donor, therefore calculations of the necessary spacing of the two donors indicate that they must be relatively close, on the order of 20-30 nm, to introduce appreciable overlap [21]. The Tan et al. process flow would introduce the need to locate an aluminum gate between two donor implant locations spaced on the order of 20-30 nm, which introduces extreme lithography alignment requirements.

An alternative approach is to form the gate first and then implant. Standard CMOS processing uses degenerately doped poly-silicon gates for self-aligned implanted structures. Nordberg et al. [22] showed that split gate tunnel barriers and quantum dots could be formed using poly-silicon gates. Bishop et al. [23] extended this work by

examining donors implanted into poly-silicon gated point contact tunnel barriers, which were self-aligned. Furthermore, antimony was used as the donor because it has lower diffusivity [24,25]. Resonant tunneling was observed in an implanted sample and extensive measurements of the capacitances of all the gates to the resonances were used to triangulate the position of the resonances assuming that they were donor sized charge centers (i.e. a metallic sphere with a Bohr radius of a donor). Although this method was effective in locating the resonances, it is computationally intensive and also does not directly provide insight about the tunnel barrier or how to optimize the tunnel barrier.

1.3 THESIS OBJECTIVES

The primary contribution of this thesis research is to extend and test the accuracy of a tunneling model used by MacLean et al. [26] for non-implanted and implanted MOS split gate tunnel barriers. In particular, this model assumes rectangular barriers and a capacitance model to determine the barrier height dependence on voltage. This model is applied to different geometries with and without implanted donors to (a) examine the agreement of the model with experiment and (b) use the model as a way to characterize different tunnel barrier heights and widths.

In Chapter 2 we discuss the fabrication process of split gate point contacts implanted with antimony donor atoms in a double gate enhancement-mode silicon MOS device structure. Non-idealities that occur in the MOS system are discussed. In addition a conceptual model of the split gate tunnel barrier is introduced that is consistent with the nanostructure and that is useful in explaining the resonant tunneling features observed in the measurements.

In Chapter 3 we discuss the necessary conditions for observing the single electron charging effects. Then the four Kelvin (4K) experimental setup is described. We also present initial device measurements.

Chapter 4 begins with a brief discussion on transport spectroscopy, i.e., measurements of the differential conductance as a function of dc source-drain bias and gate voltage. The plots obtained from these measurements are referred to as stability plots. Next the transport measurements of the right constriction are presented and discussed. The right constriction is the non-implanted split gate tunnel barrier and is known as the control case. Then we present the tunneling model that will be used to characterize the tunnel barriers in this study and apply it to the control constriction.

In Chapter 5 we discuss the transport measurements and tunnel barrier modeling of the two implanted point contacts in the device and compare the results to the control case. Finally we compare the results of the tunneling model to capacitance modeling.

CHAPTER 2: SINGLE ANTIMONY DONORS IN DOUBLE GATED SILICON MOS NANOSTRUCTURES

In this chapter, a fabrication process used for the devices measured in this thesis is described. The Quantum Information Science and technologies (QIST) group at Sandia National Laboratories (SNL) fabricated the devices and gave them to me for the measurements. Non-idealities that can occur in the fabrication of silicon MOS nanostructures, specifically process-induced damage, are discussed. This chapter concludes with a description of an energy diagram through a tunnel barrier point contact, which is a common nanostructure used for single donor spectroscopy.

2.1 FABRICATION PROCESS

The devices studied in these experiments are double top gated silicon MOS nanostructures. The devices are enhancement-mode devices, which means that the device is normally off and a gate voltage must be applied to turn the device on. The lower-level section of the device begins with a silicon substrate, followed by a silicon dioxide (SiO_2) gate dielectric, and a poly-silicon (poly) gate. The poly gate is patterned into thin fingers using electron-beam lithography. The poly-silicon gate patterns used in these devices imitate gate designs from successful quantum dot devices in GaAs/AlGaAs [14] and Si/SiGe heterostructures [27]. The poly gates can be used for both depletion and inversion, but in most cases, they are used for depletion and are referred to as depletion gates. The upper-level consists of an aluminum oxide (Al_20_3) and aluminum gate. The aluminum oxide isolates the lower poly gates from the top aluminum gate. The

aluminum gate covers the entire active region of the device and it is used to create an electron inversion layer at the Si/SiO_2 interface.

The fabrication process is separated into two phases. The first phase of fabrication is performed at the 0.35 μm silicon foundry at SNL, which is a 150 nm wafer scale silicon-only fabrication facility [28]. The benefits of processing the devices at the silicon foundry are tightly controlled processes and highly parallelized processing, however current lithographic size limitations require a portion of the processing to be done outside the silicon foundry [28]. Thus the second phase of fabrication is performed in a user-facility-like clean room equipped with electron beam lithography.

The first phase begins in the silicon foundry with a p-type silicon substrate with a dopant concentration, primarily boron, of 1×10^{15} cm^{-3}. Arsenic is implanted with a dose of 2×10^{15} cm^{-2} and energy 50 keV to create n^+ source and drain contacts. This is followed by thermal oxidation at 900°C for 150 minutes to create a 35 nm SiO_2 gate oxide. Next, 200 nm of poly-silicon is deposited and degenerately doped by implantation of arsenic. An additional 25 nm of silicon nitride is grown over the poly gate that will be used as an etch stop for oxide wet etches. An interlayer dielectric (ILD) film, about 250-500 nm of SiO_2, is deposited. Via holes through the ILD were created with a plasma-based dry etch, which allow metal to contact the poly-silicon gate and the ohmic contacts. Via holes were filled with tungsten using chemical vapor deposition. The tungsten also forms the bond pads in this process flow. Tungsten is used because it (a) provides a high contrast material for e-beam lithography and (b) it can withstand high temperature anneals allowing implanted dopants to be annealed and electrically tested without further metallization. Finally, a 100 μm × 100 μm window in the ILD is opened above a large

poly-silicon sheet using a wet etch. This will allow for further processing to form custom nanostructures with e-beam lithography. A cross-sectional schematic diagram of the device after the first phase of processing is shown in Figure 2.1.

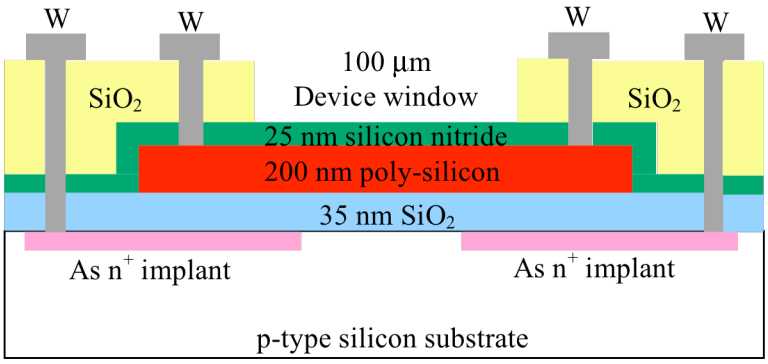


Figure 2.1 Cross-sectional diagram of the device after the first phase of processing (not to scale).

The second phase of fabrication begins with electron-beam lithography. A 100 keV electron beam is used to pattern negative e-beam resist. Once the resist is exposed and developed, a dry etch is used to etch away any exposed nitride so that the poly-silicon underneath is revealed. Next, the sample is cleaned to remove the remaining EBL resist. This creates a "hard mask" consisting of silicon nitride that is patterned from the EBL resist [28]. Then the exposed poly-silicon is etched away, removing most of the poly-silicon slab, and leaving only isolated poly-silicon nano-gates in the pattern of the initial EBL write.

Figure 2.2 shows a scanning electron micrograph (SEM) image of the device at this juncture of the fabrication process. It is a top-down view of the device showing the poly-silicon gates (white) on top of the SiO_2 gate oxide (gray). A standard nomenclature for the poly gates is shown where the acronyms mean: TP (Top Plunger), LQPC (Left Quantum Point Contact), L (Left), LP (Left Plunger), CP (Center Plunger), RP (Right

Plunger), and R (Right). Note that the left constriction (between LQPC and L) is about 100 nm greater than the constriction between TP and CP.

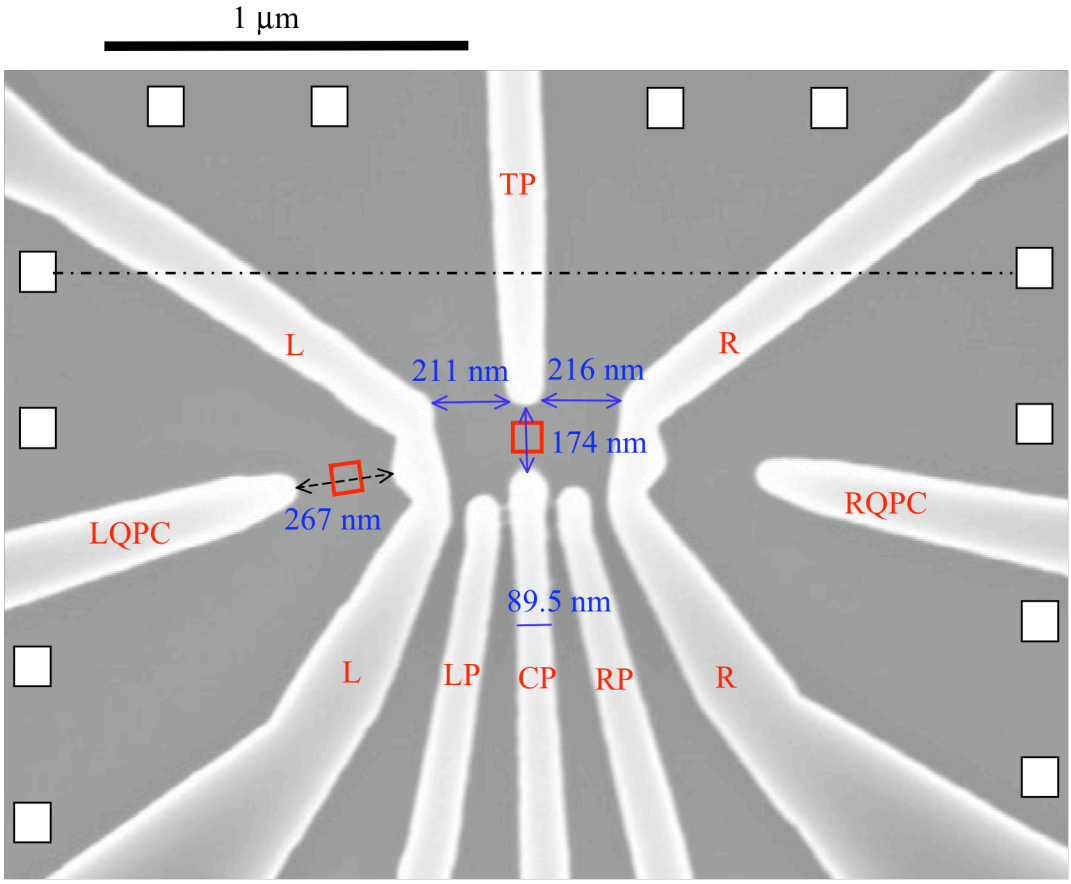


Figure 2.2 Scanning Electron Micrograph (SEM) image of the poly-silicon gate layout showing the poly gates (white) on top of the SiO_2 (gray) before secondary dielectric and top metal deposition. Also shown are the names of the poly gates used in this study. The white squares represent the position of the ohmic contacts and the red squares represent the 80 nm × 80 nm implantation window for the donors.

For these donor devices, an additional EBL step is required after the poly-Si etch. The entire device is first covered in 300 nm of PMMA and 80 nm × 80 nm openings are formed using EBL in two constrictions, the left constriction and the TP/CP constriction, while the right constriction (between RQPC and R) remains unexposed (Figure 2.2). Thus the right point contact is masked by the 300 nm PMMA during implantation and acts as a

control case where no donors are implanted. The implantation of donor ions into the Si substrate is self-aligned with the poly-silicon depletion gates forming the split gate point contacts. The devices are implanted with antimony donor atoms with an implantation energy of 120 keV and dose 2×10^{11} cm^{-2}. Simulations using SRIM (The Stopping Range of Ions in Matter) predict an average of five Sb donors in the 80×80 nm^2 window at a depth of 27 nm below the Si/SiO_2 interface when implanted at energy of 120 keV [29].

After implantation, the sample is first cleaned to remove the PMMA. The next steps include a tungsten etch, a nitride etch that removes the remaining nitride on top of the poly gates, and RCA clean. Next the sample is re-oxidized at 900°C for 24 minutes so that an additional 10-20 nm of silicon dioxide is thermally grown on the poly-Si gates. The reason for this re-oxidization is to activate the implanted dopants, to anneal any damage, to smooth surfaces for subsequent atomic layer deposition of Al_2O_3, and to ensure that small pieces of poly-silicon that may have been unetched are consumed and no longer provide a conducting path between gates [23,28].

It is important that the donors do not diffuse too far from the original implantation site during the re-oxidization process. Antimony is believed to diffuse by a purely vacancy-based mechanism [24,25] and the diffusion of antimony is retarded by oxidation due to injected silicon self-interstitials annihilating vacancies [25]. The intrinsic diffusivity of antimony in silicon is given by [25],

$$D_i = 0.214 e^{-\frac{3.65}{kT}} \ (\mathrm{cm}^2/\mathrm{s}). \tag{2.1}$$

Here $k = 8.62 \times 10^{-5}$ eV/K is Boltzmann's constant and T is the temperature. For a temperature of 1173 K, the intrinsic diffusivity is 4.5×10^{-17} cm^2/s. The characteristic diffusion length is simply [25,30],

$$L = 2\sqrt{Dt} \ . \tag{2.2}$$

Here D is the diffusivity and t is the time. Using the intrinsic diffusivity just calculated and t = 24 min = 1440 s gives a diffusion length of 5 nm, which is small relative to both the implant depth and lateral implant window size.

After re-oxidization, the next step is to deposit the secondary oxide. Aluminum oxide (Al_20_3) is deposited using atomic layer deposition (ALD) and it conformally coats the entire sample. The thickness of the aluminum oxide layer is 60 nm. This is followed by a 450°C forming gas anneal for 30 min.

The final steps include depositing and patterning 100 nm of aluminum that acts as the top metal gate, patterning and metallization of the aluminum contacts, and a final 30 min 400°C forming-gas anneal. The acronym *AG* will be used to signify the aluminum top gate throughout the text. Cross-sectional diagrams of the device after all steps in the fabrication process are completed are shown in Figure 2.3.

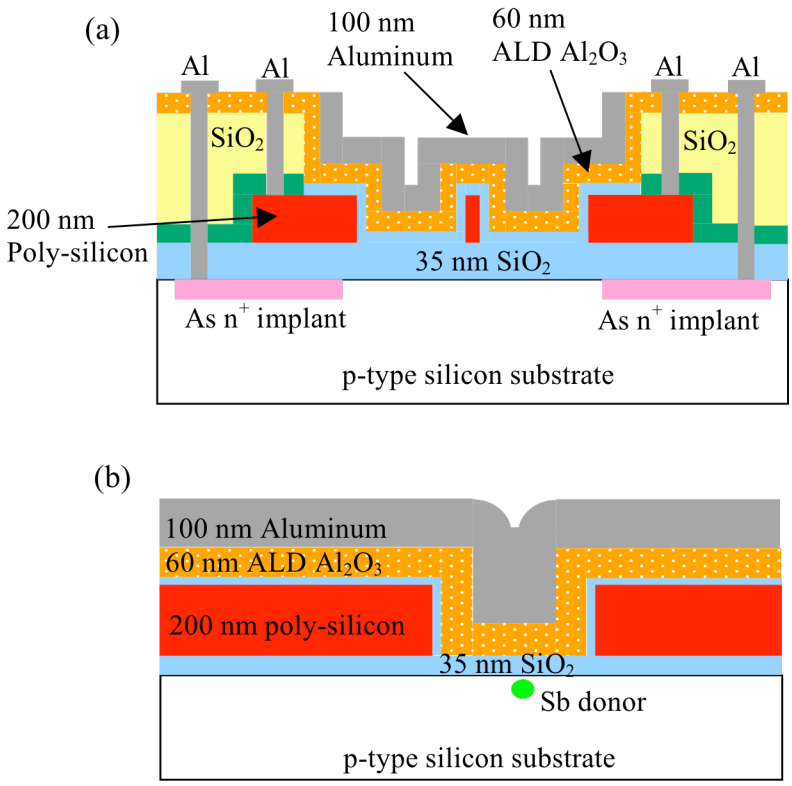


Figure 2.3 Cross-sectional diagrams of the device after the second phase of processing (not to scale). (a) Along the black dash-dot line in Figure 2.2. (b) Along the black, dash, double-arrow line in Figure 2.2.

2.2 NON-IDEAL MOS SYSTEM

A critical challenge in fabricating these devices is to avoid disorder in the MOS system. Disorder can cause scattering and parasitic dot formation in transport, which makes it difficult to probe only the transport resulting from the implanted donor atoms [22]. One potentially significant source of disorder is charge defects in the dielectric layers and at the Si/SiO_2 interface. These charge defects include fixed oxide charge and interface trapped charge. The presence of these charges is inevitable in practical systems; however, certain fabrication steps, including EBL, the poly-silicon etch, and implantation can cause further damage to the critical Si/SiO_2 interface or add more charge to system.

Thus great efforts are made (and are still being made today) to minimize damage and repair damage that has already occurred.

The fabrication steps of the previous section were characterized in references [22,23] by measuring changes in either the low temperature mobility or the charge defect density. High frequency and quasi-static capacitance-voltage (CV) measurements were used to determine the fixed oxide charge density and the interface trap density for key fabrication steps.

Significant damage can occur to the active region during both EBL and the poly-silicon etch that can severely lower the mobility. It was found that forming-gas anneals were crucial in repairing damage, recovering a large fraction of the mobility, and reducing the interface trap density. Summaries of the mobility measurements and the CV measurements that describe the effects of process damage, including EBL and the poly-silicon etch, are shown in Table 2.1 and Table 2.2 respectively.

Table 2.1 Summary of mobility measurements from reference 22.

Condition	T_{SiO2} (nm)	T_{Al2O3} (nm)	μ_{peak} (cm^2/Vs)	Start μ_{peak} (cm^2/Vs)	n_{peak} (cm^{-2})	$\mu(n=5\times10^{11}\ cm^{-2})$ (cm^2/Vs)	Density method	Oxidation condition
Phase I only	35	0	8000–16 000 (wafer dependent)	8000–16 000	$\sim10^{12}$	5500–10000	$C_{ox\text{-}nominal}$	Various
Phase I/EBL	10	0	2000	10 000	3.5×10^{12}	650	$C_{ox\text{-}nominal}$	10 nm Ox. w/DCE[a]
Phase I/EBL/ forming gas	10	0	6600	10 000	2.4×10^{12}	3500	$C_{ox\text{-}nominal}$	10 nm Ox. w/DCE
Phase I/ polysilicon etch/Al[b]	35	0	150	13 800	$>4\times10^{12}$	30	$C_{ox\text{-}nominal}$	35 nm Ox. w/DCE
Phase I/polysilicon etch/ Al/forming gas	35	0	5250	13 800	1.8×10^{12}	750	Hall	35 nm Ox. w/DCE
Phase I/polysilicon etch/ ALD/Al	35	60	300	13 800	$>4\times10^{12}$	50	$C_{ox\text{-}nominal}$	35 nm Ox. w/DCE
Phase I/polysilicon etch/ ALD/Al/forming gas	35	60	8300	13 800	1×10^{12}	6800	Hall	35 nm Ox. w/DCE
Phase I/ebeam Al	35	0	4950	14 250	2×10^{12}	2500	$C_{ox\text{-}nominal}$	35 nm Ox. w/DCE
Phase I/ebeam Al/ forming gas	35	0	8700	14 250	1.2×10^{12}	5700	$C_{ox\text{-}nominal}$	35 nm Ox. w/DCE
Phase I/thermal Al	35	0	8000	8000				

[a]DCE—(Dichloroethane).
[b]Unless noted, aluminum deposited via electron-beam evaporation.

Table 2.2 Summary of CV measurements from reference 22.

Condition	$T_{SiO2\text{-}nominal}$ (nm)	T_{Al2O3} (nm)	$T_{SiO2\text{-}meas}$ (nm)	$D_{it\text{-}lo}$ (cm^2/Vs) $\pm1\times10^{10}$	$D_{it\text{-}av}$ (cm^2/Vs)	V_{fb} (V)	Q_{fb} (cm^{-2}) $\pm3.2\times10^{10}$
SiO_2 [a]/Al	35	0	35.3	2.39×10^{10}	3.51×10^{10}	−0.79	6.58×10^{10}
SiO_2/15 nm Al_2O_3/Al	35	15	35	2.88×10^{10}	2.71×10^{10}	−0.45	-1.17×10^{11}
SiO_2/30 nm Al_2O_3/Al	35	30	35	3.68×10^{10}	4.19×10^{10}	−0.76	3.5×10^{10}
SiO_2/polysilicon etch/Al	35	0	8.4	[c]	[c]	[c]	[c]
SiO_2/Al/no FG anneal (Ref. 41)	N/A	0	N/A	$3-6\times10^{12}$	N/A	N/A	N/A
SiO_2 [b]/Al	10	0	10			−0.72	8.73×10^{10}
SiO_2/Al	70	0	70	1.74×10^{10}	2.55×10^{10}	−0.86	5.38×10^{10}
SiO_2/polysilicon etch/Al	70	0	44.7	3.43×10^{10}	3.4×10^{10}	−0.13	-2.69×10^{11}
SiO_2/thermal Al	35	0	35	3.32×10^{10}	2.98×10^{10}	−1.25	2.71×10^{11}

[a]Oxides grown in oxygen ambient at 1 atm with a temperature of 1000 °C.
[b]10 nm oxide grown in 10% oxygen partial pressure diluted with Ar at 1000 °C.
[c]Measurements unattainable due to oxide leakage current. See Appendix B for details.

Ion implantation of the antimony donors also damages the critical Si/SiO_2 interface. It was found that re-oxidization at 900°C for 24 minutes helps to repair ion implant damage and decrease both the interface trap density and fixed oxide charge density compared to rapid thermal anneals [23]. A summary of the CV measurements that describe the effects of process damage due to implantation is shown in Table 2.3.

Table 2.3 Summary of CV measurements from reference 23.

Sample type	Q_{fb} (q/cm^2)	D_{it} (q/cm^2eV)
Normal process	$+5 \times 10^{10}$	1×10^{10}
Silicon implant + 30 sec @ 800 C (Donor device equivalent dose)	$+3 \times 10^{11}$	2×10^{11}
Silicon implant + 24 min @ 900 C	$+1 \times 10^{11}$	1×10^{10}

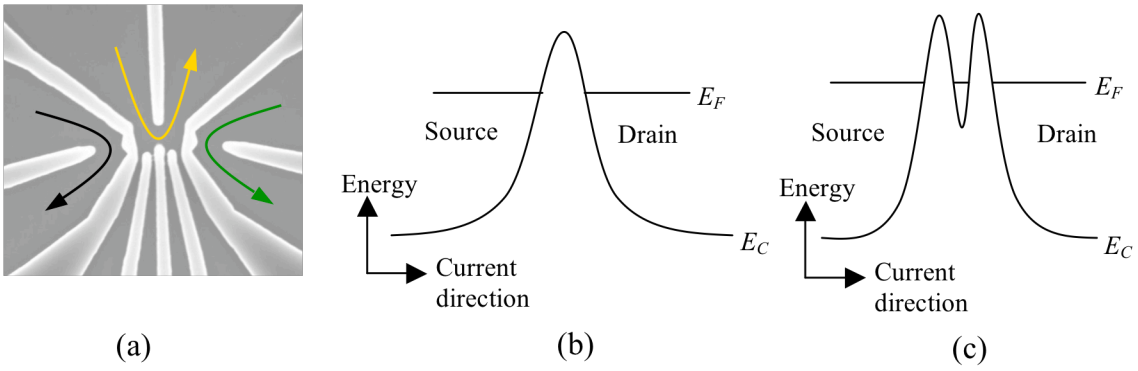
2.3 ENERGY DIAGRAM THROUGH THE CONSTRICTION

It is useful to have a conceptual model of the split gate tunnel barrier, which is consistent with this nanostructure. The energy diagram through the point contact is valuable in explaining the resonant-tunneling features in the current.

In this model, a positive bias on the aluminum top gate creates a high-density electron inversion layer (also known as a two-dimensional electron gas or 2DEG) on either side of the split gates and through the point contact. The two poly-silicon gates forming the point contact are biased negatively into depletion; thus in this region the conduction band edge is brought above the Fermi level, creating a single tunnel barrier. On either side of the point contact are high-density 2DEGs where the Fermi level is well above the conduction band edge. These are the source and drain reservoirs. Ideally, if no

donors or charge defects are present in the constrictions, then a smooth tunnel barrier potential is formed, as shown in Figure 2.4(b). Donors, charge defects, and structure non-uniformity in the gates or local strain can modulate the tunnel barrier potential and form local trapping wells. The binding energy of one or a combination of two oxide charges within approximately 2 nm of the interface has recently been calculated to be on the order of 1-10 meV [31]. In contrast, donors produce a binding energy of approximately 45 meV below the conduction band edge [32]. Schematically this forms a trapping potential within the wide tunnel barrier, Figure 2.4(c), which results in a quantum dot potential with two thinner tunnel barriers. The current peaks whenever an energy level enters the bias window. The bias window is defined as the difference between the Fermi level in the source and the Fermi level in the drain and is set by the source-drain voltage.

Note that for the energy diagrams shown below and in the subsequent chapters of this thesis, the potential well drawn within the tunnel barrier has no special meaning and is purely for illustrative purposes. In general, a donor atom would be represented as an attracting Coulomb potential and a quantum dot potential would be represented as a parabolic potential with equally spaced energy levels as for a quantum harmonic oscillator because the electrons are usually tightly confined in the growth or vertical direction and spread farther in the lateral directions. But unless otherwise noted, these drawings are simply used to describe the resonant-tunneling features seen in later chapters and no inferences should be drawn from the potential wells in the diagrams.



(a) (b) (c)

Figure 2.4 Schematic energy diagrams through the constrictions. (a) SEM image of the poly gate layout. (b) Schematic energy diagram along the green arrow. (c) Along the black and gold arrows. For this energy diagram to be true along the gold arrow, the gates L, LP, RP, and R must be biased positively into inversion to ensure a single constriction forms between the TP and CP gates.

One quantity that is helpful in determining the relative tunnel barrier height is the Fermi level in the source and drain regions. The Fermi level can be estimated by noting that for strong inversion, the two-dimensional electron sheet density is a linear function of the gate voltage [33],

$$n_{2D} = \frac{C_{ox}}{q}\left(V_{AG} - V_{th}\right). \tag{2.3}$$

In this equation, V_{AG} is the aluminum top gate voltage that induces the 2DEG, V_{th} is the threshold voltage, C_{ox} is the oxide capacitance per unit area, and $q = 1.6 \times 10^{-19}$ C is the electron charge. The oxide capacitance is actually two parallel-plate capacitors connected in series and is given by,

$$C_{ox} = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}}, \tag{2.4}$$

$$C_1 = \frac{\varepsilon_1}{t_1} = \frac{3.9\varepsilon_0}{t_1}, \tag{2.5}$$

$$C_2 = \frac{\varepsilon_2}{t_2} = \frac{7.5\varepsilon_0}{t_2}. \tag{2.6}$$

Here $\varepsilon_1 = 3.9\varepsilon_0$ and $t_1 = 35$ nm are the electric permittivity and thickness of the SiO_2 layer and $\varepsilon_2 = 7.5\varepsilon_0$ and $t_2 = 60$ nm are the electric permittivity and thickness of the Al_2O_3 layer. The permittivity of free space is $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m. Using these values in Equations (2.5) and (2.6) and inserting into Equation (2.4) gives an oxide capacitance $C_{ox} = 5.22 \times 10^{-4}$ F/m^2.

The next step is to relate the two-dimensional electron sheet density to the Fermi level. For a 2DEG at zero temperature, the Fermi level is directly proportional to the sheet density [34],

$$E_F = \frac{n_{2D}\pi\hbar^2}{gm^*}. \tag{2.7}$$

In this equation, g is the band degeneracy, m^* is the effective mass, and $\hbar$ is Planck's constant divided by 2π. Spin degeneracy is assumed to be two and has already been applied to this equation. Bulk silicon has an indirect band gap, and six equivalent conduction band valleys in the (100) direction in reciprocal space. In inversion layers on the (100) silicon surface, the degeneracy between these valleys is partially lifted, producing two-fold valley degeneracy [33]. Hence the band degeneracy is $g = 2$. Additionally, free motion occurs in a plane with an effective mass of $m^* = 0.19m_0$, where $m_0 = 9.31 \times 10^{-31}$ kg is the electron rest mass [33]. Using these values, and substituting Equation (2.3) into (2.7), gives the Fermi level in the source and drain 2DEG reservoirs as a function of the top aluminum gate voltage,

$$E_F = m\left(V_{AG} - V_{th}\right), \;\; m = 2.06 \;\; (\text{meV/V}). \tag{2.8}$$

As an example, if the aluminum top gate is V_{AG} = 6 V and the threshold voltage in the source and drain 2DEG regions is V_{th} = 1 V, then the electron density is $n_{2D} = 1.6 \times 10^{12}$ cm^{-2} and the Fermi level is 10.3 meV above the conduction band edge in the source and drain 2DEGs.

CHAPTER 3: FOUR KELVIN MEASUREMENT SETUP

In this chapter, the experimental setup and laboratory tools used to characterize the devices in this thesis are described. Nearly all the measurements were performed at low temperatures. All measurements presented in this thesis were performed in liquid helium at a temperature of approximately four Kelvin (4K) unless otherwise specified. The procedure used to reach low temperatures is described and initial device characterization measurements are presented.

3.1 EXPERIMENTAL SETUP

Recall from Figure 2.4(c) that the energy diagram along the current direction in the split gate point contact consists of a localized confinement potential (i.e., an island for electrons) separated by tunnel barriers to source and drain reservoirs. To observe single electron tunneling effects it is necessary to satisfy two conditions [35]. First, the thermal energy of the system must be much smaller than the charging energy, q^2/C, where C is the total capacitance of the island. The charging energy is the energy required to add or remove a single electron from the localized island.

Second, the tunnel barriers must be sufficiently opaque such that the electron is located either in the source, drain, or on the island. Consider the time to charge or discharge the island, $\Delta t = R_t C$, where R_t is the resistance of the tunnel barrier. From the Heisenberg uncertainty relation we have that $\Delta E \Delta t = (q^2/C) R_t C > h$, which means that the tunnel barrier resistance must be much greater than the resistance $h/q^2 = 25.81\ \text{k}\Omega$ so that the energy uncertainty is much less than the charging energy [35]. These two conditions can be summarized mathematically,

$$q^2/C \gg kT\ , \tag{3.1}$$

$$R_t \gg h/q^2\ . \tag{3.2}$$

Weakly coupling the dot or island from the source/drain leads satisfies the second condition. Performing the measurements at low temperatures can satisfy the first condition. The charging energy in donors is typically around 30 meV [19]. Liquid helium temperature ($T \sim 4$ K) corresponds to a thermal energy of $kT \sim 0.345$ meV. The device is first wire-bonded to a chip carrier, inserted into a dipper, and then dipped into a liquid helium dewar to reach the desired temperature.

There are four separate devices on a sample die. The device is wire-bonded to a 64-pin PGA (Pin Grid Array) connector chip. The chip has a flat surface where the sample is placed and 64 bond pads on the top. Out of the 64 bond pads on the chip, only 24 bond pads are used per device. These 24 bond pads are for the 12 ohmic contacts, one bond pad each for the TP, LP, CP, RP, LQPC, and RQPC poly-silicon gates (six bond pads), and two bond pads each for the L poly-silicon gate, R poly-silicon gate, and the aluminum gate (six bond pads).

Once the device is wire-bonded, the chip is then connected to a PGA board that resides inside a dipper. The dipper is connected to a breakout box. The breakout box is the tool used to interact and communicate with the device. It contains 24 BNC connectors with 24 switches. Each of the 24 bond pads on the chip corresponds to a specific BNC connector and switch. Once the chip is on the board, then a metal sheath is used to completely cover the inside of the dipper.

After the device is inside the dipper and the metal sheath has been sealed, a vacuum pump is used to create a vacuum inside the dipper. Once a vacuum has been

created, helium gas is injected into the dipper. This is done to improve the thermal conductivity because there are no openings in the metal sheath, so no liquid helium enters the inside of the dipper. Thus the device itself will not be immersed in the liquid helium. Then the dipper is inserted into a 100 liter liquid helium dewar.

In addition to low temperatures, a small probing voltage is also necessary. The voltage must be smaller than the energy scales of the effects being measured. The typical source-drain voltage used in the measurements is 100 μV, which corresponds to a temperature of 1.16K.

The currents measured in these devices can be as high as 2 nA and as low as 1 pA. With a source-drain voltage of 100 μV, this corresponds to a resistance range from 50 kΩ to 100 MΩ. Because of these low currents it is important to minimize the noise in the system and properly amplify the signal. Low current measurements in this thesis were made using a current pre-amplifier and a lock-in amplifier, both of which were at room temperature.

Figure 3.1 shows the typical measurement circuit used in this study. In this circuit, the ac signal that comes from the lock-in amplifier is divided down to 1:10,000 its output value, and is passively added to a dc signal that is divided down to 1:100 its output value. There is a capacitive coupling between the various gates and the sample. The output current from the sample is connected to the input of the current pre-amp, which acts as a virtual ground. The current pre-amp amplifies the signal and converts current to voltage. Finally, the lock-in measures the signal. The lock-in and voltage sources are connected through GPIB cables to a computer. The computer uses LabVIEW to collect data and control the voltage sources (LabVIEW code was written by Dr. Nathan Bishop of SNL).

The lock-in frequency was typically 37 Hz; however, depending on the speed of the measurement, frequencies as high as 107 Hz were also used.

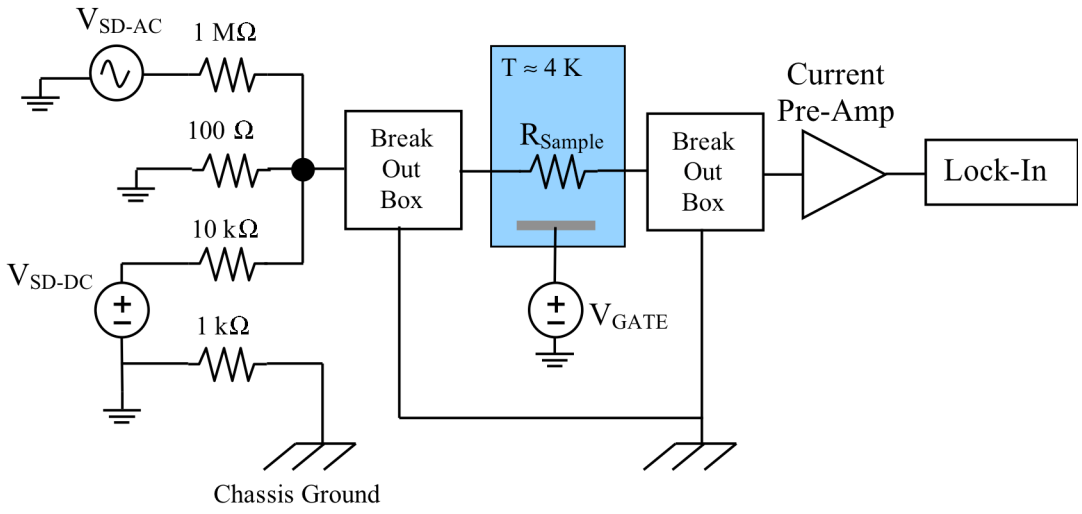


Figure 3.1 Schematic diagram of the measurement circuit used in this study.

3.2 INITIAL DEVICE CHARACTERIZATION

After the device has been dipped into liquid helium, measurements were performed to determine how much positive bias must be applied to the aluminum gate for the device to turn on (threshold voltages), and how much negative bias must be applied to the poly-silicon depletion gates to turn the channel off (pinch-off voltages) once the channel is turned on.

Threshold voltages were measured using the circuit configuration of Figure 3.1 but with the V_{SD-DC} voltage source and 10 kΩ resistor removed from the circuit. A small ac source-drain voltage, ~ 100 μV, is applied across the ohmic contacts. Positive bias is applied to the aluminum top gate to induce the electron inversion layer and the current is

measured as a function of the aluminum gate voltage. All the poly-silicon gates are grounded in these measurements.

At these low temperatures, the p-type silicon substrate will freeze-out and the acceptor states will not be ionized, which creates an insulating substrate. Moreover, the mobility is high at these low temperatures because lattice vibrations will freeze out and the main scattering mechanisms that limit mobility are impurity scattering and interface roughness.

We can determine the effect of low temperatures on the threshold voltage by considering the energy-band diagram of the MOS capacitor. Figure 3.2 shows the energy-band diagram of an MOS system with a p-type semiconductor substrate at threshold and at low temperature. At room temperature, the Fermi level E_F is close to, but still below, the intrinsic Fermi level E_i because the substrate is near-intrinsic p-type. However, at low temperatures the Fermi level is between the valence band edge E_V and the acceptor levels E_a because of freeze-out. This will increase the magnitude of the potential ϕ_p, which is defined as the difference between the Fermi level and intrinsic level in the bulk semiconductor. Consequently, a larger positive voltage must be applied to the metal gate to bend the energy bands sufficiently so that the Fermi level at the surface is as far above the intrinsic Fermi level as the Fermi level is below intrinsic level in the bulk. Thus the threshold voltage at low temperature is larger than the room temperature threshold voltage.

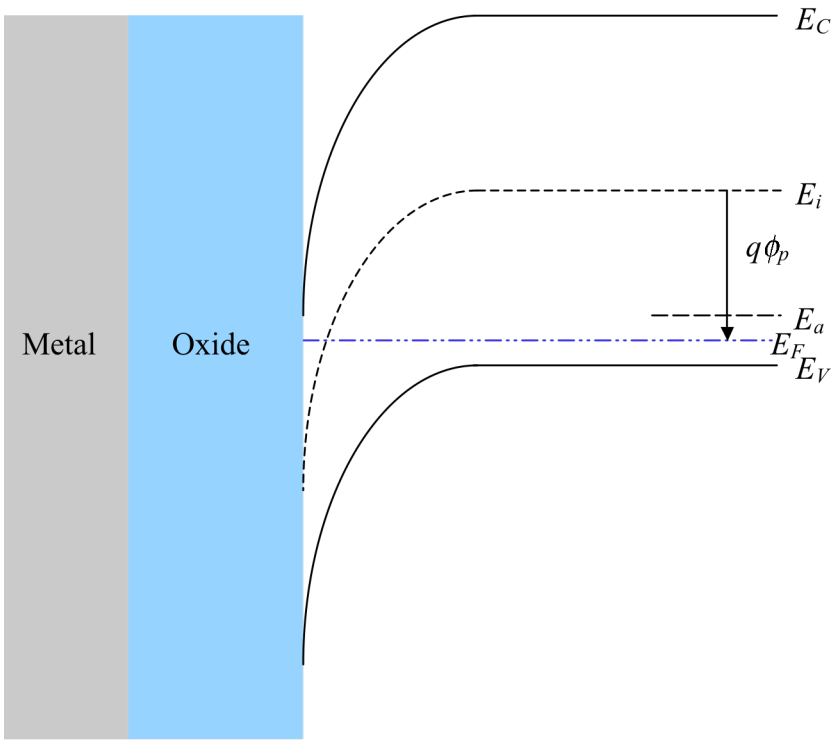


Figure 3.2 Energy-band diagram for an MOS system with a p-type semiconductor substrate biased into inversion and at low temperature.

This effect can also be seen by considering the equation for the threshold voltage for a MOS system with a p-type substrate [30],

$$V_{th} = V_{FB} + 2\left|\phi_p\right| + \frac{1}{C_{ox}}\sqrt{4\varepsilon_s qN_a\left|\phi_p\right|}\,. \tag{3.3}$$

In this equation, the third term accounts for the uniform distribution of uncompensated ionized acceptors in the depletion region, where ε_s is the permittivity of the semiconductor ($\varepsilon_s = 11.7\varepsilon_0$ for silicon), and N_a is the acceptor concentration of the semiconductor. The second term represents the voltage that must be applied to cause the energy bands to be bent in an inverted condition. The first term is the flat-band voltage and is given by,

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}}. \tag{3.4}$$

In Equation (3.4), ϕ_{ms} is the metal-semiconductor work function and the second term represents the shift of the flat-band voltage due to the fixed interface charge density Q_f. Both the second and third term of Equation (3.3) increase for low temperature because of the increased magnitude of the potential ϕ_p; thus the threshold voltage increases for low temperatures.

The current between two nearest neighboring ohmic contacts, with no poly-silicon gates in between, is measured as a function of the aluminum gate voltage. An example of this measurement is shown in Figure 3.3. The ideal current-voltage relationship for an n-channel MOSFET in the non-saturation regime is given by [36],

$$I = \frac{W \mu_n C_{ox}}{2L}\left[2\left(V_{GS} - V_{th}\right)V_{DS} - V_{DS}^2\right]. \tag{3.5}$$

In this equation V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, V_{th} is the threshold voltage, μ_n is the mobility of the electrons in the inversion layer, W is the width of the channel, and L is the channel length. For very small values of V_{DS}, Equation (3.5) can be approximated as,

$$I \simeq \frac{W \mu_n C_{ox}}{L}\left(V_{GS} - V_{th}\right)V_{DS}. \tag{3.6}$$

This equation shows that the current is a linear function of the gate-to-source voltage V_{GS}. Therefore the threshold voltage can be found by fitting a line to a region where the current is linearly dependent on the aluminum top gate voltage and extrapolating to zero current. This measurement is performed for all six ohmic pairs and the threshold voltages extracted are called field thresholds.

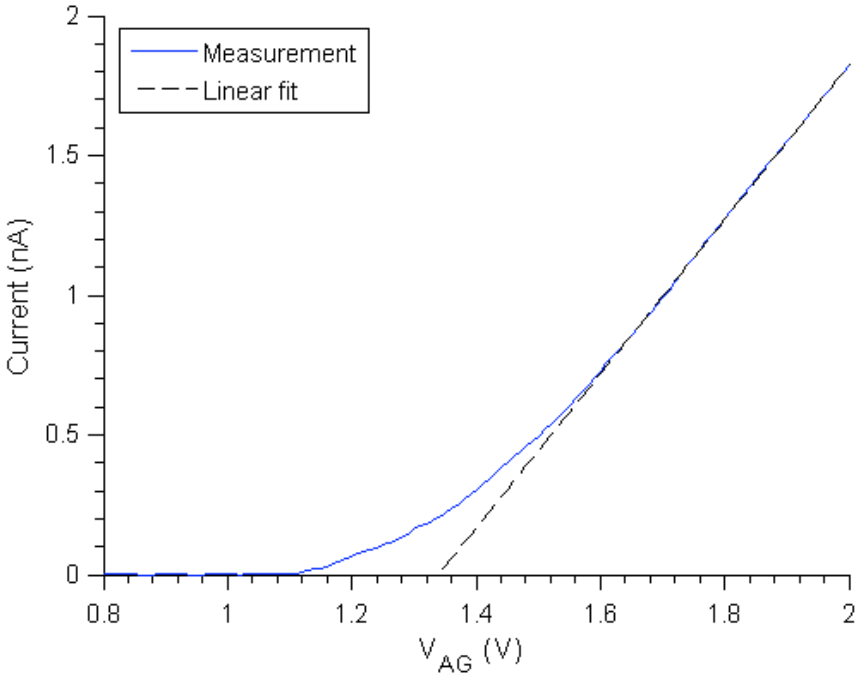


Figure 3.3 Current between two adjacent ohmic contacts (no poly gate between the ohmic contacts) as a function of aluminum gate voltage. The extrapolation of the straight line to zero current gives the threshold voltage, which is about 1.34 V.

Next, the current through the constrictions is measured as a function of the aluminum gate voltage. The threshold voltages for the constrictions can be considerably larger than the field thresholds because the electrons are forced to travel through a narrow space defined by the poly-silicon gates. Examples of these measurements are shown in Figure 3.4. Measured values of the average field thresholds and thresholds in the constrictions for the samples considered in this thesis are shown in Table 3.1.

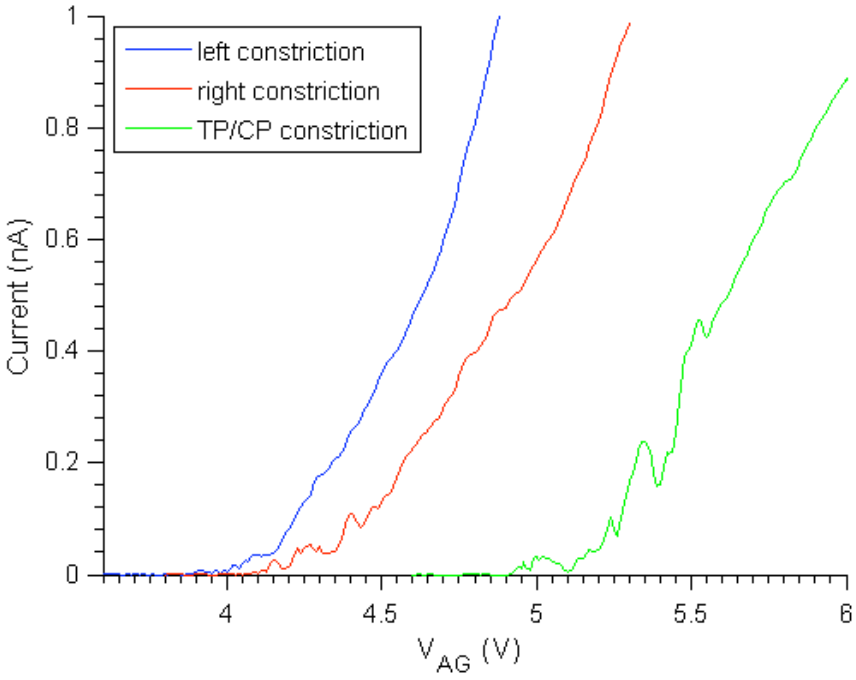


Figure 3.4 Current through the constrictions as a function of aluminum gate voltage.

Table 3.1 Measured threshold voltages in the field and the constrictions.

Device	Description	Avg. Field Threshold (V)	Standard Deviation (V)	Left Constriction (Implant) Threshold (V)	Right Constriction (Control) Threshold (V)	TP/CP Constriction (Implant) Threshold (V)
S561UR	120 keV Sb implant	1.9	0.72	2.4	2.5	5.8
S561UL	120 keV Sb implant	1.3	0.56	4.3	4.4	5.3
S562LL	120 keV Sb implant	1.1	0.29	2.8	2.9	3.0

It can be seen from Figure 3.4 and Table 3.1 that the threshold in the TP/CP constriction is greater than for the other two constrictions. One possible reason for this observation can be explained by considering the SEM image of Figure 2.2. Both the left and right constrictions are approximately 270 nm. In contrast, electrons traveling through the TP/CP constriction actually have to pass through three constrictions, i.e., the

constrictions between TP and L, between TP and CP, and between TP and R. As seen in Figure 2.2 these constrictions can be smaller than 270 nm, which can lead to larger threshold voltages.

The current does not turn on smoothly at these temperatures. At low temperatures a number of effects introduce energy and voltage dependence in the transmission through a barrier. The wide range of thresholds and complex voltage dependence of the current indicate that changes in lithography and fabrication can significantly change the tunnel barrier. However, the energy dependent transmission is complex and difficult to model and the threshold voltages alone provide little quantitative information about the tunnel barrier itself, although they do provide information about the charge density in the dielectrics and the coupling capacitances. In the following chapter we will show that a rectangular barrier model agrees well with the observed tunneling current dependence on voltages and provides a characteristic barrier height and width.

The final test is gate pinch-off. A small ac source-drain bias is applied across a point contact and the aluminum top gate is used to form a channel in the constriction. The aluminum top gate is held at a fixed positive voltage while negative bias is applied to a poly-silicon depletion gate to turn off the channel. This is tested in all three constrictions. In the left constriction, the LQPC and L gates are used individually to pinch-off the channel. While one gate is being swept, the other gate is grounded. A similar procedure is used in the right constriction but with the RQPC and R gates.

The TP/CP constriction is slightly more complicated because there is more than one constriction. In order to ensure that the only constriction formed is between the TP and CP gates where the donors are implanted, the L, LP, RP, and R gates are biased

positively into inversion so that there is unrestricted electron transport under these gates and these constrictions are open. Then the TP and CP gates are used individually to pinch-off the channel. Examples of these measurements for the three split gate point contacts studied in this thesis are shown in Figure 3.5.

As seen in all of these scans, there are numerous resonances in the pinch-off curve. Resonances through a point contact normally result from tunneling through a localized confinement potential or charge center within the tunnel barrier. As mentioned previously, these trapping potentials can be due to intentionally implanted donors or charge defects in the oxide.

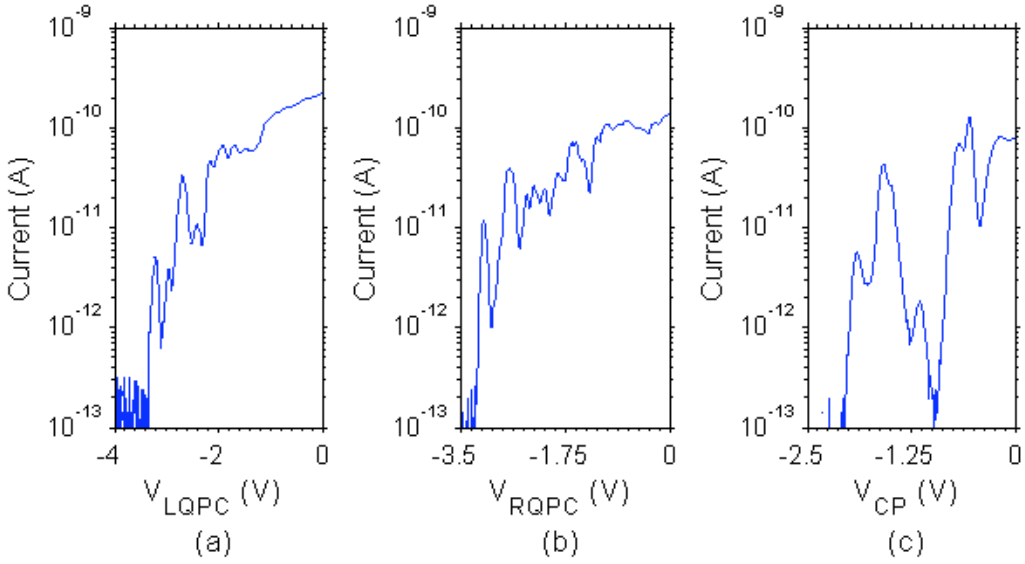


Figure 3.5 Examples of pinch-off curves for sample 561. (a) Left constriction. Current through the left point contact as a function of LQPC gate voltage with V_{AG} = 4.4 V. (b) Right constriction. Current through the right point contact as a function of RQPC gate voltage with V_{AG} = 4.6 V. (c) TP/CP constriction. Current as a function of the CP gate voltage with V_{AG} = 5.72 V, V_{TP} = 0 V, V_R = V_L = 1.5 V, and V_R = V_L = 1.5 V.

CHAPTER 4: TUNNEL BARRIERS WITHOUT IMPLANTS AND TUNNEL BARRIER MODEL WITH VOLTAGE DEPENDENT BARRIER HEIGHT

This chapter presents transport measurements of tunnel barriers without implantation, which is the right side point contact. We call this the "control" case. The constriction was masked by 300 nm of PMMA during the implantation process, which should be sufficient to block the implant from reaching the silicon and therefore there are no antimony donor atoms in this constriction. In addition, this chapter examines the agreement of a tunneling model to the observed current dependence on voltage. In particular, a capacitance model for the barrier height dependence on voltage is introduced along with assuming a simple rectangular potential for the barrier. The model produces reasonable agreement with the experiment leading to an estimate of barrier height and width, which can be used to quantitatively describe each tunnel barrier with two physical parameters. This rectangular barrier model will be used throughout this study to characterize and compare the tunnel barriers formed in the constrictions.

In the first section, the energy diagram along the current direction will be revisited and its dependence on depletion gate voltage and dc source-drain bias will be discussed. This will help in understanding the stability plots that are used to examine the constrictions. Next, transport measurements through the control constriction (right point contact) will be presented and discussed. Finally, the tunnel barrier model will be introduced and used to characterize the control constriction tunnel barrier.

4.1 TRANSPORT CHARACTERISTICS AND STABILITY PLOTS

In this study, the point contacts are examined by using transport spectroscopy. This is accomplished by measuring the differential conductance dI/dV_{SD} as a function of the dc source-drain bias V_{SD} and gate voltage V_G. The differential conductance is measured by adding a dc offset V_{SD} to the ac signal provided by the lock-in. The resulting two-dimensional plots are often referred to as stability plots. It is helpful to look at the energy diagram along the current direction to understand these stability plots.

First consider a constriction devoid of defects and donors so that a smooth tunnel barrier potential is formed. Assume a small ac source-drain voltage is applied across the constriction and that the drain lead is grounded. If enough negative bias is applied to the poly-silicon depletion gates there will be a point at which the Fermi level in the source and drain regions matches the top of the barrier, Figure 4.1(a). If more negative bias is applied to the poly gates then the barrier height will increase and exceed the Fermi levels in the source and drain. Below this point, transport is rapidly suppressed and the conductance will be zero. This is shown in Figure 4.1(b).

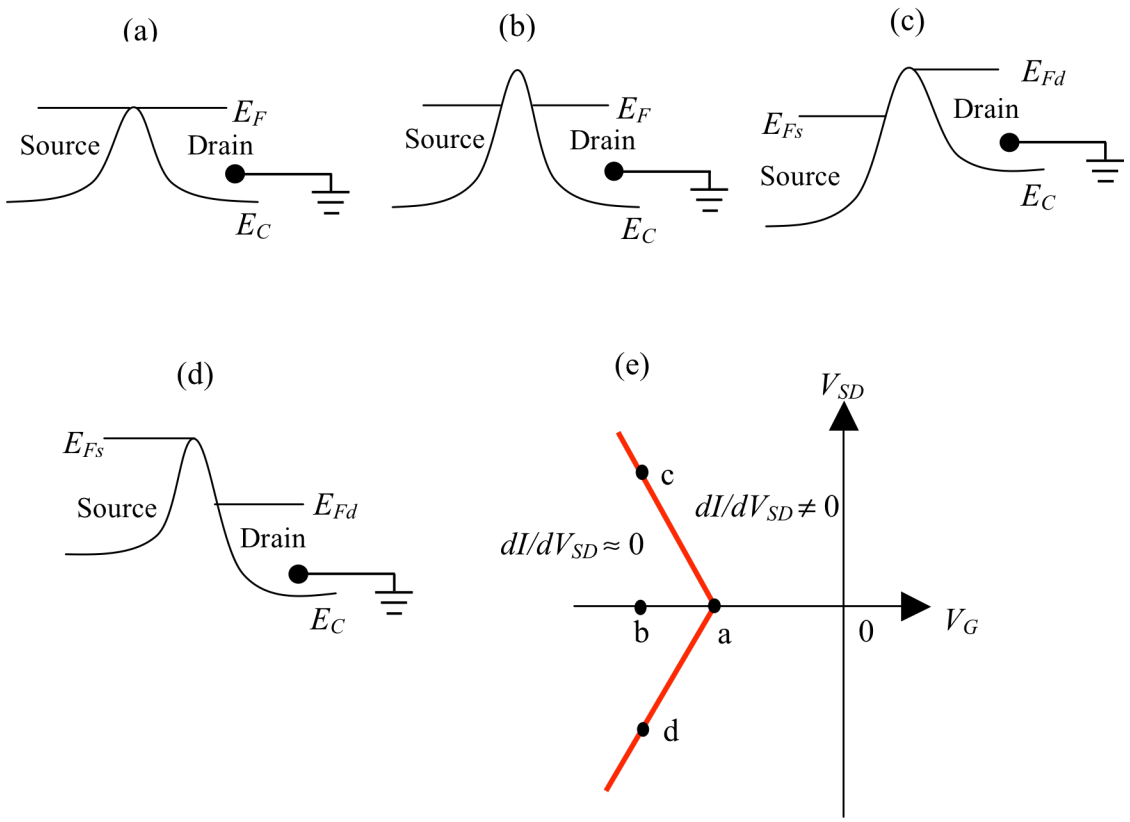


Figure 4.1 Energy diagrams along the current direction and schematic diagram of the differential conductance for a split gate tunnel barrier that is free of donors and charge defects. (a) The Fermi level in the source and drain match the top of the barrier. (b) More negative voltage applied to a depletion gate increases the barrier height so that it exceeds the Fermi level in the source and drain. (c) Positive dc source-drain bias applied to the source lowers the quasi-Fermi level in the source and also decreases the tunnel barrier height. (d) Negative dc source-drain bias applied to the source increases the quasi-Fermi level in the source and the tunnel barrier with respect to the quasi-Fermi level in the drain. (e) Resulting differential conductance plot as function of V_{SD} and V_G. The red lines define the conduction band edge. The energy diagrams in (a-d) correspond to the points shown in (e).

Now if a positive dc source-drain bias is applied across the constriction, then quasi-Fermi levels can be used to describe the relative positions of the chemical potentials of the two leads. That is the quasi-Fermi level in the source will decrease in energy with respect to the quasi-Fermi level in the drain. The source-drain voltage sets the difference in the quasi-Fermi levels

$$E_{Fs} - E_{Fd} = -qV_{SD}\,. \tag{4.1}$$

In this equation, E_{Fs} is the quasi-Fermi level in the source and E_{Fd} is the quasi-Fermi level in the drain. The barrier height will also decrease a fraction of the applied source-drain bias. That is the barrier height depends on the bias of all gates including the source and drain. If enough positive source-drain bias is applied, then eventually the top of the barrier will match the quasi-Fermi level in the drain and current will begin to flow again. This is shown in Figure 4.1(c).

Similarly, if a negative dc source-drain bias is applied across the constriction, the quasi-Fermi level in the source increases with respect to the quasi-Fermi level in the drain. The barrier height also increases a fraction of the applied bias. Eventually, when enough negative source-drain bias is applied, the quasi-Fermi level in the source will match the top of the barrier and current will begin to flow again. This is shown schematically in Figure 4.1(d).

A drawing of the differential conductance versus gate voltage and dc source-drain voltage for the situation just described is shown Figure 4.1(e). In this drawing, the red lines separate regions where dI/dV_{SD} has some non-zero value and regions where $dI/dV_{SD} \approx 0$ (below the noise floor). Also shown in this figure are points that correspond to the energy diagrams in Figures 4.1(a-d).

Now suppose that a charge center is present in the constriction so that there is an energy level below the band edge. In this case, the current peaks when the energy level enters the bias window defined by $E_{Fs} - E_{Fd} = -qV_{SD}$. If the resonant energy level is outside of the bias window then an electron cannot tunnel from the source/drain leads onto the charge center; thus no current flows. This is known as Coulomb blockade.

The energy diagrams through the point contact for zero applied source-drain voltage, positive source-drain voltage, and negative source-drain voltage are shown in Figures 4.2(a-c), respectively. Now both the tunnel barrier potential and energy level are affected by the gate voltage and source-drain bias. Again note that these drawings are simply used to describe the resonant-tunneling features and no inferences should be drawn from the potential wells in the diagrams.

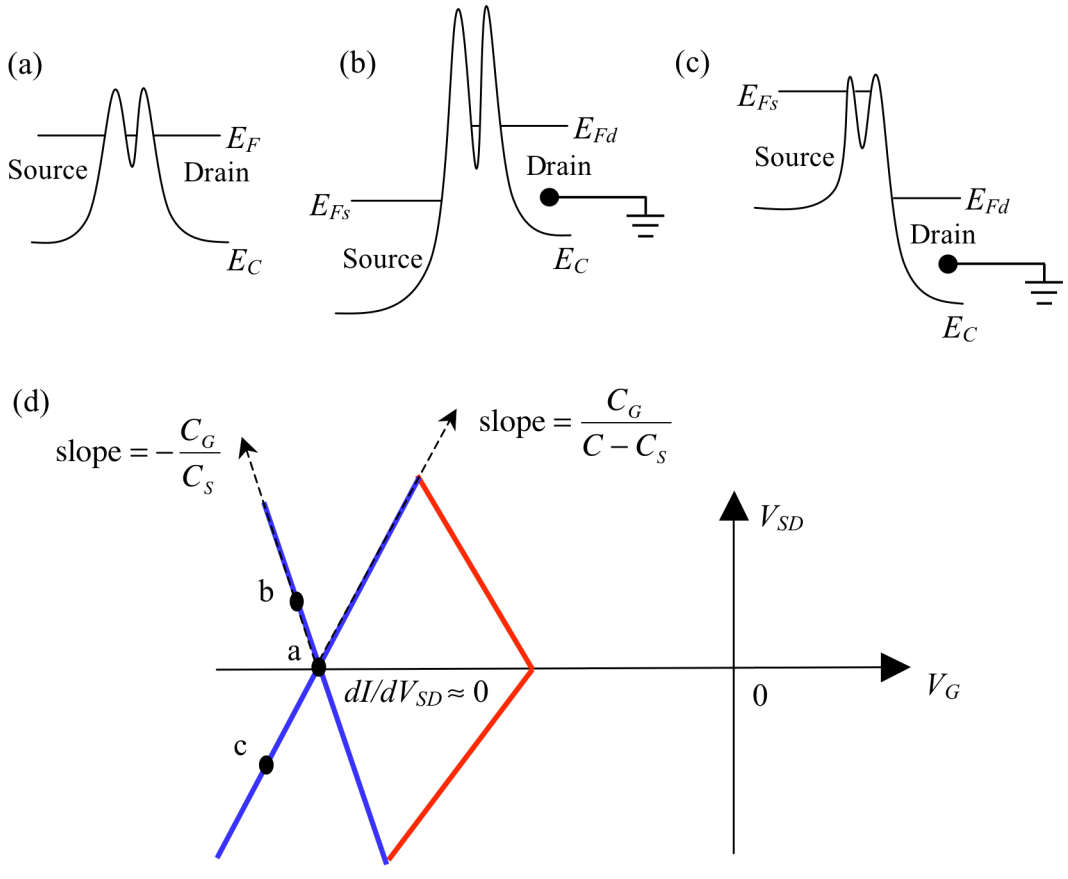


Figure 4.2 Energy diagrams along the current direction and schematic diagram of the differential conductance for a split gate tunnel barrier that contains a single resonant energy level below the conduction band edge. Energy diagram for (a) zero applied source-drain bias (b) positive source-drain bias and (c) negative source-drain bias. In each case the resonant energy level is aligned with either the quasi-Fermi level in the source or the drain. (d) Resulting differential conductance plot as a function of V_{SD} and V_G. The red lines define the conduction band edge and the blue lines define the resonant level. The energy diagrams in panels (a), (b), and (c) correspond to the points shown in (d).

A drawing of the differential conductance versus gate voltage and source-drain voltage for this case is shown in Figure 4.2(d). The edges of the diamond-shaped regions (red and blue solid lines) correspond to the onset of current. Inside the diamond-shaped areas are regions of Coulomb blockade where the differential conductance is approximately zero. The diamonds are called Coulomb diamonds. Inside the diamonds the number of electrons is fixed. The size and shape of the diamonds reflect the regions where the charge on the device is stable. Thus, these plots are referred to as stability plots [37]. In this figure the red lines delineate the band edge and the blue lines delineate the resonant level below the band edge. The edges of the diamond correspond to voltages at which the band edge or resonant level are aligned with either the source or drain quasi-Fermi level. As seen in Figure 4.2 (d), the Coulomb blockade can be lifted in two ways: (1) By changing the gate voltage V_G, which shifts the tunnel barrier potential and the resonant energy levels with respect to the source/drain reservoirs, and (2) by changing the dc source-drain bias V_{SD}, which increases the bias window and also drags the tunnel barrier potential and energy levels along, because of the capacitive coupling to the source.

It is important to note that the slopes of the two edges of the resonance depend on the capacitances of the system. Assuming the drain 2DEG region is grounded the positive slope of the resonance equals $C_G/(C - C_S)$ and the negative slope equals $-C_G/C_S$, which is shown schematically in Figure 4.2(d). Here C is the total capacitance between the localized electron state and all the conductors in the system, C_S is the capacitance between the source 2DEG region and the localized state, and C_G is the capacitance

between the gate and the localized state [38]. The capacitive coupling between the resonant state and the source and between the resonant state and the gate, which are given by C_S/C and C_G/C respectively, can be determined by estimating the positive and negative slopes of the resonance from the differential conductance plot and using the above the expressions.

Finally, consider the ideal case for which a single donor is in the split gate tunnel barrier, Figure 4.3(a). Here the potential well is represented as an attracting Coulomb potential and there are two resonant energy levels below the conduction band edge: the neutral D^0 state where a single electron is bound to the donor and the negatively charged D^- state where a second electron is more weakly bound to the donor due to the strong repulsive Coulomb interaction. Hence we expect two resonances below the band edge in the differential conductance plot, Figure 4.3(b). The resonances should have approximately the same slopes because the capacitances are attributed to the same donor.

The difference between the D^0 and D^- energy levels gives the charging energy. This value can be determined from the stability diagram. As seen in Figure 4.3(b) the charging energy is given by the peak of the diamond formed by the resonances that correspond to the transitions from $D^+ \leftrightarrow D^0$ and from $D^0 \leftrightarrow D^-$. However, this is a highly idealized system in which a single donor is in the tunnel barrier. Other donors, charge defects, or other forms of disorder can be present in the constriction that can cause resonances in the transport measurements. Thus one must be careful in assigning the peak of a diamond as the charging energy. We will first discuss the transport measurements of the non-implanted or control constriction and defer the transport measurements of the implanted constrictions for the next chapter.

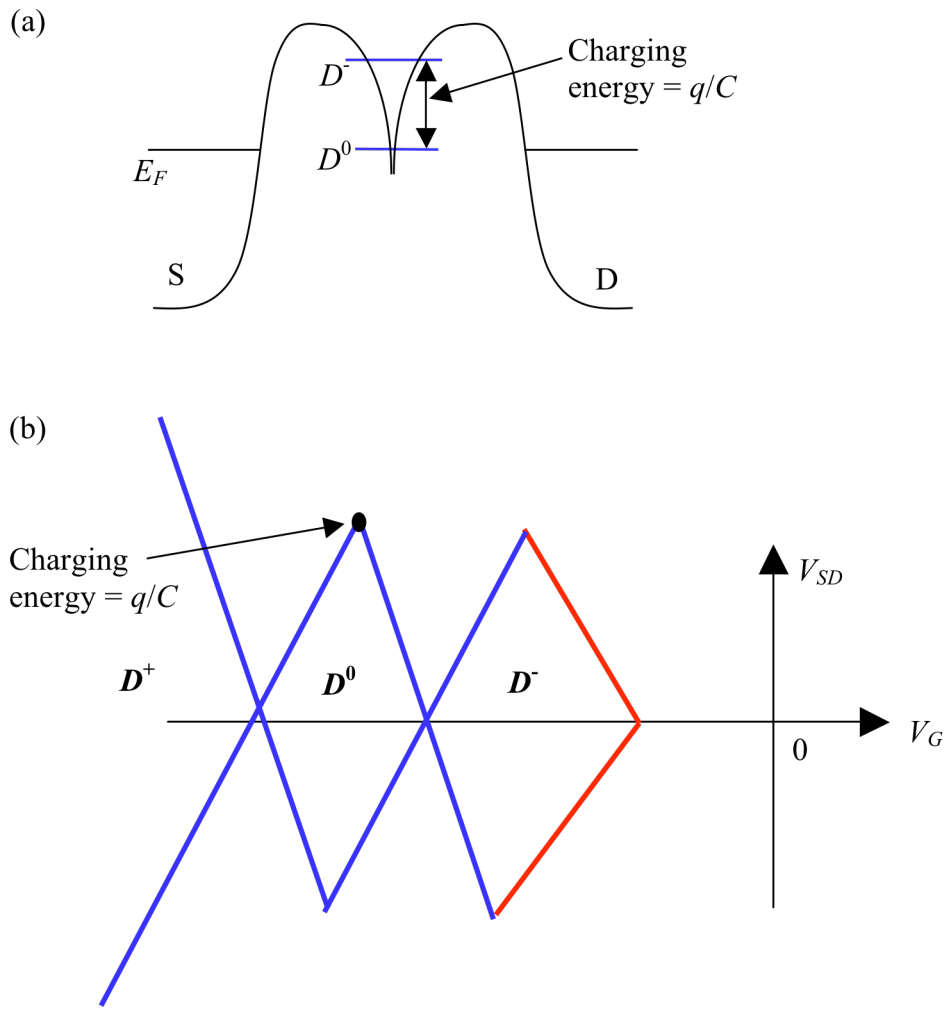


Figure 4.3 (a) Conceptual energy diagram along the current direction and (b) schematic diagram of the differential conductance for a split gate tunnel barrier that contains a single donor. Drawings are adapted from reference [39].

4.2 CONTROL CONSTRICTION: TRANSPORT MEASUREMENTS

In this section the transport measurements of the right constriction (gates R and RQPC) are examined. Figure 4.4 shows a plot of the differential conductance of the right

point contact of sample 562 as a function of the dc source-drain voltage and the RQPC gate voltage. The ac signal from the lock-in was a 107 Hz 100 μV excitation. The aluminum top gate was V_{AG} = +3.3 V and the R gate was V_R = -0.5 V.

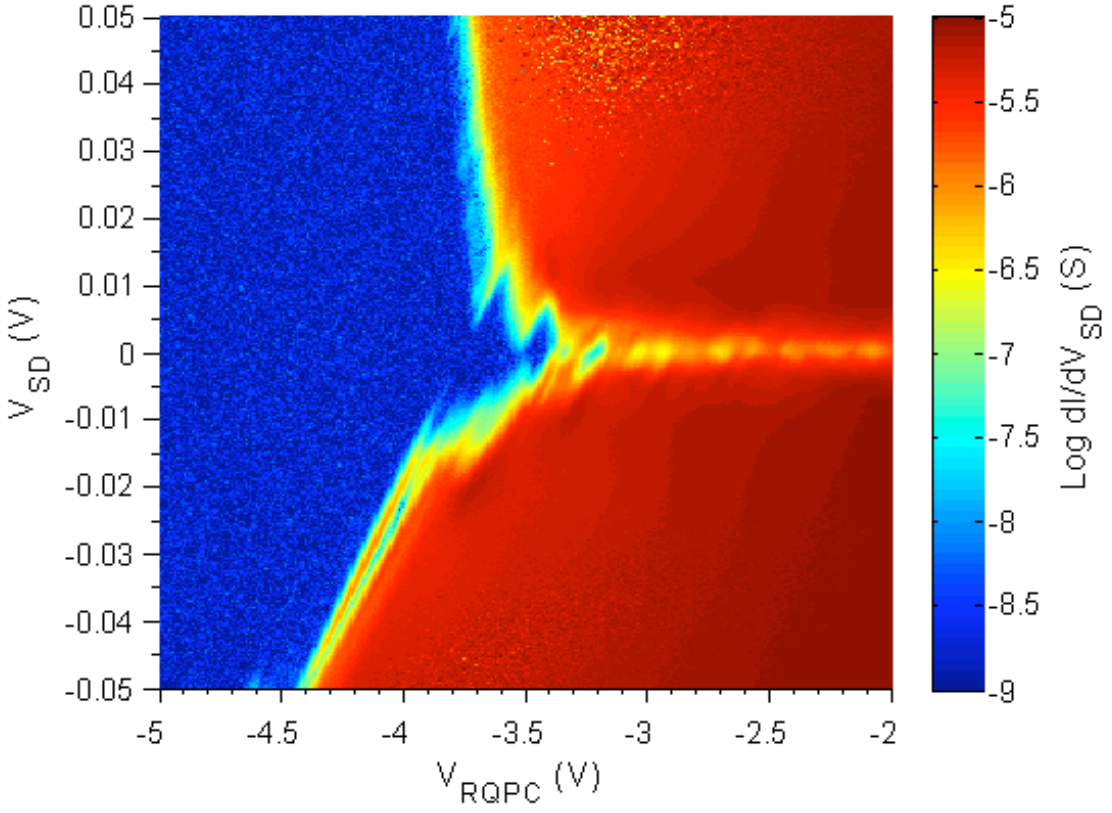


Figure 4.4 Transport through the control constriction of sample 562. The plot shows the differential conductance as a function of the dc source-drain bias and RQPC gate voltage. Voltages on remaining gates are V_{AG} = 3.3 V and V_R = -0.5 V. The resonances seen at low source-drain voltages are most likely due to tunneling through unintentional dots in the constriction.

To create such a scan, a single trace of dI/dV_{SD} versus V_{SD} at a fixed value for V_G (in this case V_{RQPC}) is taken. For the next trace V_G is changed slightly and this process is repeated many times [37]. The scan in Figure 4.4 had a total of 300 traces each with 500 data points.

This plot is a good qualitative representation of most of the control constrictions measured in this study. Ideally, the stability diagram of the control constriction would look similar to the drawing in Figure 4.1(e); however this is not what is seen in Figure 4.4. Instead many resonances are seen at low source-drain voltages. Disorder, such as charge defects in SiO_2 layer, impurities, or structural defects, can cause variations in the potential of the conducting channel. These defects can create relatively deep confining potentials that can trap a small number of electrons. That is the defects can produce an unintentional quantum dot. This can lead to Coulomb blockade in the transport measurement through the constriction [28]. This can be seen more clearly by taking a line cut at zero source-drain bias of the stability diagram in Figure 4.4, which is shown in Figure 4.5. The presence of these defect related resonances in the transport measurements are a significant problem because they make it difficult to probe the single electron behavior from the intentionally implanted antimony donors.

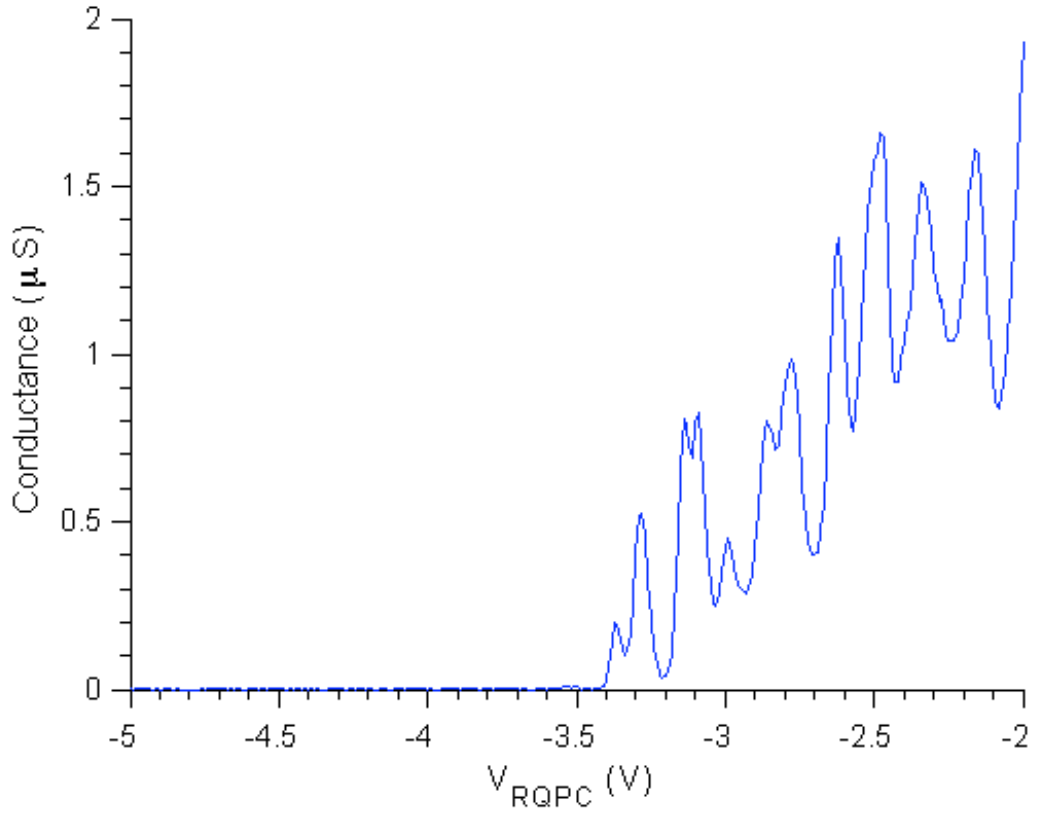


Figure 4.5 Coulomb blockade in transport through the control constriction of sample 562. The plot was obtained by taking a line cut along $V_{SD} = 0$V in Figure 4.4. The plot shows periodic oscillations in the conductance through the constriction at 4K. The resonances are most likely due to resonant tunneling through an unintentional localized trapping potential within the split gate tunnel barrier.

Now consider regions in the stability diagram of Figure 4.4 where $|V_{SD}| > q/C$, that is the Coulomb blockade is lifted. In this regime the tunneling current is only limited by the transmission through the most opaque barrier or a combination of two similarly balanced barriers rather than depending on the statistics of occupation of the dot. That is the current does not depend on the exact quasi-Fermi level's alignment with the lowest occupation chemical potential level of the trapping potential in the barrier. We also assume that the effect of reflection is small in this regime.

For a constant $V_{SD} > q/C$, for example a line cut of $V_{SD} = 25$ mV from Figure 4.4 shown in Figure 4.6, the conductance first increases exponentially as the depletion gate voltage becomes more positive and the quasi-Fermi level is approaching the top of the barrier. This is consistent with a single barrier limiting the transmission coefficient, which is continuously raised or lowered by changing the depletion gate voltage. For more positive depletion gate voltage the conductance increases more gradually, which corresponds to a bias regime for which the quasi-Fermi level is close to the barrier height, and is probably limited by a series resistance in the source/drain starting to take effect.

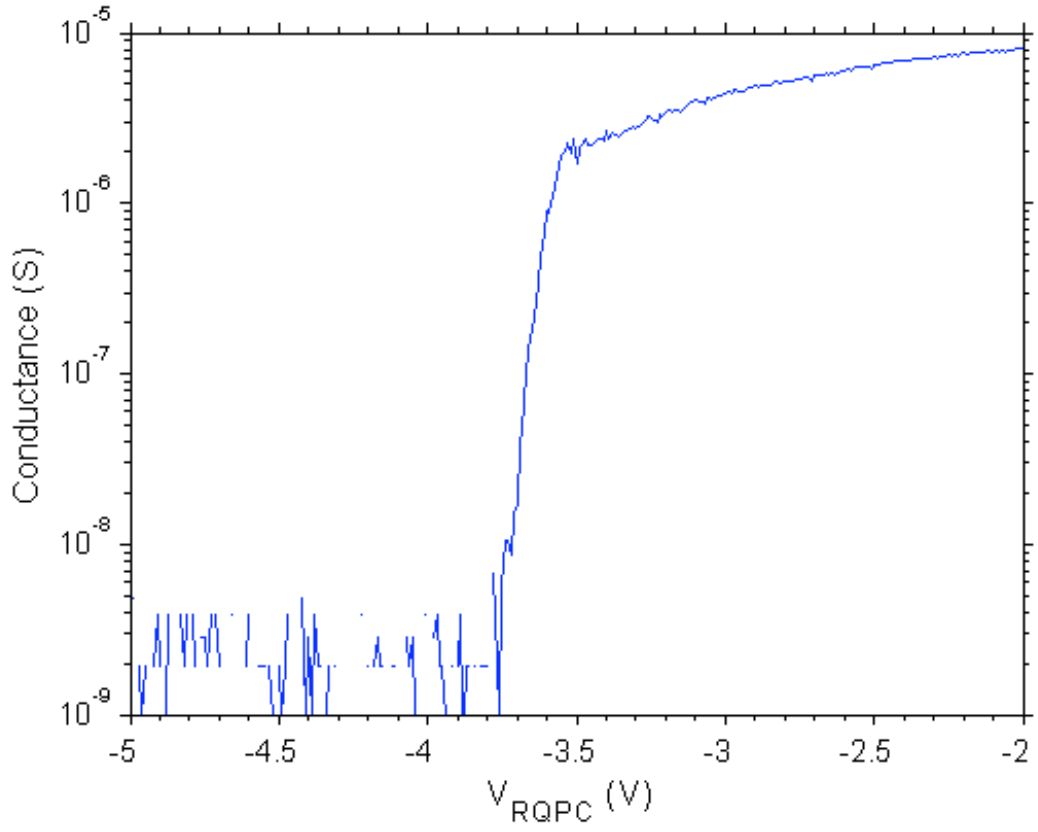


Figure 4.6 Transport through the control constriction of sample 562 for $V_{SD} > q/C$. The plot was obtained by taking a line cut along $V_{SD} = 25$ mV from Figure 4.4. This plot shows an exponential turn-on followed by a region where the conductance increases more slowly due to some series resistance in the source/drain.

The key observation from Figure 4.6 is that for a constant dc source-drain bias the conductance increases exponentially for more positive depletion gate voltage showing a classic tunneling dependence. One question is whether the measured values of conductance can be used to deduce other properties about the tunnel barrier such as barrier height and width. In the next section, we approximate the tunnel barrier as a rectangular barrier to model the tunneling current. When using a capacitance model for the barrier height dependence on voltage, the model is found to agree well with experiment.

4.3 TUNNELING MODEL

A one-dimensional rectangular potential barrier of height U_0 and thickness w is shown in Figure 4.7. The quantum mechanical probability of tunneling through the barrier (also known as the transmission coefficient) for a particle, such as an electron, is used to define the ratio of transmitted flux to incident flux. For a particle incident on the barrier from the left and with energy $E < U_0$ the transmission coefficient is given by [34],

$$T = \frac{1}{1 + \dfrac{U_0^2 \sinh^2 \kappa w}{4E(U_0 - E)}}. \tag{4.2}$$

In this equation, κ is the wave number and is given by,

$$\kappa = \sqrt{\frac{2m(U_0 - E)}{\hbar^2}}, \tag{4.3}$$

where m is the mass of the particle.

If κw is large then the transmission coefficient can be approximately written as,

$$T \approx 16 \frac{E}{U_0}\left(1 - \frac{E}{U_0}\right)\exp(-2\kappa w). \tag{4.4}$$

This equation is dominated by the exponential term; thus the probability of tunneling through the barrier can be estimated as $T \approx \exp(-2\kappa w)$.

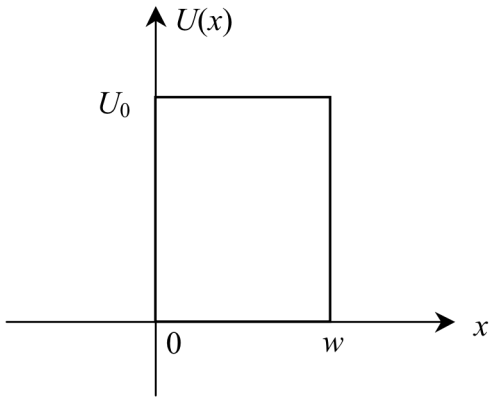


Figure 4.7 Rectangular potential barrier of height U_0 and thickness w.

The next step is to relate the transmission coefficient to the current. Figure 4.8 shows the energy diagram through the resonant charge center assuming rectangular barriers for large dc source-drain bias such that $V_{SD} > q/C$. The thick black lines represent the rectangular tunnel barriers. All the states below the quasi-Fermi levels in the source and drain are filled, which are represented by the gray regions. In this case there is more than one chemical potential μ within the bias window. Here the more opaque tunnel barrier limits the tunneling current.

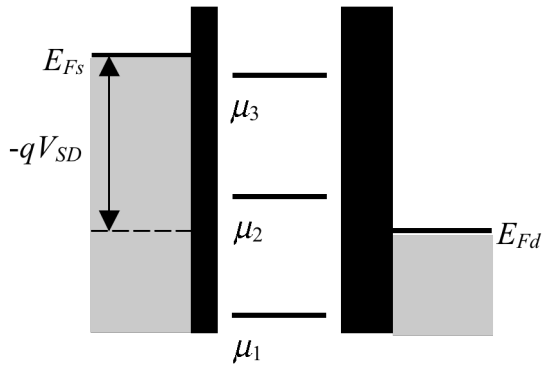


Figure 4.8 Energy diagram through the resonant charge center assuming rectangular barriers for large dc source-drain bias such that $V_{SD} > q/C$. There is more than one chemical potential μ within the bias window defined by the quasi-Fermi levels in the source and drain. In this case the less transmissive barrier will limit the tunneling current.

For a large bias in the unblocked regime, the magnitude of the current can be approximated as,

$$I \approx qfT \,. \tag{4.5}$$

Here this assumes there is a substantially more opaque barrier and T is the lesser of the transmission coefficients of the left and right tunnel barriers. The parameter f is a constant frequency value that has units of Hz. As will be shown below, the values of tunnel barrier height and width are logarithmically sensitive to the value of f and thus depend little on the estimate of this parameter; a constant value of 1 THz is assumed in this study [26]. Using the rectangular barrier approximation the transmission coefficient can be written approximately as $T \approx \exp(-2\kappa w)$ and using Equation (4.3) the current becomes,

$$I \approx qf \exp\left(-\frac{2w}{\hbar}\sqrt{2m(U-E)}\right). \tag{4.6}$$

The goal is to use this equation and the measured values of conductance to calculate the relative tunnel barrier height $\Delta = U - E$ and the tunnel barrier width w.

The measured data in Figure 4.4 gives values of differential conductance dI/dV_{SD} but Equation 4.6 is an equation for current I. Thus the numerical integral of the data is taken using MATLAB. This is shown in Figure 4.9 where the magnitude of the dc current is plotted as a function of dc source-drain bias and RQPC gate voltage.

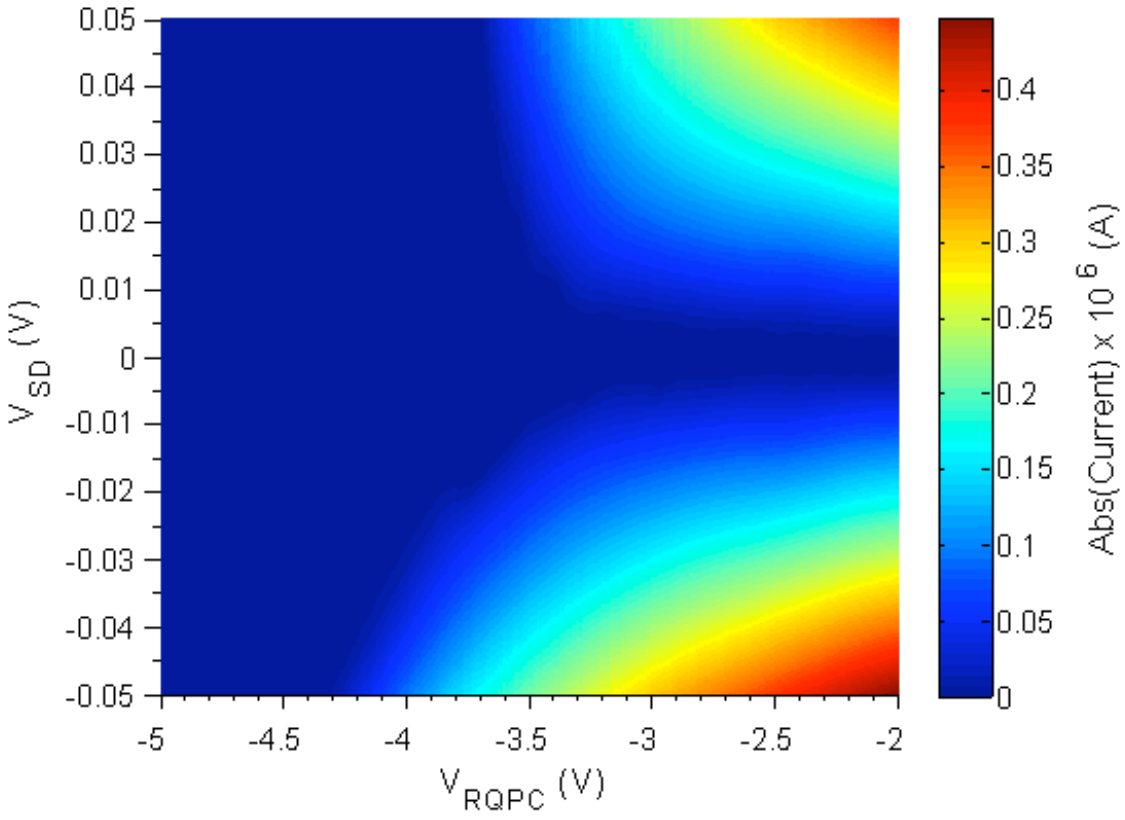


Figure 4.9 Magnitude of the dc current through the right constriction of sample 562. The plot was obtained by numerically integrating the data in Figure 4.4 using MATLAB.

Figure 4.10 shows a line cut along V_{SD} = 30 mV, which shows an exponential region in the I-V_{RQPC} plot where a line can be fit. To fit the data to Equation 4.6 a few additional approximations must be made.

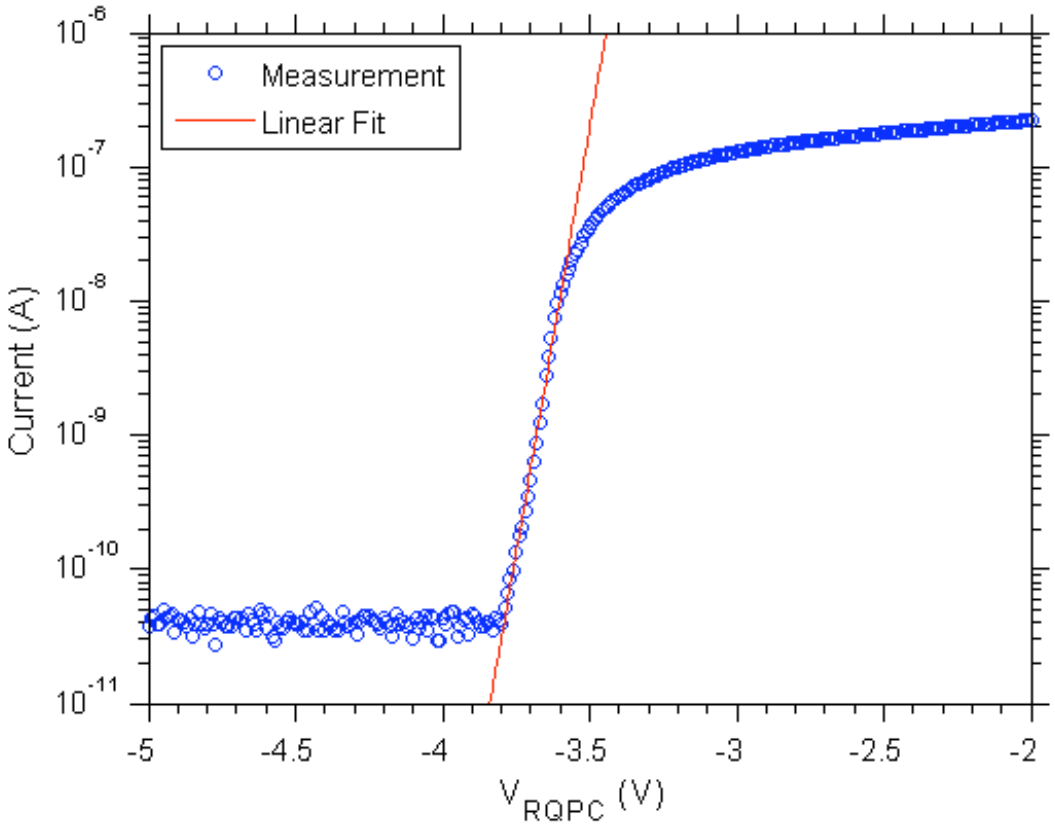


Figure 4.10 Current through the control constriction as a function of the RQPC gate voltage for V_{SD} = 30 mV (plotted in a semi-logarithmic scale). The plot was obtained by taking a line cut from Figure 4.9. The red line is a linear fit used to extract the tunnel barrier height and width.

First, a linearization of the square root in the exponential is performed to facilitate the linear fit (i.e., a Taylor expansion to first order). The square root in the exponential is a function of two variables (U and E), thus the linear approximation is,

$$\sqrt{U-E} \simeq \sqrt{\Delta} + \frac{1}{2\sqrt{\Delta}} dU - \frac{1}{2\sqrt{\Delta}} dE \,. \tag{4.7}$$

In this equation, the parameter Δ is equal to $U - E$ at some arbitrary value of U and E.

The tunnel barrier height is treated as a function of gate voltage, aluminum top gate voltage, and source-drain bias. Assuming a simple capacitance model for the functional dependence, we model small changes in the tunnel barrier potential dU as linearly dependent on small changes in the source-drain bias V_{SD} and the depletion gate voltage V_G [26],

$$dU = -q\alpha_{SD}dV_{SD} - q\alpha_G dV_G \,. \tag{4.8}$$

The parameter α_{SD} is the capacitive coupling of V_{SD} to the tunnel barrier potential and α_G is the capacitive coupling of V_G to the tunnel barrier potential. These two parameters are estimated by measuring the positive and negative slopes of the resonance from the stability plot as was discussed in Section 4.1.

In the particular case of the experiment, the magnitude of Δ is referenced to the energy, E, of the quasi-Fermi level. The quasi-Fermi level is considered constant. Affects such as the top-gate influence on electron density are neglected because they are small relative to the barrier height change with voltage. Barrier shape dependence on lateral field is also neglected, which is a feature of arbitrarily fitting the tunnel barrier to a rectangular barrier form. In the case that there is a resonance within the barrier, the voltage dependence of Δ is considered independent of the chemical potential of the resonance because the Coulomb blockade is lifted in the regime of high V_{SD}. We therefore reference Δ to $E \approx E_F$.

If the depletion gate voltage is the only parameter that is changing and the aluminum top gate voltage and the source-drain bias are held constant then the last term on the right-hand side of Equation (4.7) and the first term on the right-hand side of

Equation (4.8) can be removed. Then substituting Equations (4.7) and (4.8) into Equation (4.6) and after some simplification the following equation is obtained,

$$I = qf \exp\left(-\frac{2w}{\hbar}\sqrt{2m\Delta}\right)\exp\left(\frac{qw\alpha_G}{\hbar}\sqrt{\frac{2m}{\Delta}}dV_G\right). \tag{4.9}$$

This equation can be rewritten in the following form,

$$I = I_0 \exp\left[\beta \cdot dV_G\right] = I_0 \exp\left[\beta\left(V_G - V_0\right)\right]. \tag{4.10}$$

Where the parameters I_0 and β are equal to,

$$I_0 = qf \exp\left(-\frac{2w}{\hbar}\sqrt{2m\Delta}\right), \tag{4.11}$$

$$\beta = \frac{qw\alpha_G}{\hbar}\sqrt{\frac{2m}{\Delta}}. \tag{4.12}$$

The equation for the magnitude of the tunneling current can be written in a simple exponential form. The parameters I_0 and β both depend on the tunnel barrier height Δ and the barrier width w. I_0 and β can be found by fitting a line to the region where the current depends exponentially on the gate voltage as shown in Figure 4.10. The parameter β is the slope, I_0 is value of the current, and V_0 is value of the voltage at the point around which the Taylor expansion is done. Once these values are determined from the I-V_G plot then Equations (4.11) and (4.12) can be used to solve for Δ and w which then give,

$$\Delta = -\frac{q\alpha_G}{2\beta}\ln\left(\frac{I_0}{qf}\right), \tag{4.13}$$

$$w = \frac{\hbar\beta}{q\alpha_G}\sqrt{\frac{\Delta}{2m}}. \tag{4.14}$$

In the next section, this procedure will be used to calculate the tunnel barrier height and width of the control constriction at various values of source-drain bias.

4.4 CONTROL CONSTRICTION: TUNNEL BARRIER MODELING

In this section the tunneling model is applied to the transport measurements of the control constriction shown in Figure 4.4. The first step is to estimate α_G, which is the capacitive coupling of the depletion gate voltage (in this example the RQPC gate voltage) to the tunnel barrier. The simplest way to do this is shown in Figure 4.11, where the positive and negative slopes of the most distinct edges in the differential conductance plot are measured. Recall from Section 4.1 that the positive and negative slopes are equal to $C_{RQPC}/(C - C_S)$ and $-C_{RQPC}/C_S$, respectively. From Figure 4.11 and the two aforementioned expressions, it is found that $\alpha_{RQPC} \approx C_{RQPC}/C \approx 0.056 \pm 0.003$.

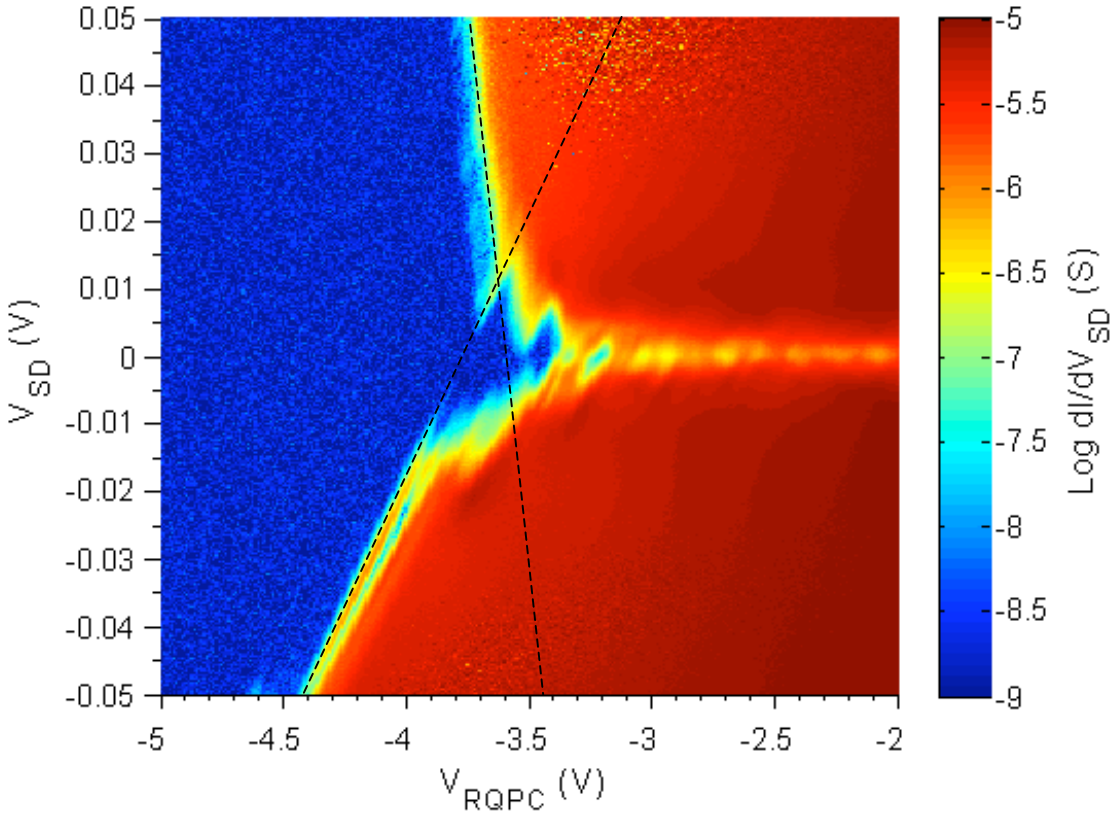


Figure 4.11 Estimating the capacitive coupling of V_{RQPC} to the tunnel barrier potential. The parameter α_{RQPC} is estimated by measuring the positive and negative slopes of the edges of the last resonance (black dashed lines) in the differential conductance plot.

Next the data in the differential conductance plot is integrated in MATLAB and a 2D plot of the dc current versus dc source-drain bias and RQPC gate voltage is obtained. This was shown in Figure 4.9. Then several line cuts at different values of source-drain bias are taken to produce the I-V_{RQPC} plots similar to Figure 4.10. The plots are in a semi-logarithmic scale and a line is fit to the region where the current increases exponentially with the RQPC gate voltage. The parameters I_0 and β are determined from these linear fits and are used to calculate the relative tunnel barrier height Δ and barrier width w from Equations 4.13 and 4.14. Table 4.1 shows the results of these calculations.

Table 4.1 Tunneling model results for the control constriction of sample 562.

V_{SD} (mV)	V_0 (V)	β (V^{-1})	I_0 (nA)	Δ (meV)	w (nm)
40	-3.69	39.97	2.44	2.9 ± 3.0	17.3 ± 4.0
30	-3.66	36.36	1.73	3.5 ± 3.0	17.2 ± 4.0
20	-3.62	25.33	2.05	4.8 ± 3.0	14.1 ± 4.0
15	-3.61	27.84	0.984	5.1 ± 3.0	15.9 ± 4.0
0[a]	-3.56	-	-	6.5 ± 3.0	13.6 ± 4.0
0[b]	-3.58	-	-	5.9 ± 3.0	11.5 ± 4.0
-20	-3.89	22.16	3.13	5.0 ± 3.0	12.5 ± 4.0
-30	-4.05	23.30	3.62	4.6 ± 3.0	12.6 ± 4.0
-40	-4.20	26.16	3.45	4.1 ± 3.0	13.4 ± 4.0

[a] Values at zero source-drain bias were determined by using the values at positive V_{SD} and performing a linear extrapolation to V_{SD} = 0 V.

[b] Values at zero source-drain bias were determined by using the values at negative V_{SD} and performing a linear extrapolation to V_{SD} = 0 V.

The error bars in Table 4.1 are determined from the uncertainties in the value of the capacitive coupling α_{RQPC} and the frequency constant f. The frequency values chosen were 0.1 THz, 1 THz, and 10 THz. The barrier heights and widths extrapolated from both positive and negative V_{SD} agree with each other to within about 10% and 17%, respectively.

The values of the tunnel barrier height Δ indicate a relatively deep potential well. The value of Δ can also be interpreted as the binding energy; that is the energy to lift an electron from its bound state so that it can just escape the potential well. Theoretical calculations show that a single isolated defect in the SiO_2 layer can bind an electron with

energies between 1 to 3 meV, depending on the distance of the defect from the Si-SiO_2 interface [31]. Two charge defects that are laterally close to each other can form a cluster, which can bind the electrons even more strongly. The binding energies are now about 6 to 9 meV, depending on the distance of the cluster of defects from the Si- SiO_2 interface and the lateral separation. It is possible that in the example considered above for the control constriction a combination of charge defects in the SiO_2 layer have amalgamated into a cluster, which would lead to a larger binding energy. This also corresponds well to Figure 4.5 that shows a number of resonances in the line cut of the differential conductance at zero source-drain bias. Each defect can trap at least one or possibly two electrons, which would lead to at least one defect-related resonance. Thus the high number of resonances may indicate a high number of defects in the constriction. Moreover, the resonances do not have the same capacitances consistent with many different charge centers rather than a single quantum dot with many transitions.

In the next chapter, the rectangular barrier model is used to characterize the tunnel barriers of the Sb-implanted constrictions.

CHAPTER 5: THE IMPLANTED CONSTRICTIONS

In this chapter transport measurements of the Sb-implanted constrictions are presented. We recall from previous chapters that the antimony donor atoms are implanted between the TP and CP poly-silicon gates and between the L and LQPC poly-silicon gates (left constriction). The tunneling model presented in the previous chapter is applied to these measurements and is used to characterize the tunnel barrier heights and widths of the constrictions. The results of the model for the implanted constrictions are compared to those for the control case. Finally, the results of the tunneling model are compared with capacitance modeling.

5.1 TP/CP CONSTRICTION: MEASUREMENTS AND MODELING

We first consider the TP/CP constriction. In this measurement the L, LP, RP, and R gates are biased positively into inversion so that there is unrestricted electron transport under these gates and these constrictions are open. This ensures that the only constriction formed is between the TP and CP gates where the donors were implanted.

Figure 5.1 shows a plot of the differential conductance of the TP/CP constriction of sample 561 as a function of the dc source-drain voltage and the CP gate voltage. The ac excitation from the lock-in was a 37 Hz 100 μV signal. The aluminum top gate was V_{AG} = +5.7 V, the TP gate was V_{TP} = -3.0 V, the R and L gates were $V_R = V_L$ = +2.0 V, and the RP and LP gates were $V_{RP} = V_{LP}$ = +1.5 V. All the other gates were grounded. There is a faint resonance at about V_{CP} = -1.6 V. This resonance is due to tunneling through some unknown charge center (for example a defect or donor). One important quality to note is that there are two separate regions where the current turns on. The edges of the resonance, delineated by the black dashed lines in Figure 5.1, represent the first turn-on

region. A second turn-on region, delineated by the red dash-dotted lines in Figure 5.1, is seen at more positive CP voltage. In contrast, there is only one prevalent turn-on in the differential conductance plot of the control constriction at $V_{SD} > q/C$ presented in the previous chapter. The two edges at voltages above the blockading energy are consistent with conduction through two different resonant centers, for example, the primary lithographically formed tunnel barrier combined with a donor or defect center.

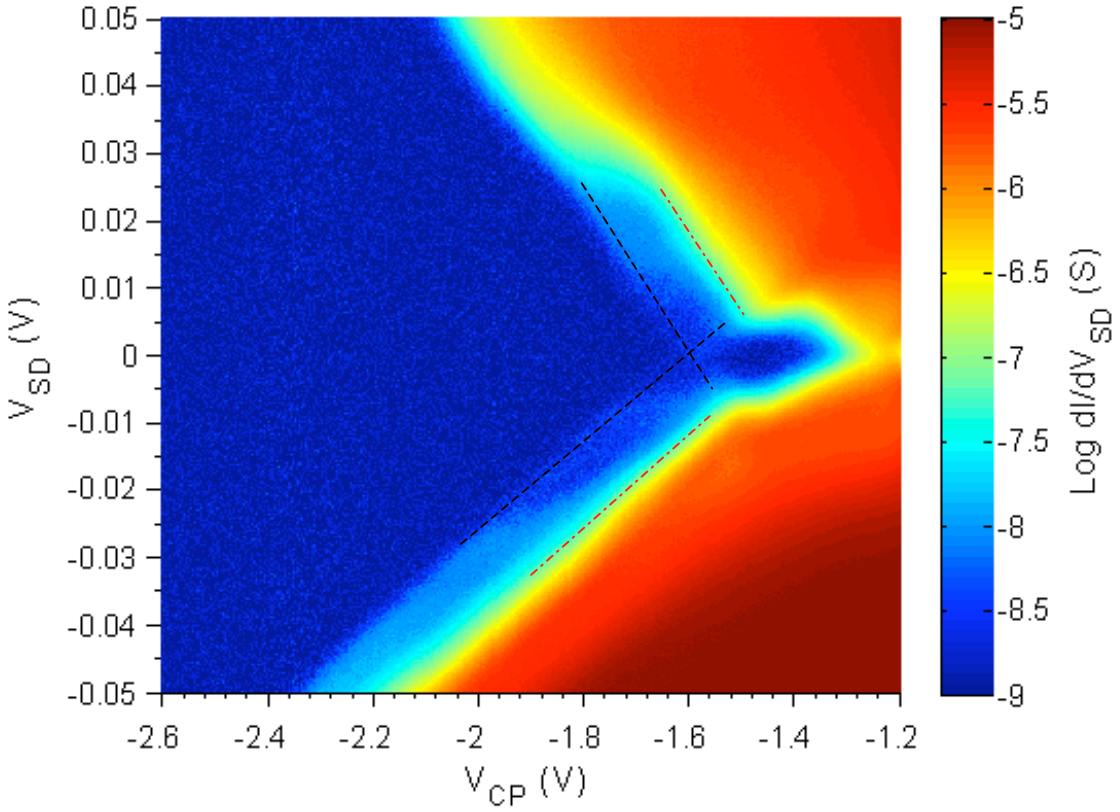


Figure 5.1 Transport through the TP/CP constriction of sample 561. The plot shows the differential conductance as a function of dc source-drain bias and CP gate voltage. The voltages on the remaining gates were V_{AG} = 5.7 V, V_{TP} = -3.0 V, $V_R = V_L$ = 2.0 V, $V_{RP} = V_{LP}$ = 1.5 V. A faint resonance, which is probably due to tunneling through a charge center, is seen at approximately V_{CP} = -1.6 V. The black dashed lined represent the first turn-on region. The red dash-dotted lines at higher CP voltage represent the second turn-on region.

The tunnel barrier of the resonance can be characterized by using the tunneling model. The same procedure described in Chapter 4 is used to determine the tunnel barrier height and width. First the capacitive coupling of V_{CP} to the tunnel barrier potential is estimated by measuring the positive and negative slopes of the edges of the resonance in the differential conductance plot, which are delineated by the black-dashed lines in Figure 5.1. The positive-going slope and the negative-going slope are equal to $C_{CP}/(C - C_S)$ and $-C_{CP}/C_S$, respectively. Thus the capacitive coupling of V_{CP} to the tunnel barrier potential is $\alpha_{CP} \approx C_{CP}/C \approx 0.042 \pm 0.003$.

Next the differential conductance plot in Figure 5.1 is numerically integrated in MATLAB. Figure 5.2 shows the resulting plot of dc current versus dc source-drain bias and CP gate voltage. Single line traces at constant values of dc source-drain bias are taken from this plot. An example is shown in Figure 5.3 where the current is plotted versus CP gate voltage for V_{SD} = 15 mV in a semi-logarithmic scale. As noted before, there are two separate regions where the current turns-on exponentially, which can be seen in Figure 5.3. The exponential turn-on at more negative CP voltage corresponds to the resonance; hence lines are fit to this region and the parameters I_0 and β are obtained from these linear fits. The results of these calculations are shown in Table 5.1.

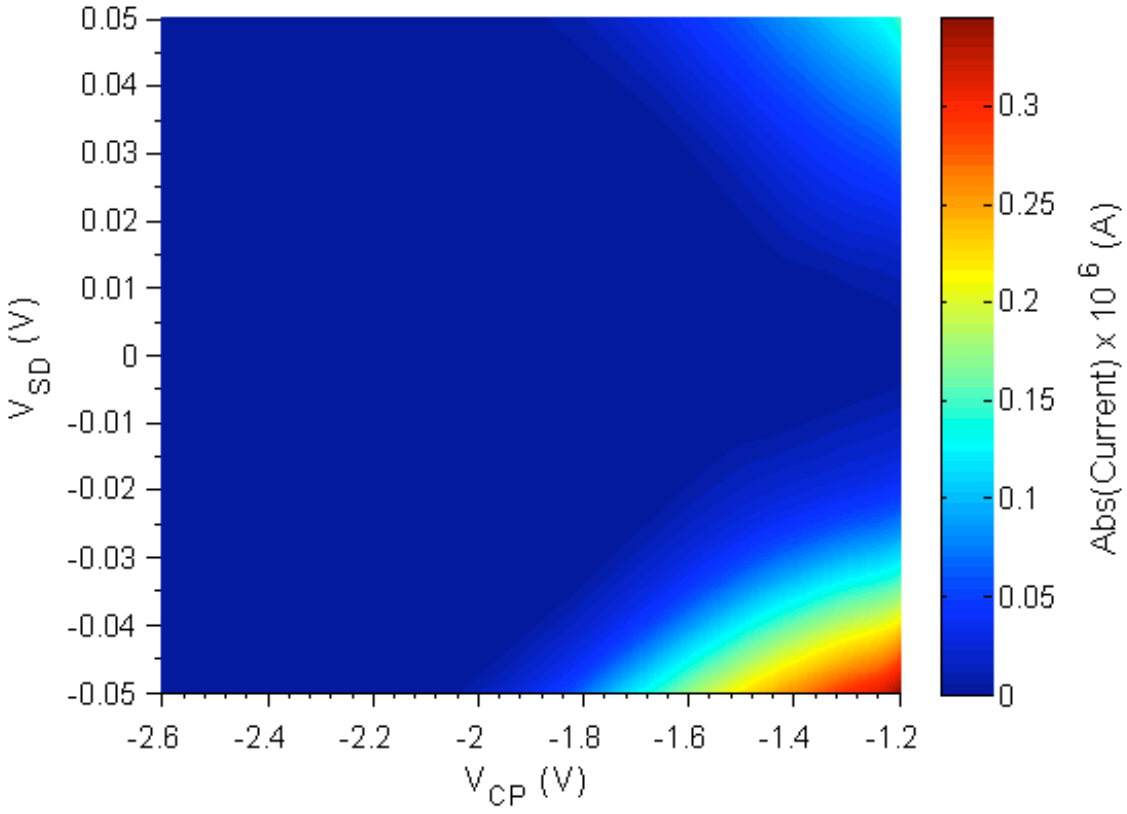


Figure 5.2 Magnitude of the dc current through the TP/CP constriction of sample 561 as a function of dc source-drain bias and CP gate voltage. The plot was obtained by taking the numerical integral of the data in Figure 5.1 using MATLAB.

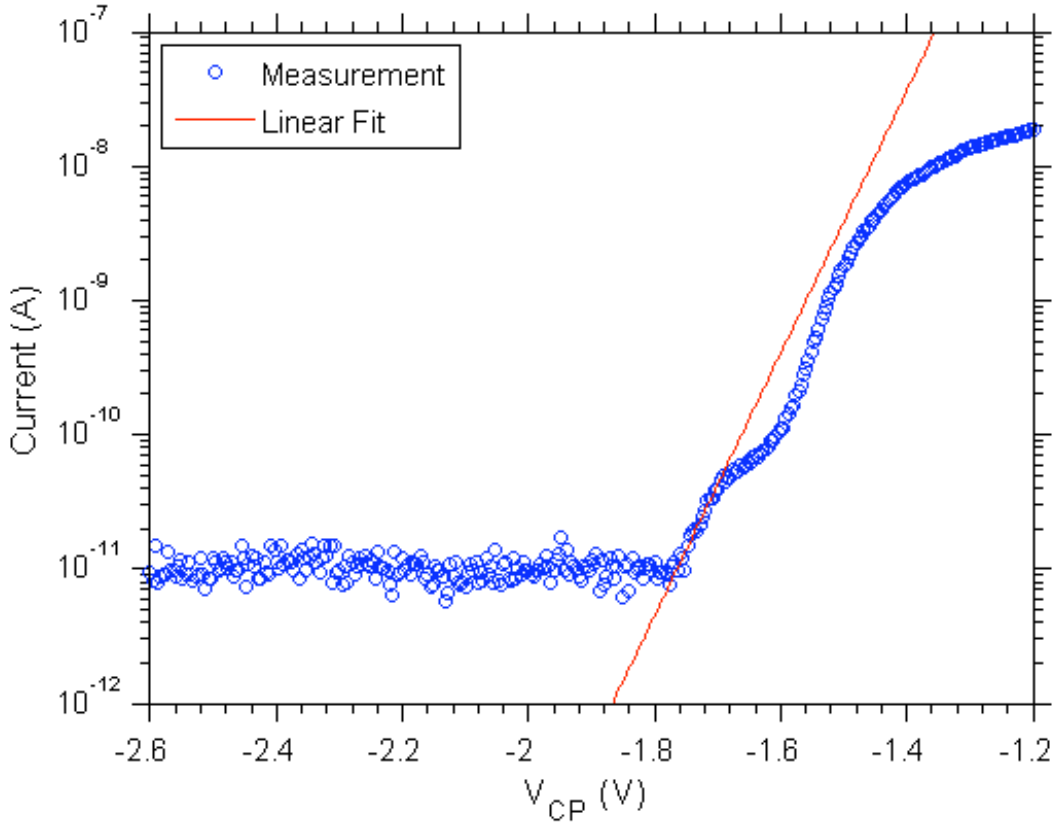


Figure 5.3 Current through the TP/CP constriction as a function of the CP gate voltage for V_{SD} = 15 mV (plotted in a semi-logarithmic scale). The plot was obtained by taking a line cut from Figure 5.2. Two exponential turn-on regions are seen; the turn-on at more negative CP voltage corresponds to the resonance. The red line is a linear fit used to extract the tunnel barrier height and width.

Table 5.1 Tunneling model results for the TP/CP constriction of sample 561.

V_{SD} (mV)	V_0 (V)	β (V^{-1})	I_0 (pA)	Δ (meV)	w (nm)
15	-1.720	22.39	27.5	8.1 ± 3.0	21.6 ± 4.0
10	-1.668	16.96	20.9	11.1 ± 3.0	19.1 ± 4.0
5	-1.616	14.36	13.8	13.7 ± 3.0	17.9 ± 4.0
0[a]	-1.560	-	-	16.6 ± 3.0	15.8 ± 4.0
0[b]	-1.500	-	-	16.3 ± 3.0	17.7 ± 4.0
-5	-1.620	12.18	10.2	16.7 ± 3.0	16.8 ± 4.0
-10	-1.740	11.43	14.8	17.1 ± 3.0	15.9 ± 4.0

[a] Values at zero source-drain bias were determined by using the values at positive V_{SD} and performing a linear extrapolation to $V_{SD} = 0$ V.

[b] Values at zero source-drain bias were determined by using the values at negative V_{SD} and performing a linear extrapolation to $V_{SD} = 0$ V.

The error bars in Table 5.1 are determined from the uncertainties in the value of the capacitive coupling α_{CP} and the frequency constant f. The frequency values chosen were 0.1 THz, 1 THz, and 10 THz. The barrier heights and widths extrapolated from both positive and negative V_{SD} agree with each other to within about 2% and 11%, respectively. The tunnel barrier height for the resonance in the TP/CP constriction is about 10 meV greater than the resonance in the control constriction, while the tunnel barrier widths are about the same.

It is known that the binding energy of the first electron, known as the D^0 state, for antimony in bulk silicon is around 43 meV [32]. The tunneling model fit indicates a binding energy of about 16 meV at $V_{SD} = 0$ V, which does not match with the bulk value of approximately 43 meV.

Measurements and modeling of transport through donors near the surface and in the presence of high vertical electric fields show D^0 to D^- charging energies smaller than the bulk energy difference [19]. Two mechanisms can lead to a charging energy smaller than the bulk value: the contribution of capacitances to gates near the surface [40] and hybridization of the wavefunction with a surface state [41]. In the Lansbergen study [19], a range of arsenic binding energies from 52 meV to 29 meV were found for a random scattering of donor positions near the surface, indicating that at least a 13 meV reduction in charging energy can be observed for a Bohr radius resonant center near the surface with gate electrodes being present. The decrease in charging energy is dominated by a reduced binding energy of the D^0 state, which would correspond to a smaller barrier height than an ideal bulk case. The observed 16-17 meV barrier height might, therefore, be explained as a D^0 transition in a donor.

Binding energies from potential wells produced by charge defects in the gate oxide, in contrast, are predicted to be less than ~ 10 meV for defect densities measured in devices processed similarly to the devices presented in this work [31]. Electron spin resonance (ESR) measurements of shallow trap depths and density of states has shown that the Sandia devices do have traps but the energies are shallow, much smaller than 16 meV [42]. The fixed charge and interface trap densities for a process flow that used reoxidation, similar to this case, were measured and found to be similar to pre-implant defect densities (see Table 2.3) [23].

These results are suggestive that transport through a single donor has been observed. Subsequent spin readout measurements on this sample by other researchers have also shown evidence of very long spin relaxation times T_1 (i.e., $T_1 > 1$ s), a strong

indicator that a donor spin is being read-out [17]. To prove unambiguously that the transport is through a donor, however, is challenging. Electron and nuclear spin resonance on a single donor has recently been demonstrated for a phosphorus donor, which appears to be the first definitive evidence that a single donor spin has been accessed and coherently manipulated. In particular the nuclear magnetic resonance (NMR) resonant frequency can be used as a chemical fingerprint. However, the necessary experimental setup and time required to implement such a measurement are well beyond the scope of this thesis.

5.2 LEFT CONSTRICTION: MEASUREMENTS AND MODELING

Next consider the left constriction, which consists of the LQPC and L poly-silicon depletion gates. Recall that the left constriction is essentially the mirror image of the control or right constriction except that the left constriction is implanted with antimony donor atoms.

Figure 5.4 shows a plot of the differential conductance of the left constriction of sample 562 as a function of the dc source-drain voltage and the LQPC gate voltage. The ac excitation from the lock-in was a 107 Hz 100 μV signal. The aluminum top gate was V_{AG} = +2.2 V and the L gate was V_L = -0.5 V. All the other gates were grounded. There are a few resonances seen at low dc source-drain bias. Qualitatively, the stability diagram of the left constriction looks more similar to the stability diagram of the control constriction (Figure 4.4) than the TP/CP constriction (Figure 5.1). In particular, there seems to be only one exponential turn-on region, similar to control constriction, rather than two separate exponential turn-on regions that were seen in the TP/CP constriction. In

fact, most of the left constrictions measured in this study more closely resembled the control constriction rather than the implanted TP/CP constriction.

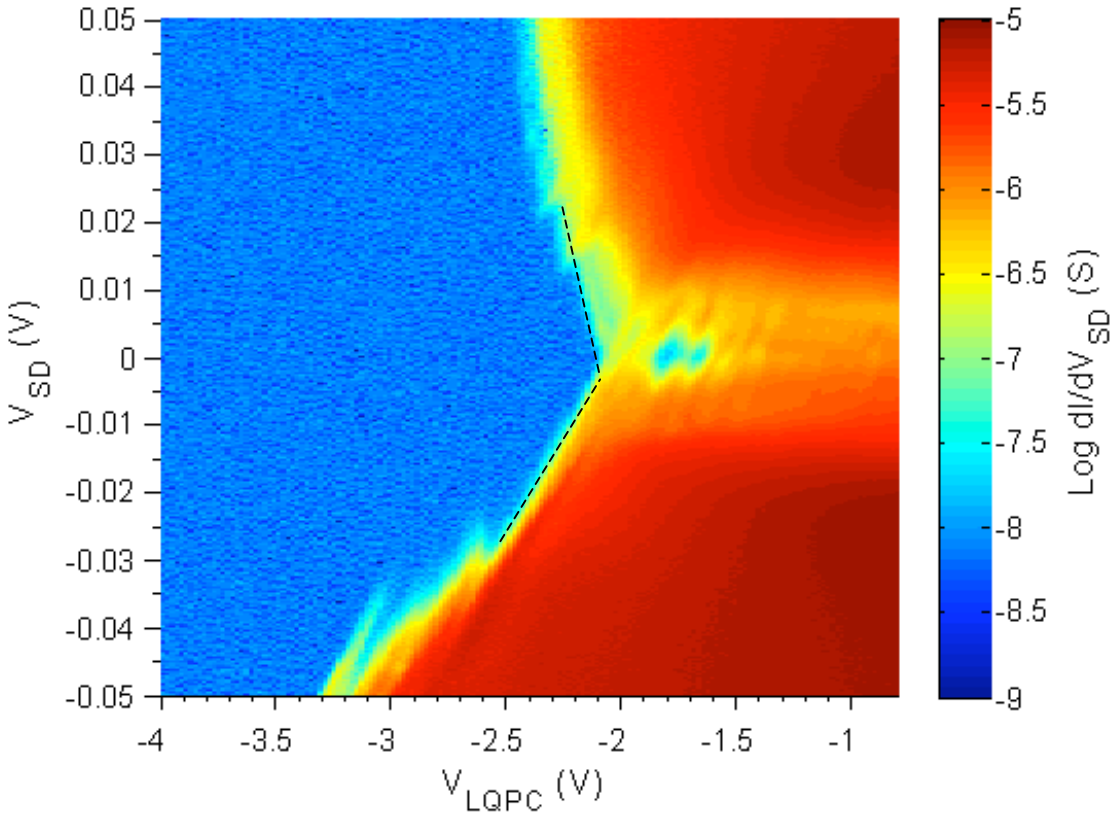


Figure 5.4 Transport through the left constriction of sample 562. The plot shows the differential conductance as a function of dc source-drain bias and LQPC gate voltage. The voltages on the remaining gates were V_{AG} = 2.2 V and V_L = -0.5 V. A few resonances are seen at low source-drain voltages, but it is not clear that these resonances are due to the implanted donors. This plot looks similar to the stability diagram of control constriction. The black dashed lines are used to estimate the capacitive coupling of V_{LQPC} to the tunnel barrier potential.

The tunneling model can be used to estimate the tunnel barrier height and width of the left constriction. The positive and negative slopes of the edges of the last resonance in the differential conductance plot, which are delineated by the black-dashed lines in Figure 5.4, are equal to $C_{LQPC}/(C - C_S)$ and $-C_{LQPC}/C_S$, respectively. This gives a

capacitive coupling of V_{LQPC} to the tunnel barrier potential of about $\alpha_{LQPC} \approx C_{LQPC}/C \approx 0.045 \pm 0.006$. Figure 5.5 shows the plot of dc current versus dc source-drain bias and LQPC gate voltage, which was obtained by numerically integrating the data in Figure 5.4. A single line trace at $V_{SD} = -15$ mV is shown in Figure 5.6 where the current is plotted versus LQPC gate voltage in a semi-logarithmic scale. The results of the model are shown in Table 5.2.

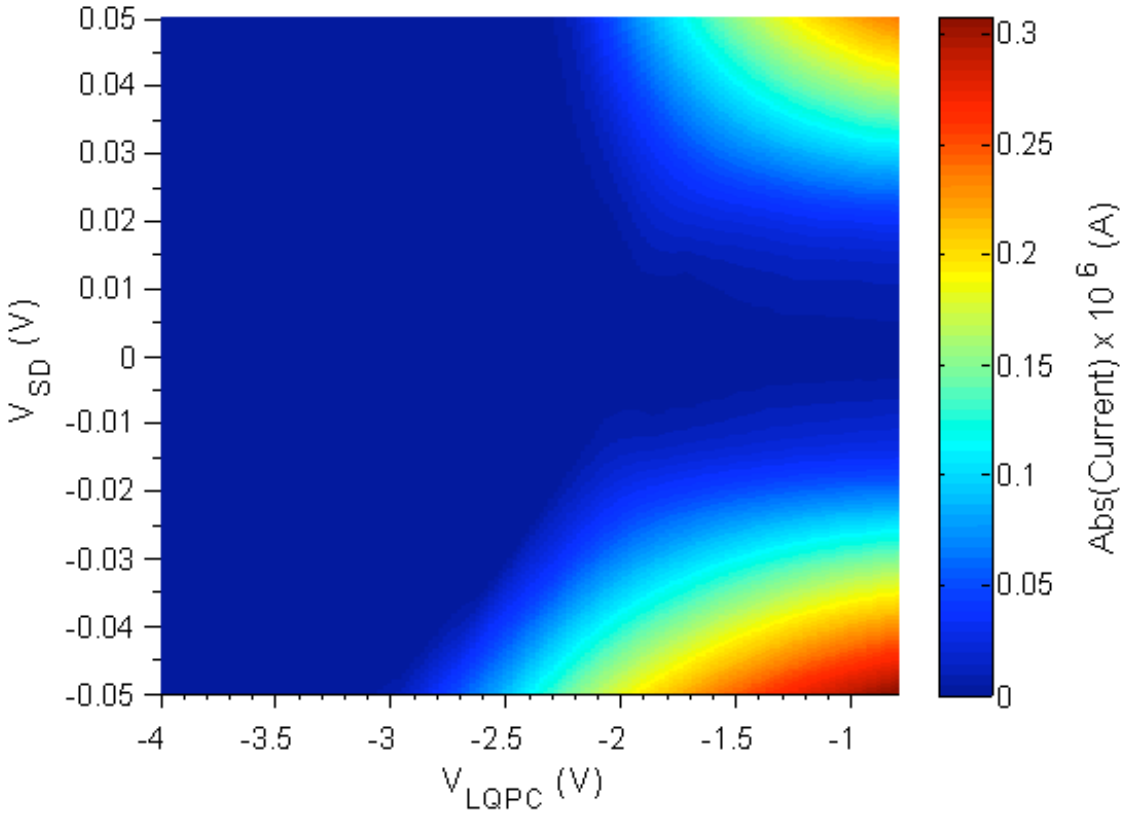


Figure 5.5 Magnitude of the dc current through the left constriction of sample 562 as a function of dc source-drain bias and LQPC gate voltage. The plot was obtained by taking the numerical integral of the data in Figure 5.4 using MATLAB.

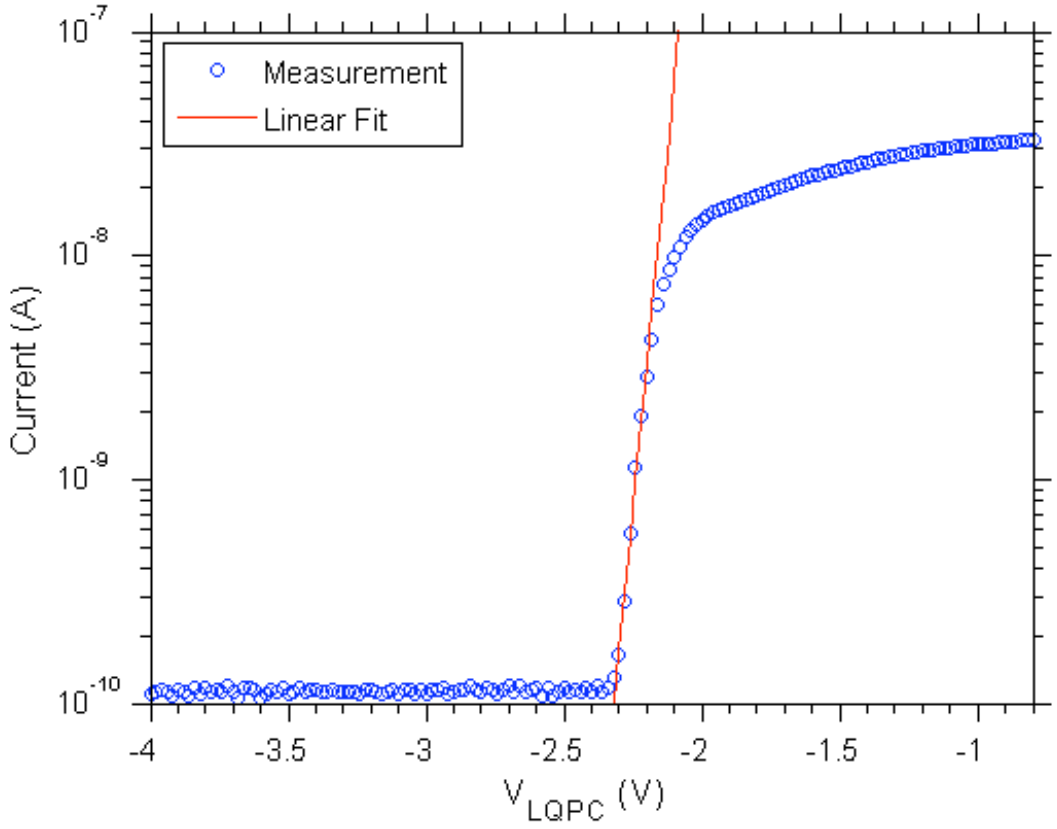


Figure 5.6 Current through the left constriction as a function of the LQPC gate voltage for V_{SD} = -15 mV (plotted in a semi-logarithmic scale). The plot was obtained by taking a line cut from Figure 5.5. The red line is a linear fit used to extract the tunnel barrier height and width.

Table 5.2 Tunneling model results for the left constriction of sample 562.

V_{SD} (mV)	V_0 (V)	β (V^{-1})	I_0 (pA)	Δ (meV)	w (nm)
20	-2.22	18.84	760	6.4 ± 2.5	15.0 ± 5.0
15	-2.16	19.75	504	6.6 ± 2.5	15.9 ± 5.0
10	-2.12	26.18	489	5.0 ± 2.5	18.4 ± 5.0
5	-2.10	29.59	208	5.1 ± 2.5	21.0 ± 5.0
0[a]	-2.05	-	-	4.4 ± 2.5	22.7 ± 5.0
0[b]	-2.02	-	-	3.0 ± 2.5	23.9 ± 5.0
-5	-2.10	43.08	566	2.9 ± 2.5	23.3 ± 5.0
-10	-2.18	32.97	452	4.0 ± 2.5	20.8 ± 5.0
-15	-2.26	29.45	579	4.3 ± 2.5	19.2 ± 5.0
-20	-2.34	31.32	710	3.9 ± 2.5	19.5 ± 5.0

[a] Values at zero source-drain bias were determined by using the values at positive V_{SD} and performing a linear extrapolation to $V_{SD} = 0$ V.

[b] Values at zero source-drain bias were determined by using the values at negative V_{SD} and performing a linear extrapolation to $V_{SD} = 0$ V.

The error bars in Table 5.2 are determined from the uncertainties in the value of the capacitive coupling α_{LQPC} and the frequency constant f. The frequency values chosen were 0.1 THz, 1 THz, and 10 THz. The barrier heights and widths extrapolated from both positive and negative V_{SD} agree with each other to within about 38% and 5%, respectively.

The values of Δ and w are closer to those of the control constriction than the TP/CP constriction. This supports the previous statement that the left constriction is more similar to the control constriction. One hypothesis for explaining this phenomenon is that the tunnel barrier is not forming in the region where the donors were implanted because

of the shape and geometry of the L poly-silicon gate. It is believed that the L gate pushes the tunnel barrier closer to the QPC gate.

5.3 COMPARISION TO CAPACITANCE TRIANGUALTION

In this section, the tunneling model is used to fit measurements of a different sample, sample 438, which was measured and characterized extensively by previous researchers. The data from this sample is revisited because one of the results from the previous work was that resonances were triangulated using a capacitance modeling approach. All relevant capacitances were measured and, from these geometry dependent parameters, the position of the resonant center was determined. A comparison of the tunnel barrier width extracted from the tunneling model can therefore be compared to the position extracted from the capacitances. The structure of the rest of this chapter is that the results of the capacitance modeling will be reviewed. Then the transport data of sample 438 is analyzed using the tunneling model and compared.

The fabrication, measurements, and capacitance modeling of sample 438 were presented and thoroughly analyzed in reference 23. The fabrication process of sample 438 is similar to the one described in Chapter 2; however, there are several differences between sample 438 and the previous devices including a different poly-silicon depletion gate pattern, antimony implantation energy, and dose (100 keV with a dose of 4×10^{11} cm^{-2}). The dose and energy correspond to an average of 8 Sb donor ions in the implanted constrictions at a depth of 10 nm below the Si/SiO_2 interface. Figure 5.7 shows an SEM image of the poly-silicon depletion gate layout of sample 438 before secondary dielectric and top aluminum gate deposition.

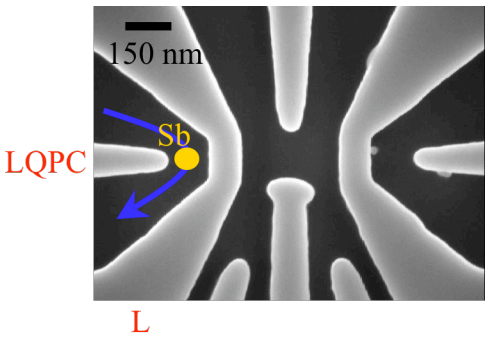


Figure 5.7 SEM image of the poly-silicon depletion gate layout of sample 438. Transport is measured through the left point contact where antimony donor atoms have been implanted. Image is from reference 23.

Figure 5.8 shows a plot of the differential conductance of the left constriction of sample 438 as a function of the dc source-drain voltage and the LPOLY voltage. The LPOLY voltage is the combined voltage of gates L and LQPC; that is to say that these gates are connected to the same voltage supply. The ac excitation from the lock-in was a 27 Hz 100 μV signal. The aluminum top gate was V_{AG} = +18 V. Sample 438 was measured in a dilution refrigerator at a temperature of 20 mK. Two sub-threshold resonances, labeled A and B, are seen in the stability diagram of Figure 5.8. These resonances are due to tunneling through charge centers located within the tunnel barrier and capacitance modeling is used to triangulate the position of these charge centers.

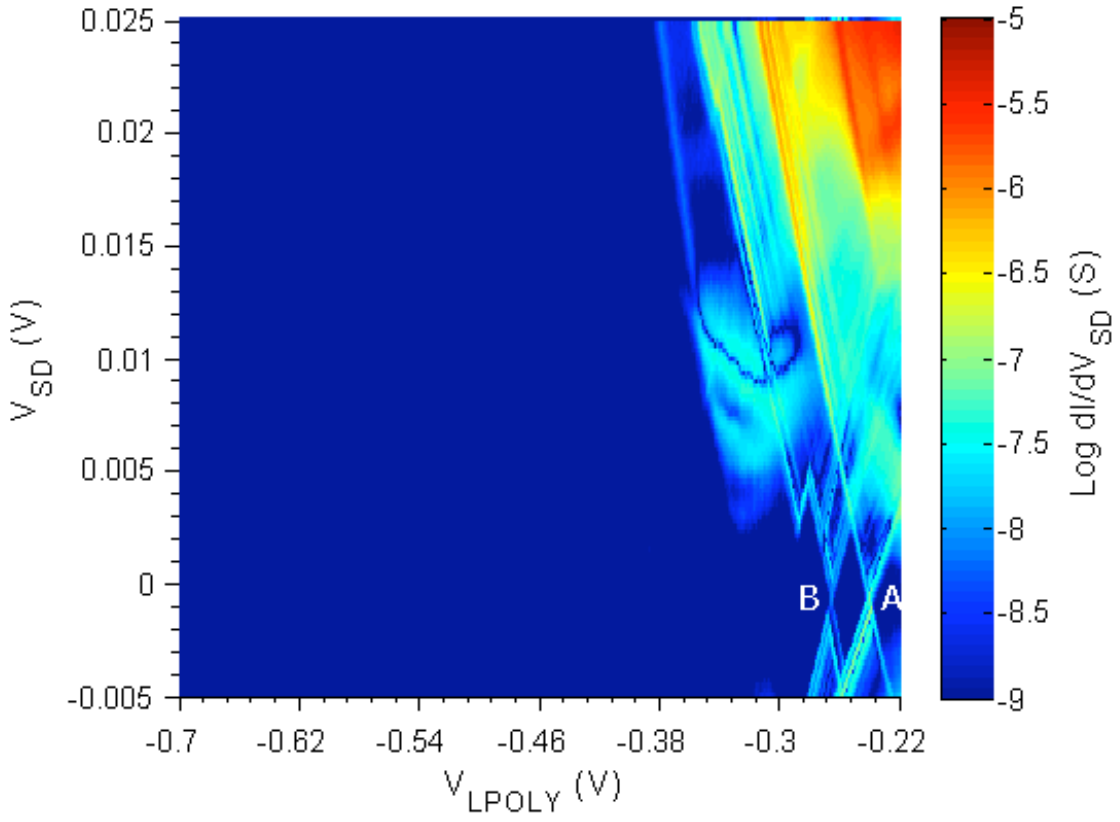


Figure 5.8 Transport through the left constriction of sample 438. The plot shows the differential conductance as a function of dc source-drain bias and LPOLY voltage at a temperature of 20 mK. The aluminum top gate voltage was V_{AG} = 18 V. Two sub-threshold resonances, labeled A and B, are seen in the stability diagram. The data is from the work done in reference 23.

It is already known from Figure 4.2(d) that the positive and negative slopes of the edges of the resonances are equal to $C_G/(C - C_S)$ and $-C_G/C_S$ (assuming the drain 2DEG is grounded), respectively. A set of capacitance ratios can be obtained for each resonance by performing measurements similar to Figure 5.8 for each gate (L, LQPC, and top aluminum gate) and by changing which 2DEG region is held at ground potential. Performing this set of measurements yields the following ratios of capacitances for each resonance: C_S/C, C_D/C, C_{LQPC}/C, C_L/C, and C_{AG}/C. The measured capacitance ratios bound the possible locations of the charge centers through the geometric dependence of

capacitance to position. To calculate the capacitances, the poly-silicon gates, aluminum top gate, and source/drain 2DEGs are modeled as perfect conductors and the charge centers are modeled as 1.8 nm radius spheres, which is approximately the radius of the first bound electron on antimony in bulk silicon (i.e., the Bohr radius in silicon). The capacitances between these conductors are calculated and through trial and error an optimal position for each resonance is found that is a good match to the measured capacitance ratios.

The schematic diagram in Figure 5.9 shows the results of capacitance triangulation for resonances A and B. The figure shows that the best-fit locations for A and B are under the QPC poly gate, which is an unlikely position for the intentionally implanted Sb donors because the poly-silicon extends 200 nm further masking this region. Diffusion lengths for this thermal budget are small compared to the implantation window, assuming literature values for antimony diffusivity under thermal equilibrium conditions. Charge defects in the SiO_2 layer are a possible source of the confining potentials for resonances A and B. The figure shows that the resonances are located close to the mid-point between the source/drain 2DEGs and that the total tunnel barrier width is approximately 40-50 nm using the lithographic dimensions of the poly gate. The actual tunnel barrier width is likely bigger due to depletion of the 2DEG that extends beyond the lithographic edge. Gaps of approximately 60 nm are predicted if it is assumed that the edge of the 2DEG, for tunneling, is defined at a density of $\sim 10^{11}$ cm^{-2} [43].

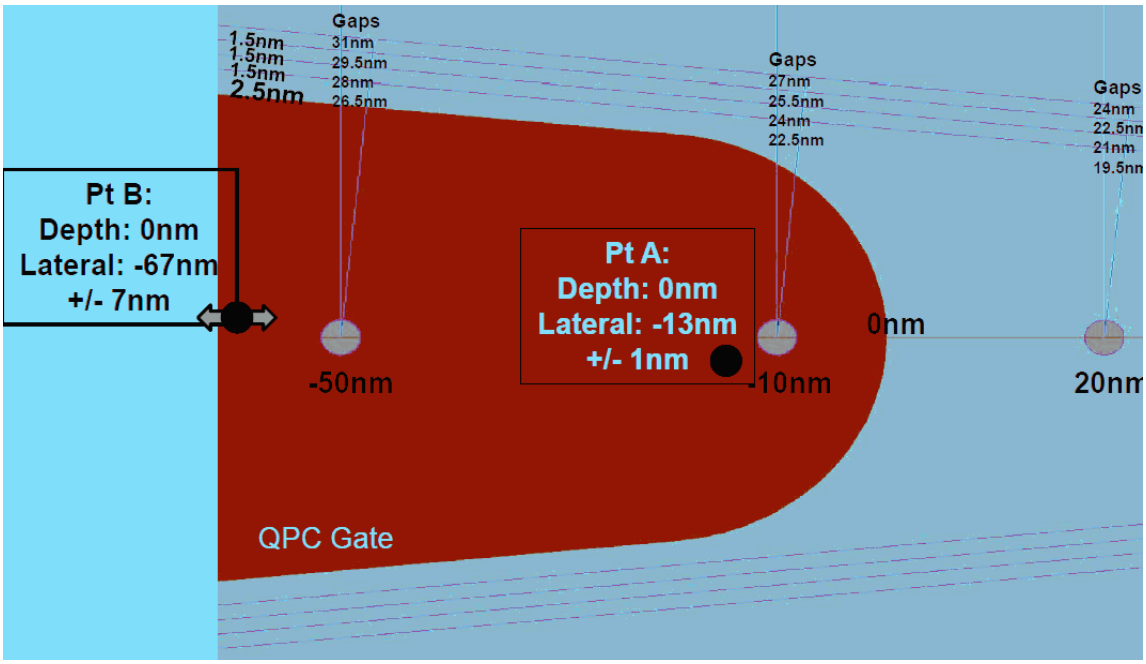


Figure 5.9 Results of capacitance modeling for resonances A and B. The diagram shows the locations of the resonances that are a good match to the measured capacitance ratios. The edge of the 2DEG is calculated using a semi-classical simulation of the electron density and assuming that the metallic edge starts at a density of ~10^{11} cm^{-2}. The figure is from the work done in reference 23.

Now the tunneling model will be used to estimate the tunnel barrier height and width of resonances A and B. In particular, the barrier width obtained from capacitance modeling is compared to that obtained from the tunneling model. The capacitive coupling of V_{LPOLY} to the tunnel barrier potential of resonance A and resonance B is approximated as $(\alpha_{LPOLY})_A \approx (C_{LPOLY}/C)_A \approx 0.12 \pm 0.01$ and $(\alpha_{LPOLY})_B \approx (C_{LPOLY}/C)_B \approx 0.17 \pm 0.03$, respectively. Figure 5.10 shows the plot of dc current versus dc source-drain bias and LPOLY voltage, which was obtained by numerically integrating the data in Figure 5.8. A line trace at $V_{SD} = 15$ mV is shown in Figure 5.11 where the current is plotted versus LPOLY voltage in a semi-logarithmic scale. The figure shows that there are three regions where the current turns on exponentially. The exponential turn-on regions that correspond to the same LPOLY voltage as the resonances in the stability diagram are associated with

that particular resonance. The results of the model are shown in Table 5.3 and Table 5.4 for resonance A and B respectively.

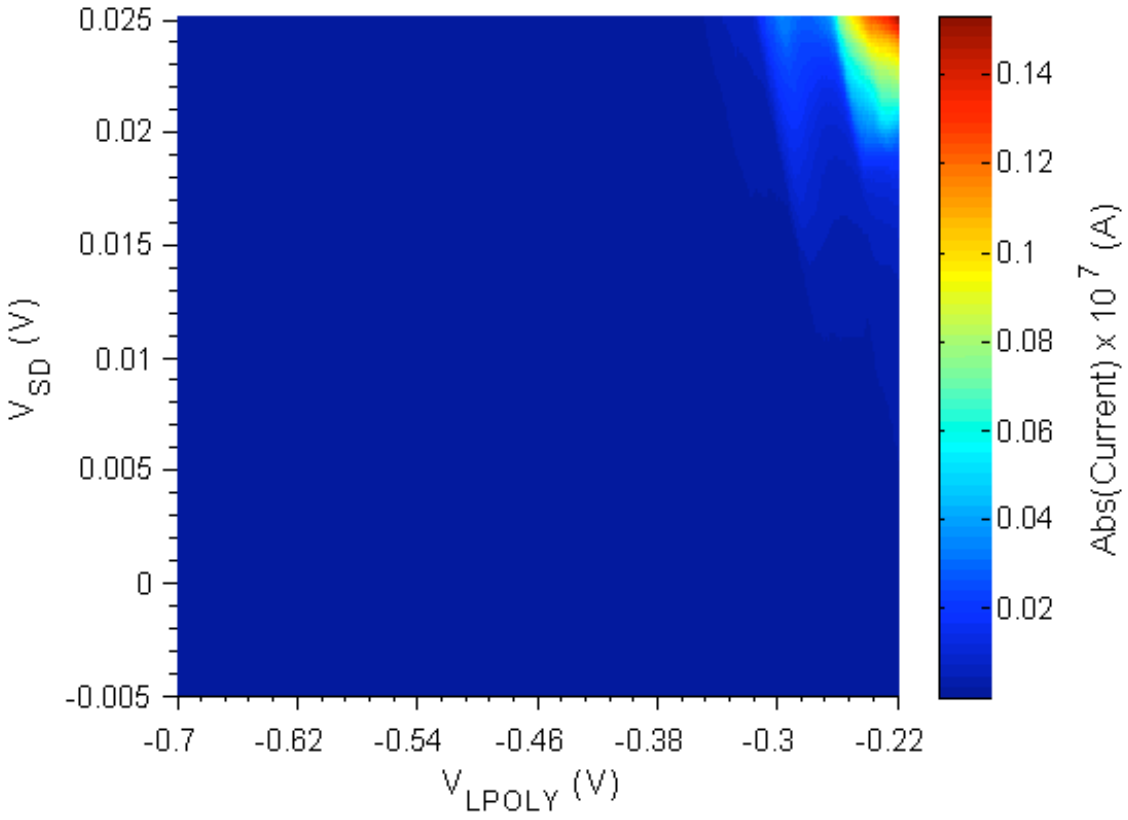


Figure 5.10 Magnitude of the dc current through the left constriction of sample 438 as a function of dc source-drain bias and LPOLY voltage. The plot was obtained by numerically integrating the data in Figure 5.8.

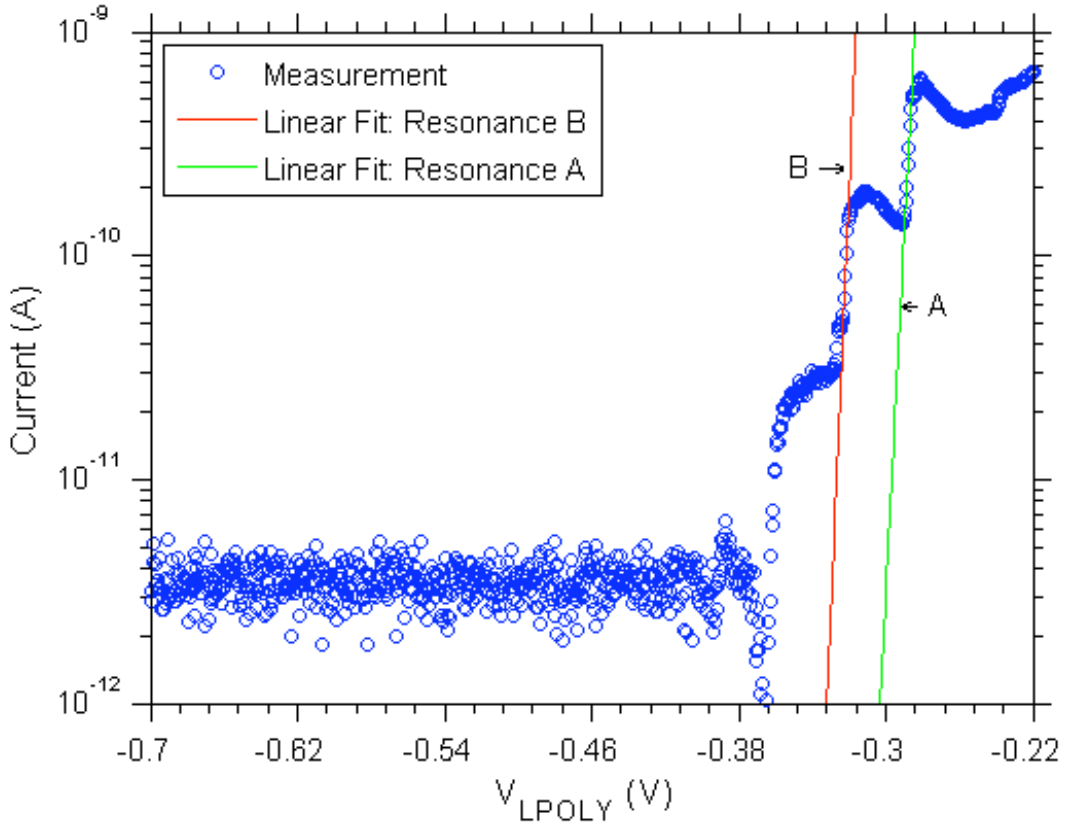


Figure 5.11 Current through the left constriction as a function of the LPOLY voltage for V_{SD} = 15 mV (plotted in a semi-logarithmic scale). The plot was obtained by taking a line cut from Figure 5.10. The resonances are associated with the exponential turn-on regions that occur at the same LPOLY voltage as in the stability plot. The linear fits are used to extract the tunnel barrier height and width.

Table 5.3 Tunneling model results for resonance A of sample 438.

V_{SD} (mV)	V_0 (V)	β (V^{-1})	I_0 (pA)	Δ (meV)	w (nm)
20	-0.3010	242.8	719	1.3 ± 0.7	33.2 ± 8.0
15	-0.2880	366.1	256	1.1 ± 0.7	44.4 ± 8.0
10	-0.2730	381.1	136	1.1 ± 0.7	47.5 ± 8.0
5	-0.2580	348.9	55.0	1.4 ± 0.7	48.3 ± 8.0

Table 5.4 Tunneling model results for resonance B of sample 438.

V_{SD} (mV)	V_0 (V)	β (V^{-1})	I_0 (pA)	Δ (meV)	w (nm)
20	-0.3375	397.4	75.9	1.6 ± 0.7	42.4 ± 10.0
15	-0.3220	435.6	81.3	1.5 ± 0.7	44.2 ± 10.0
5	-0.2960	374.4	5.89	2.3 ± 0.7	47.5 ± 10.0

The tunnel barrier height for both resonances is about 1-2 meV, which corresponds well to single isolated charge defects in the SiO_2 layer [31], consistent with the conclusion of Bishop et al., that the resonant tunneling was assisted by a defect under the poly gate.

The widths of the tunnel barriers, extracted from the fit, are approximately 48 nm at low V_{SD}. The gaps estimated from the semi-classical estimate are ~30 nm, assuming symmetric position of the resonant center and a metallic edge starting at a density of 10^{11} cm^{-2}.

There are several possible causes for disagreement between the tunneling fit and the capacitance triangulation. One inconsistency in the tunneling model when applied to small barriers and large V_{SD} is that the simple rectangular barrier approximation should breakdown. That is, the voltage drop across the junction varies between 5 to 20 mV. Assuming that the voltage drop across the junction is 20 mV, then the voltage drop across a single tunnel barrier is approximately 10 meV. But the barrier heights calculated using the model are only about 1-2 meV. Therefore the tunnel barriers are probably more triangular and the rectangular barrier approximation is most likely a bad approximation in this case. A second source of uncertainty is the width of the tunnel barrier predicted by

the triangulation, because the edge of the 2DEG is not well established. A third source of uncertainty is the details about the resonance position relative to the mid-point and the size of the resonance. The largest barrier will dominate the tunneling and the capacitance triangulation only indicates a range of possible positions around the mid-point, perhaps as much as 10% deviation. Lastly, the size of the resonance has a non-zero radius, which should also be considered although the size of the resonance will qualitatively reduce the gap extracted from the capacitance modeling thereby making the disagreement larger. At this time, given the uncertainties, no conclusions are made about this comparison.

CHAPTER 6: SUMMARY AND OUTLOOK

6.1 SUMMARY

In this thesis we measure tunneling conductance through a voltage tunable barrier in silicon at T ~ 4 K and test a model for tunneling that accurately estimates the conductance over a wide range of voltages. The tunneling model was conjectured in earlier work for a specific case but its accuracy has not been tested over a wide regime of cases. In this thesis, many tunnel barriers are measured and examined using the tunnel barrier model. The specific tunnel barrier geometry is formed from a split gate nanostructure, commonly used as a starting element to form lateral quantum dots (i.e., this is a common tunnel barrier geometry). The tunneling behavior is found to agree well with a voltage dependent barrier height that depends linearly over a wide range of voltages. The linear dependence can be described with a capacitance model and two fitting parameters: barrier width and barrier height.

The good agreement between the tunneling model and experiment introduces several implications including: (a) a better quantitative understanding of the physical dependence of the barrier height on voltage in the split gate geometry, (b) an experimental method to extract an effective barrier height and width (for relative comparison between devices with, for example, different processing), (c) a way to extrapolate the barrier height in regimes where current is too small to measure (i.e., high resistance regime of the barrier), and (d) a foundation for a compact model of tunnel barriers in quantum dot systems.

Tunneling resonances can be caused by a number of underlying physical mechanisms, for example, defects or intentionally introduced resonant centers such as

implanted donors. This thesis furthermore studies an application of the tunneling model as an approach to distinguish between resonances that are low or high probability donor candidates in contrast with defects. Study of transport through single donors is of interest for transistor characterization in the regime of few dopant implants for threshold adjustment, for example, as well as beyond Moore's law paths such as quantum computing. In this particular application, high barrier heights are indicative of donors in contrast with low binding energies anticipated for many types of defects near the conduction band edge. Transport through a number of non-implanted and implanted constrictions is discussed. Examples of candidates for defect resonances as well as a donor resonance are highlighted.

The model was also applied to tunnel barriers for which extensive capacitance modeling was already completed. Two charge centers, probably due to charge defects near the Si/SiO_2 interface, were found from capacitance modeling. The tunneling model found barrier heights that were consistent with single isolated charge defects, but the barrier widths predicted by the tunneling model were greater than those predicted by capacitance modeling. This may be due to the simple rectangular barrier approximation used in the tunneling model. More realistic tunnel barriers, such as triangular potential barriers, may possibly improve the accuracy of the model.

6.2 FUTURE OUTLOOK

One of the next major milestones for these donor devices is to successfully read-out the spin of an electron. Morello et al. recently demonstrated read-out of an electron spin in silicon [17]. The device structure consisted of single phosphorus donor atoms implanted into an intrinsic silicon substrate near a silicon single electron transistor (SET).

The SET is a nanoelectronic device consisting of a small island of electrons (a quantum dot) tunnel-coupled to source and drain reservoirs and electrostatically induced beneath a SiO_2 layer by an overlaying top aluminum gate. The donors are implanted close to the small island of electrons (approximately 30-60 nm) so that the donor and SET are both electrostatically coupled and tunnel-coupled.

Spin read-out is achieved through spin-dependent tunneling. An externally applied magnetic field splits the energy levels of the charge center into a spin-up and a spin-down state; the spin-up state has a higher energy than the spin-down state. The electrochemical potentials of the charge center and SET are tuned so that a spin-up electron from a nearby charge center can tunnel into the SET island, while the tunneling of a spin-down electron is blocked. The tunneling of a single electron onto the SET island causes a shift in the current through the SET, which allows one to determine the spin-state of the electron. This configuration is also capable of measuring the spin relaxation time T_1, i.e. the time for spin relaxation from a spin-up to a spin-down state. Such a measurement has been pursued with one of the devices measured in this thesis, sample 561, and a long T_1 has been measured, indicative of a donor instead of a defect, in the same constriction as a donor was indicated by the transport measurements and modeling from this thesis.

Another future goal is to be able to controllably couple and decouple two donor-bound electron spins, which stems from the donor-based quantum computing architecture proposed by Kane [12]. This requires precision and accuracy in the placement of single donors with spacing on the order of 20 nm, which is difficult to do with ion implantation processes because it requires verification of single ion arrival, while also limiting the

straggle. Straggle is a measure of the random displacement of the ion as it is stopped by the substrate. The straggle decreases with decreasing ion energy.

One way to establish control of single ion implantation is by integrating single ion detectors with future devices that will ensure the arrival of a single ion. Avalanche diode detectors operating in Geiger-mode have recently been demonstrated that are highly sensitive to low energy ions and single ion strikes that are remotely located from the detector [44,45]. Integration of these detectors with future single donor devices can thus provide a path for more precise and accurate placement of single donors.

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