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Spatio-temporal circuits for imaging sensors

Glauco Rogerio Cugler Fiorante

Glauco Rogerio Cugler Fiorante
Candidate

Electrical and Computer Engineering
Department

This dissertation is approved, and it is acceptable in quality and form for publication:

Approved by the Dissertation Committee:

Dr. Sanjay Krishna , Chairperson

Dr. Payman Zarkesh-Ha

Dr. Francisco Javier Ramirez Fernandez

Dr. Keith A. Lidke

Dr. Sang Han

SPATIO-TEMPORAL CIRCUITS FOR IMAGING SENSORS

by

GLAUCO ROGERIO CUGLER FIORANTE

B.S.,Electrical Engineering, Universidade Santa Cecilia, 1995
M.S.,Electrical Engineering, Universidade de São Paulo, 2004

DISSERTATION

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DEDICATION

Carmem Barduco Cugler Fiorante (in memoriam),

João Batista de Oliveira Fiorante,

Elaine Cristina Silva Cugler Fiorante, and

Nathaly Ann Silva Cugler Fiorante,

who, in addition to their long names,

had in common the sacrifice of

moving through life without a

husband, father, and son, at their side.

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ABSTRACT

The first and second generations of infrared detectors–developed from the 1950s to the 1990s–were dominated by single pixel, linear, and staring small format, containing from 1 Kpixels to 100 Kpixels. In the past decade, the third-generation systems presented (a) large format (1 Mpixels to 16 Mpixels), (b) higher operating temperature (200 K to 250 K for MWIR, and 120 K to150 K for LWIR), and (c) multicolor operation. The emphasis demanded for the next generation of devices is the incorporation of an enhanced functionality in the imagers–preferably at the pixel level–such as color, polarization, and dynamic range control, leading to a dramatic reduction in the size, complexity, and cost of infrared imaging systems.

In this work, a new 96 × 96 pixel, 30 μm pitch mixed-signal readout-integrated circuit (ROIC) with a pixel-level tunable bias control is demonstrated. The new ROIC is capable of providing a large-bias voltage in both polarities on each individual pixel, independently. These enhanced functionalities are achieved by modifying a capacitive transimpedance amplifier (CTIA) CMOS ROIC architecture. The unit cell electronic circuit was designed using 15 transistors and four capacitors and consists of the CTIA integrator–a two-stage, seven-transistor operational amplifier–one analog memory, one address selector, one reference recover switch, a sample-and-hold stage, an output buffer, and an output multiplex switch. Several test structures of individual devices and complete circuits were implemented on the test chip to characterize each one and to reconstruct the unit cell with discrete components, if necessary. Intending to test, characterize, and control the ITP-ROIC, an FPGA-based hardware and GUI software were developed to generate four analog and 26 digital output signals, with 87 adjustable parameters, and it contributes for the unit cell characterization setup, the FPA/ROIC system test, and for the development of an autonomous controller for a DWELL-based IR portable camera. In addition to the hardware, chip interconnection techniques were developed to grant nondestructive, flexible, quick interconnections for definition of new test setups. The test chip has been fabricated in TMSC 2P4M 0.35 μm high-voltage CMOS technology by MOSIS. With 250 kHz of pixel clock and 57 ms of integration time, the acquired image presents 10 FPS. The ITP-ROIC has a bias voltage range of +/-5 V and an output voltage swing of +/-3.9 V. The 74 fF integration capacitor presents a charge capacity of 370 fC– or 2.31 x 10^6 electrons–at 5 V.

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Chapter 1

Introduction

1.1. Electromagnetic radiation

The visible region of the electromagnetic spectrum is defined by the range of wavelength (λ) visible to the human eye, from 380 nm to 700 nm [2]. The correspondent electromagnetic frequency ($f = 1/\lambda$) ranges from 790 THz to 430 THz, and its energy (eV) ranges from 1.7 eV to 3.3 eV (Figure 1.1).

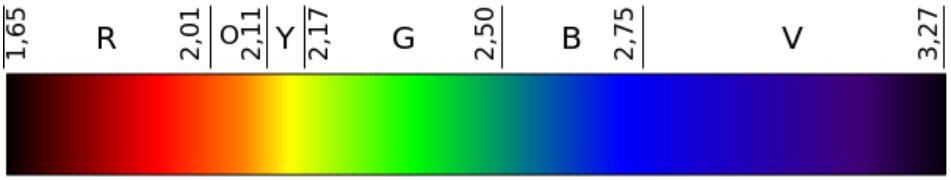


Figure 1.1. Energy of photons in the visible spectrum [3].

The infrared (IR) region of the electromagnetic spectrum presents several subdivision schemes commonly used for the IR region [4], such as from the International Commission on Illumination (CIE), the ISO 20473, and the astronomy division scheme [5]. The sensor-response division scheme divides the band based on the response of various detectors [6]:

- Near infrared (NIR): from 0.7 μm to 1.0 μm, from the approximate end of the response of the human eye to that of the silicon.
- Shortwave infrared (SWIR): 1.0 μm to 3 μm, from the cutoff of silicon to that of the MWIR atmospheric window. InGaAs covers to about 1.8 μm; the less sensitive lead salts cover this region.
- Midwave infrared (MWIR): 3 μm to 5 μm, defined by the atmospheric window

and covered by Indium antimonide [InSb] and HgCdTe and partially by lead selenide [PbSe].

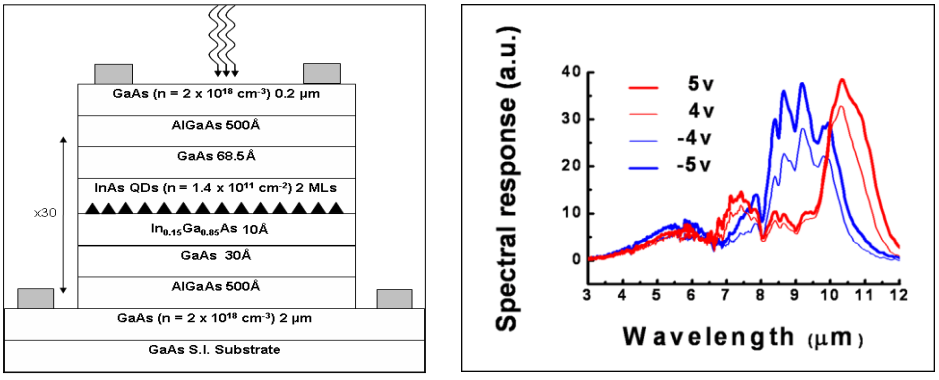
- Long-wave infrared (LWIR): 8 μm to 12 μm, or 7 μm to 14 μm, the atmospheric window covered by HgCdTe and microbolometers.
- Very-long wave infrared (VLWIR): 12 μm to approximately 30 μm, covered by doped silicon.
- Far infrared (FIR): more than 25 μm.

MWIR and LWIR bands of the spectrum present high importance for three main reasons. First: Most objects emit radiation in this wavelength range, thus IR sensors are effective in "seeing in the dark" and in this way are useful for applications in thermography for noninvasive medical imaging and in night vision imaging. Second: The majority of chemical species have spectral signatures in the IR regime due to fundamental absorption processes associated with vibrational states of the molecules, permitting applications such as pollution monitoring, gas leakage detection, and spectroscopy. Third: Terrestrial applications on MWIR and LWIR are very attractive due to the transmission window in the atmosphere [7].

1.2. DWELL

One possible technology for image acquisition on infrared bands of MWIR and LWIR is the quantum dots in a well (DWELL) device. Although DWELL detector is a motivation for the designed ROIC presented in this work, it is not the scope here to detail the DWELL development, functionality, fabrication, and characterization. However, a brief device description and principle of operation are presented:

"A DWELL detector is basically a hybrid of conventional quantum well (QW) and quantum dot (QD) detectors. In a representative DWELL heterostructure, InAs QDs are embedded in InGaAs–GaAs multiple QW structures and electrons in the ground state of QD are promoted to a set of bound states within the QW by photoexcitation. Altering the QW thickness of the DWELL detector alters the nature of the allowable energy transitions (bound-to-bound, bound-to-quasi-bound, and bound-to-continuum), thereby altering the DWELL's operating wavelengths. These energy transitions enable the detection of photons from MWIR to VLWIR within a single detector. Moreover, a bias-dependent spectral response is also observed in DWELL detectors due to the QCSE. The asymmetric geometry of the electronic potential, due to the shape of the dot and the different thicknesses of QW above and below the dot, results in variation of the local potential as a function of the applied bias. From these measurements, one can observe the multicolor capability of the DWELL detector structure." [8]. The DWELL-1781 structure was grown by molecular beam epitaxy (MBE) and fabricated using a standard lithography technique in a class 100 clean-room environment. The growth conditions of DWELL-1781 and its bias-dependent spectral response are shown in Figure 1.2 (b).



(a) (b)

Figure 1.2. Growth schematic (a) and bias-dependent spectral response at 30K (b) of DWELL-1781 [8].

1.3. Photodiode

To demonstrate the functionality of the new ITP-ROIC without the direct implementation of the DWELL-FPA, a CMOS-compatible photodiode structure needed to be chosen for implementation. A detailed comparative study of three photodiode structures in standard n-well CMOS process can be found in [9] but is summarized as follows:

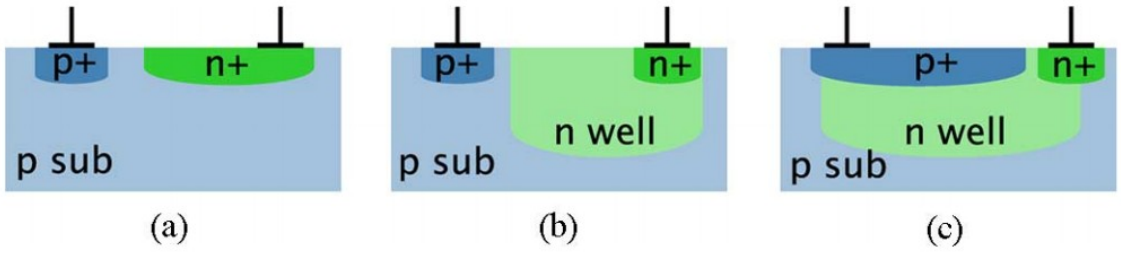


Figure 1.3. Schematic drawings of three CMOS photodiode structures [9].

Figure 1.3 (a) shows the most compact structure related to the design rules and the most straightforward structure used to make a photodiode. The n+/p-sub (or NP/Psub) is considered the reference design. The highly doped n+ region presents a small depletion-region width, which leads to low collection efficiency. Figure 1.3 (b) presents the lightly doped n-well diffusion to create a *pn* junction in the p substrate. This increases the depletion that, combined with the deeper junction, presents more efficiency at capturing long wavelength photons. Figure 1.3 (c) adds a p+ (or PP) implant covering the n-well diffusion, called "pinned" structure, that serves to create two *pn* junctions and two effective depletion regions larger than n-well/p-sub, intended to lead to the highest collection efficiency. Figure 1.4 (a) shows the comparison of the spectral (circuit-independent) sensitivities of the three photodiodes measured from a CTIA active pixel sensor (APS). Comparison of sensitivity, noise, and SNR averaged over all wavelengths

for all photodiodes using data from circuit-independent CTIA APS are shown in Figure 1.4 (b).

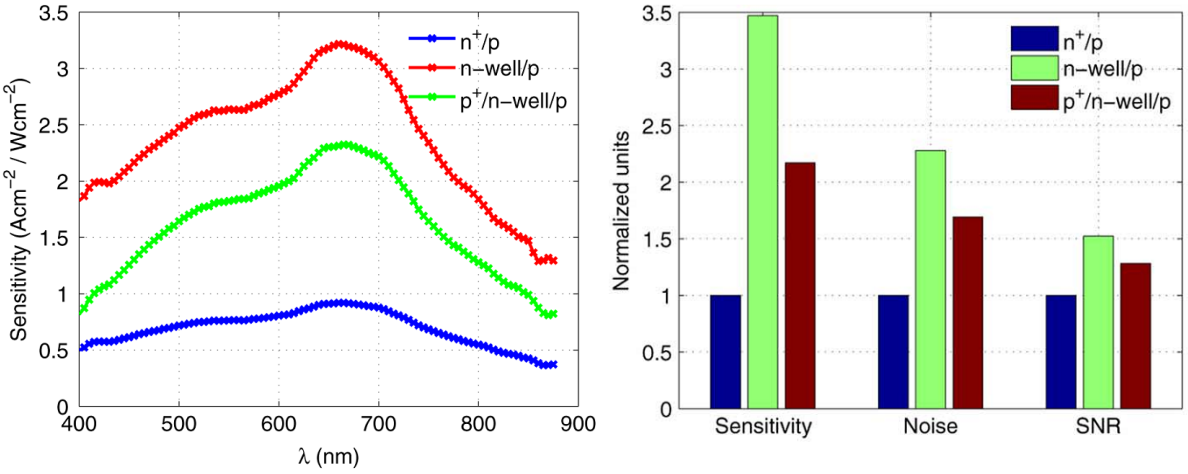


Figure 1.4. Spectral (circuit-independent) sensitivities (a) and averaged sensitivity, noise, and SNR (b) of the three photodiode structures [9].

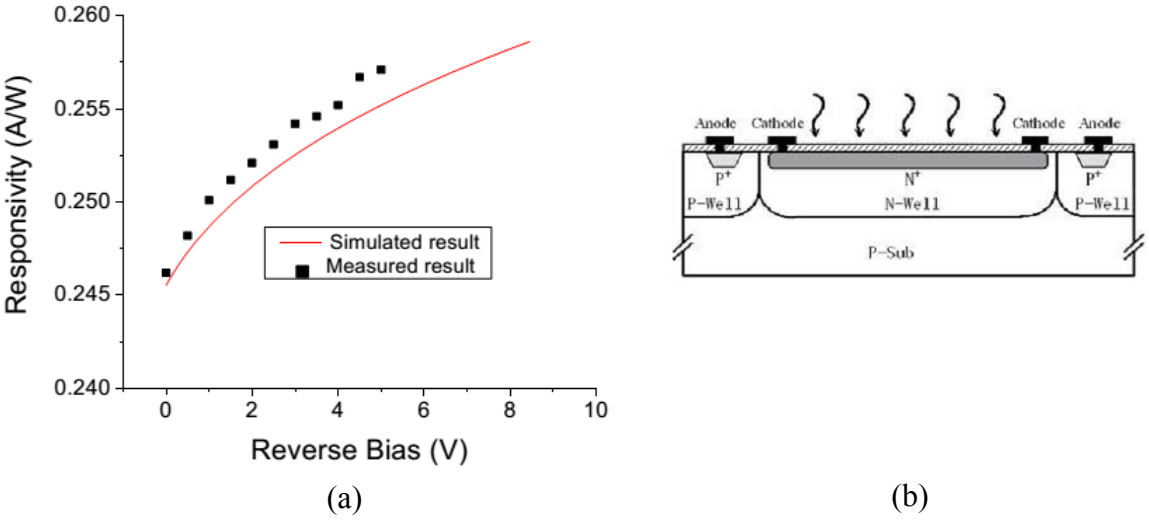
The larger sensitivity of the n-well/p-sub photodiode makes it the best option for testing our proposed new design. Furthermore, its larger dark current (Table 1.1), although not desired in general applications, is presented as an advantage in the bias-dependent unit cell.

Photodiode type	Dark current (nA/cm^2)
n^+/p-sub	96.2
n-well/p-sub	363.4
p^+/n-well/p-sub	90.3

Table 1.1. Dark current on the three types of photodiode [9].

It is desired for the proof of concept of the proposed ITP-ROIC, to have not only the photodiode response to the incident light but also a different gain on response in relation to the applied reverse bias. This requirement is confirmed by [10], which presents a

variation of the responsivity versus the applied reverse bias (Figure 1.5 a) in an n+/n-well/p-sub photodiode of 50 x 50 μm^2 (Figure 1.5 b), a device similar to the one adopted in this project.



(a) (b)

Figure 1.5. Spectral (circuit-independent) sensitivities (a) and device structure (b) [10].

1.4. Focal-plane array and readout integrated circuit

A focal-plane array (FPA) is an image device consisting of an array of pixels sensitive to electromagnetic radiation–i.e., photodiodes and DWELL–at the focal plane of a lens, most commonly for imaging purposes. A readout integrated circuit (ROIC) is a silicon-based chip that integrates the photocurrent generated by the sensors during a defined period of time, converting this charge in voltage for multiplexing to the output of the chip. Generally, each sensor of the FPA has one terminal connected to a common point with a defined bias voltage, and the other terminal is connected to the ROIC input via indium bumps, in a hybrid process know as flip-chip (Figure 1.6).

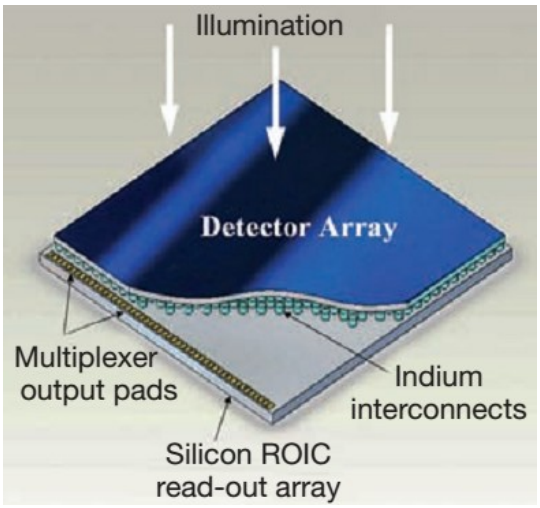


Figure 1.6. FPA hybridized over a ROIC [11].

1.5. Motivation

There is an increasing demand on next-generation infrared imagers to bring enhanced functionality to the pixel. Such functionality could include control over the color, polarization, and dynamic range of the sensor, enabling several applications and leading to the development of an infrared retina [7]. An infrared retina is defined as an IR-FPA that works similarly to the human eye to receive different spectral responses (colors) on different spatial pixels–rods and cones–but without the limitation of a fixed spectral response per pixel. These developments at the sensor-level demand advanced spatio-temporal circuitry at the pixel level. One approach to realize an infrared retina, involves the use of spectrally adaptive sensors that are bias tunable by exploiting the quantum confined Stark effect (QCSE) in the quantum dots in a well (DWELL) heterostructure [12]. Combined with a projection algorithm [8], the QCSE can obtain a continuously tunable detector with overlapping wavelength bands that can be used for target recognition. Only one focal-plane array (FPA) could be used to realize multicolor images, reducing the prerequisite for different spectral band sensors and the number of

connections on the same pixel. This requires a wide voltage-range bias and the ability to independently control the voltage bias on each pixel, the characteristics of which are provided by this novelty proposed ROIC. Commercially available ROICs, although offering two-color or dual-band capability for quantum-well infrared photodetectors (QWIP) [13], are based on dual stacked sensors, which need at least two contacts to the FPA. Our proposed architecture reduces the number of indium bumps by 50%, which requires less force during the FPA hybridization process with the ROIC. Moreover, the global pixel biasing in conventional ROICs does not allow advanced processing at the pixel level. Dual polarity for spectral response modification (Figure 1.7) also was demonstrated successfully on a p-i-n-i-p amorphous-silicon image sensor in a dynamic range of +/-2.4 V [14], proving the demand for the design proposed in this effort.

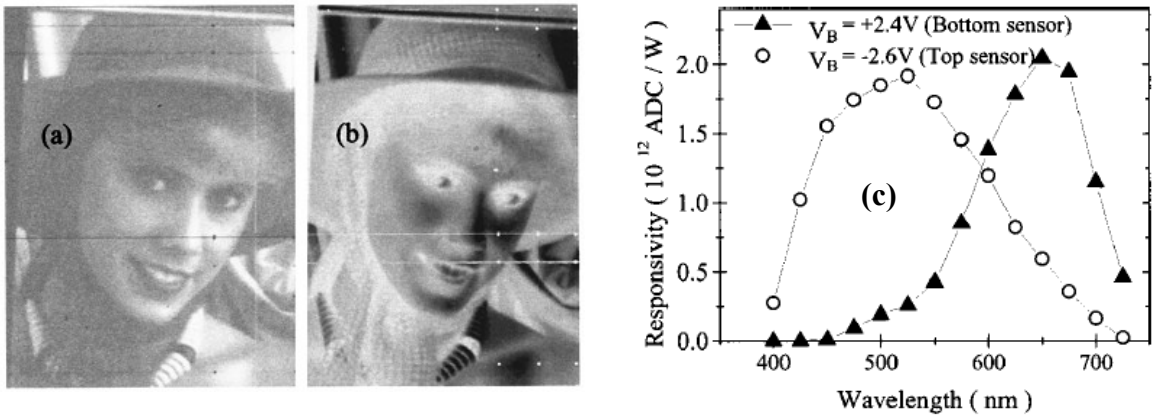


Figure 1.7. "Images taken with the array under white light exposition and sensor bias of -2.6 V (a) and 2.4 V (b), respectively. The image in (b) is reversed because of the different current flow direction in the detection system, since the two p-i-n sensors have opposite orientations. Some bad contacting gate and data lines can be observed" [14].

One can observe in Figure 1.7 (c) the spectral-response control in the visible spectrum, while the bias is changed only at the frame level (Figure 1.7 a-b), not at the pixel level, in which an RGB pixel could have its color defined only by its bias, not by its specific

physical/chemical constitution.

The target wavelength depends on the detector used. For example, the target wavelength for DWELL is 3 μm to 12 μm and for p-i-n-i-p is 0.4 μm to 0.75 μm.

Although several commercial ROICs present the option of dual polarity [15], conversely, it is a global pixel bias, presents a small input dynamic range of up to 3 V, and presents greater pixel pitch of 80 μm.

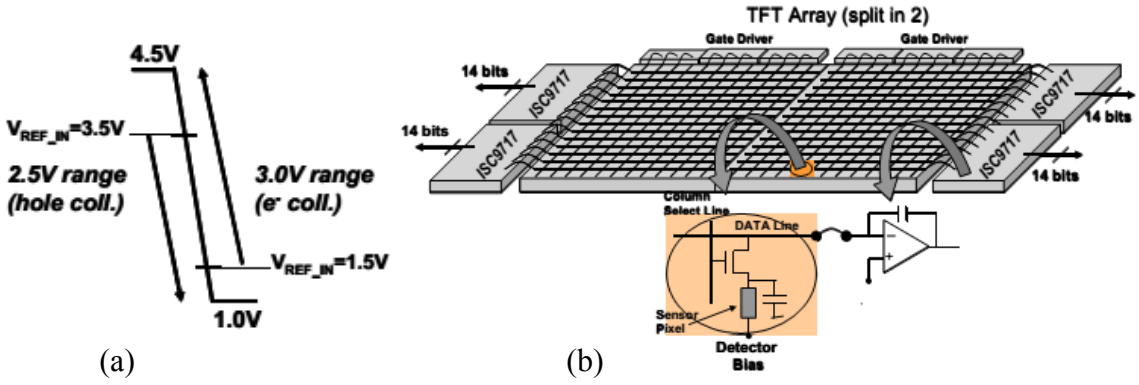


Figure 1.8. CTIA internal dynamic range (hole and electron collection) (a) [15];

Example of flat panel array configuration and TFT interface to the ROIC input (b) [15].

Unlike currently available commercial ROICs, Figure 1.9 (a), that apply the same constant bias across all pixels in a limited polarity selection and voltage range, in this paper, we demonstrate the first readout circuit capable of controlling each pixel voltage bias, individually. Furthermore, the new ROIC is capable of applying a dual polarity and a large bias voltage to the detector devices, in smaller pixel pitch. We have made it possible by implementing three different but integrated blocks in each unit cell (Figure 1.9 b), including analog memory capacitor (i.e., sample-and-hold capacitor), address selector, and reference recover circuitries.

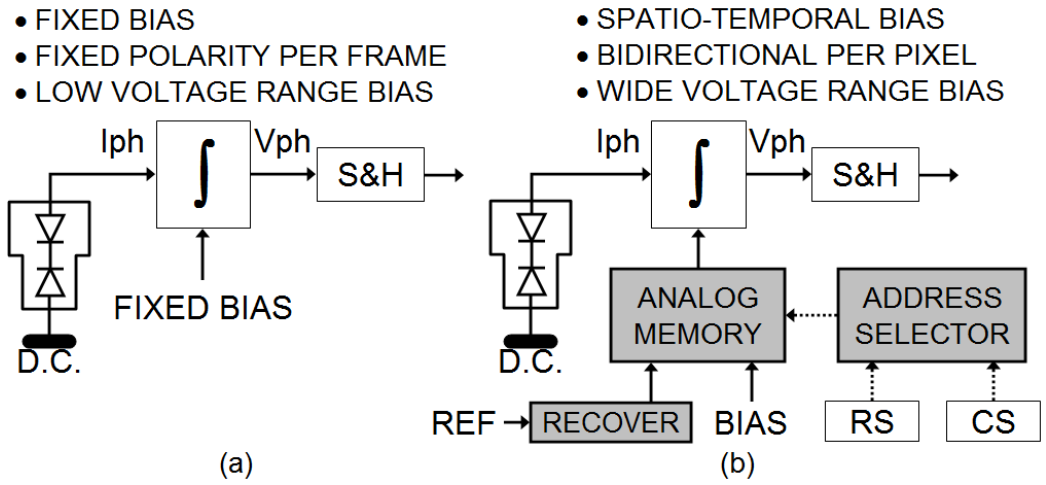


Figure 1.9. Typical (a) unit cell and new ITP-ROIC (b) unit cell.

1.6. Approach

A typical ROIC unit cell consists of a photocurrent-to-voltage integrator (Figure 1.9 a), where the same bias value is presented in all pixels of the detector arrays, during each frame. The bias is applied with respect to a detector common (DC) node, generally the backplane of the FPA. After the integration time, the value is stored in a sample-and-hold (S&H) block, keeping this value for external reading during the sweeping of all pixel addresses. This is known as integrate-then-read frame-time process. In contrast, our new approach presents an analog memory for each pixel and an address selector to synchronize the external desired bias to the pixel (Figure 1.9 b). This memory maintains the bias voltage during the integration time as well as during the S&H readout processing time, which is utilized to "write" the necessary individual bias for the next integration frame. In this way, we have different pixel biasing (spatial bias) inside each frame time

(temporal bias). This required an implemented voltage reference restoration block, aiming to subtract the initial pixel biasing from the integrated voltage, so that the result is sent to the S&H stage for external readout. As shown in Figure 1.10, the reading of each pixel integrated value is accomplished by a column selector (CS) and row selector (RS), which work as unit cell signal multiplexers. The reset and clock pulses applied on these shift-registers sweep and select one column and one row at a time, addressing one specific unit cell in the matrix. This typical structure had intensive circuit reuse for the address selector to achieve a compact unit cell.

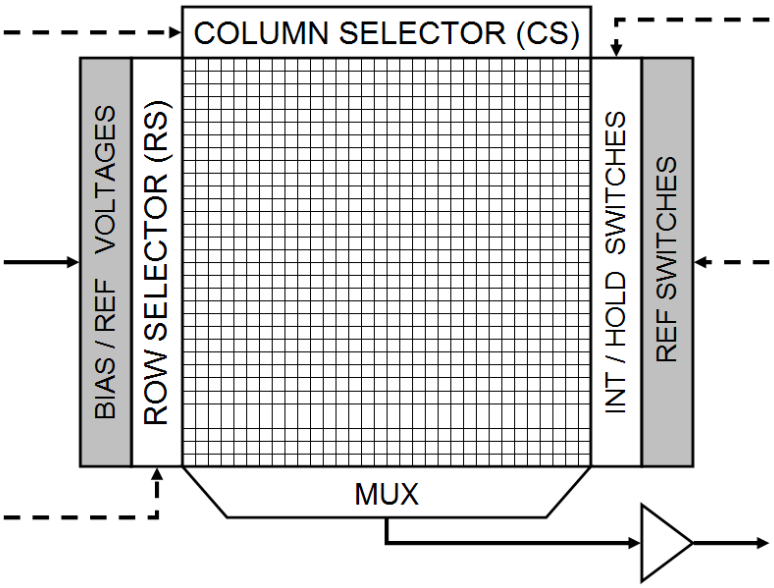


Figure 1.10. Typical ROIC multiplexer (white) with added features (gray).

1.7. Contribution of this dissertation

The main focus of this dissertation on spatio-temporal circuits for imaging sensors is to design, implement, and test a unit cell, an FPA, and an ROIC to individually define the pixel-bias voltage and to provide a solid basis for the development of a spectral-tunable

DWELL infrared camera.

The first contribution is the unit cell electronic circuit design, which should be compact, simple, and reliable to execute the required digital and analog functions: The digital function controls a row-versus-column selective transfer of an external voltage bias to the analog memory, the integration process, the voltage reference recover, the sample of the recovered voltage, and to the output voltage transferring to the column multiplex input. The analog functions: memorize a pixel-specific voltage bias, transfer this voltage bias to the coupled sensor, integrate the photocurrent generated by the sensor, convert this charge to voltage, recover a reference voltage level, and hold the processed voltage for external reading.

The second contribution is the unit cell layout implementation in a 2P4M 0.35 μm high-voltage CMOS technology, which was achieved in a restrictive area of 30 x 30 μm^2. Approximately half of this area was defined for use by four essential poly/poly2 layers capacitors, which should have the larger area–and respective capacitance–possible. A small area had to be defined for the VDD and GND pickup connection. Nine NMOS-type transistors and six PMOS-type transistors of the circuit–in a total of 45 terminals–were necessary to be designed and interconnected with only two available metal layers to nine internal nodes and 12 external nodes. Even the circuit presenting seven nodes shared between pairs of transistors of the same type, the restrictive design rules added to the limitation of the number of layers for interconnection had presented a challenge for this design, successfully executed after a systematic effort on devices and interconnection positioning.

The third contribution is the design and implementation of the ROIC itself–integrated

electronic circuit and interconnections to the FPA–necessary for generating of internal bias, for selecting of pixels, for transferring of input bias, multiplexing of output signals, and buffering of the video image. Several circuit blocks were implemented for these functions and, except for one issue that was corrected, proved to work appropriately.

In addition, the semiautonomous test and characterization system, with its flexible software and hardware developed, is working as a guideline for new test-bench structures of chip projects that are underway, to the best of our knowledge.

Additionally, the designed and implemented photodiode-based FPA and ROIC, together with the FPGA-based controller, are the first functional video camera designed and built in toto at the University of New Mexico.

Furthermore, the FPGA-based test system developed is a solid starting point to create an autonomous ROIC controller for fabrication at the commercial level, an essential feature for a portable infrared camera. Portable image systems could be the better option for preventive skin cancer examinations in rural communities, and presidents of these communities often are more likely to be exposed to sun and UV rays than are urban workers.

In addition, new techniques of chip interconnection were developed to obtain access to discrete devices, to test structures, blocks, circuits, and dies, and consecutively, to grant nondestructive, flexible, quick interconnections for definition of new test setups. These techniques are based on the use of line-distributed design layout, the semiautomatic wire-bonding process, an open-cavity chip carrier, zero insertion-force socket, and on a specifically designed connection PCB, liberating the IC design from relying on a limited number of external pad connections on the chip and on a package soldering process.

These milestones pave the way for a new ROIC with individual pixel bias control, which can be applied in a portable, tunable DWELL-FP, as described in the following publications and conference presentations:

- Glauco RC Fiorante, Payman Zarkesh-Ha, Javad Ghasemi, and Sanjay Krishna, "Design and testing of spatio-temporal tunable pixels for multi-spectral infrared imagers," IEEE Transactions on Very Large Scale Integration Systems, submitted on Jun. 30, 2013.

- Glauco RC Fiorante, Payman Zarkesh-Ha, Javad Ghasemi, and Sanjay Krishna, "Spatio-temporal tunable pixels for multi-spectral infrared imagers," (accepted), IEEE 56 MWSCAS, 4-7 Aug. 2013, Columbus, OH.

- Javad Ghasemi, P. Zarkesh-Ha, G. R. C. Fiorante, and S. Krishna, "A new CMOS readout circuit approach for multispectral imaging," (accepted) 2013 IEEE Photonics Conference, 8-12 Sep. 2013, Bellevue, WA.

- J.F. Xu, G. R. C. Fiorante, P. Zarkesh-Ha and S. Krishna, "A readout integrated circuit (ROIC) with hybrid source/sensor array," 2011 IEEE Photonics Conference, 9-13 Oct. 2011, Arlington, DC.

- Ajit V. Barve, Saumya Sengupta, Jun Oh Kim, John Montoya, Brianna Klein, Mohammad Ali Shirazi, Marziyeh Zamiri, Yagya D. Sharma, Sourav Adhikary, Sebastián E. Godoy, Woo-Yong Jang, Glauco R. C. Fiorante, Subhananda Chakrabarti, and Sanjay Krishna "Barrier selection rules for quantum dots-in-a-well infrared photodetector," IEEE Journal of Quantum Electronics, Volume: 48, Issue: 10, Oct. 2012.

1.8. Outline of dissertation

This work is organized as follows: In Chapter 2, the concept of the proposed individually tunable pixel ROIC (ITP-ROIC) is discussed, while in Chapter 3 the detailed circuit designs and implementation techniques are explained. The essential and particular infrastructure created for testing and characterization of this design are described in Chapters 4 and 5, detailing the hardware and software, respectively. In Chapter 6, experimental results are presented and analyzed. In Chapter 7, comments are offered and suggestions are made for continuing work.

Chapter 2

Chip architecture

The unit cell shown in Figure 1.9 (b) was intended to be functional yet simple enough to meet the unit cell area constraint. The circuit implementation of the ITP-ROIC unit cell is shown in Figure 2.1, together with the peripheral circuit-block diagram. The timing diagram for the dark-current response (covered chip) is shown in Figure 2.2 with Pixel 1 bias in full cycle. The CTIA integrator was chosen because of its high linearity, detector bias stability, and its capability of applying positive and negative biases to the detector. As the column and row selectors receive the reset and clock pulses to activate the output of a specific pixel, the internal address selector circuitry, represented by the AND-gate in Figure 2.1, activates the bias switch (SW-BIAS) that transfers the desired external bias voltage (V-BIAS) to the analog memory capacitor (C-MEM). After the initial reset and on the start of a frame, the integration switch (SW-INT) is turned on, and therefore the opamp operates as a buffer, reflecting the voltage on C-MEM to the detector through SW-INT. The sample-and-hold switch (SW-HOLD) is kept off, once the sweeping selection of unit cells for writing bias on each C-MEM in this frame is simultaneously reading the value on the hold capacitor (C-HOLD) from the previous frame. At the end of the writing/reading process, the integration switch is opened and the reverse-bias detector current charges the C-INT proportional to the applied bias and time of integration. During the integration time, both RS and CS are reset, avoiding any SW-BIAS to be activated and/or avoiding any change in the bias and reducing any noise generated by the clock/pixels scanning. After the desired integration time, every C-INT acquires the original bias added with the integration value.

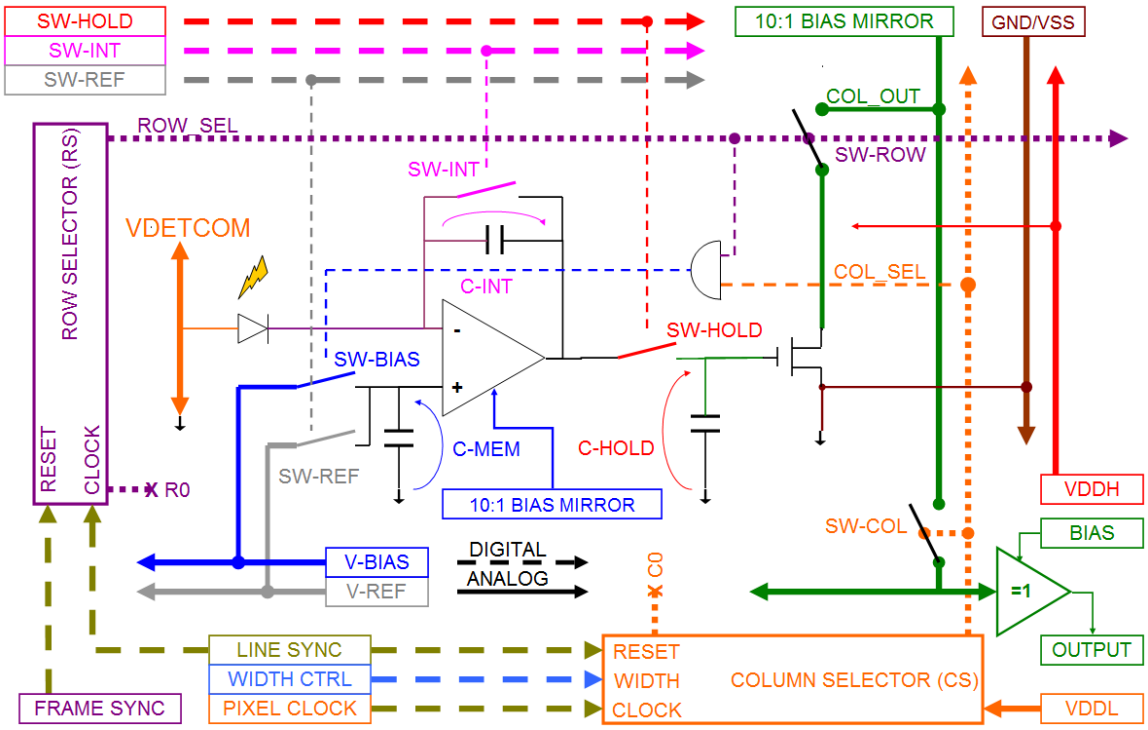


Figure 2.1. Circuit of ITP-ROIC unit cell and peripheral circuit-block diagram.

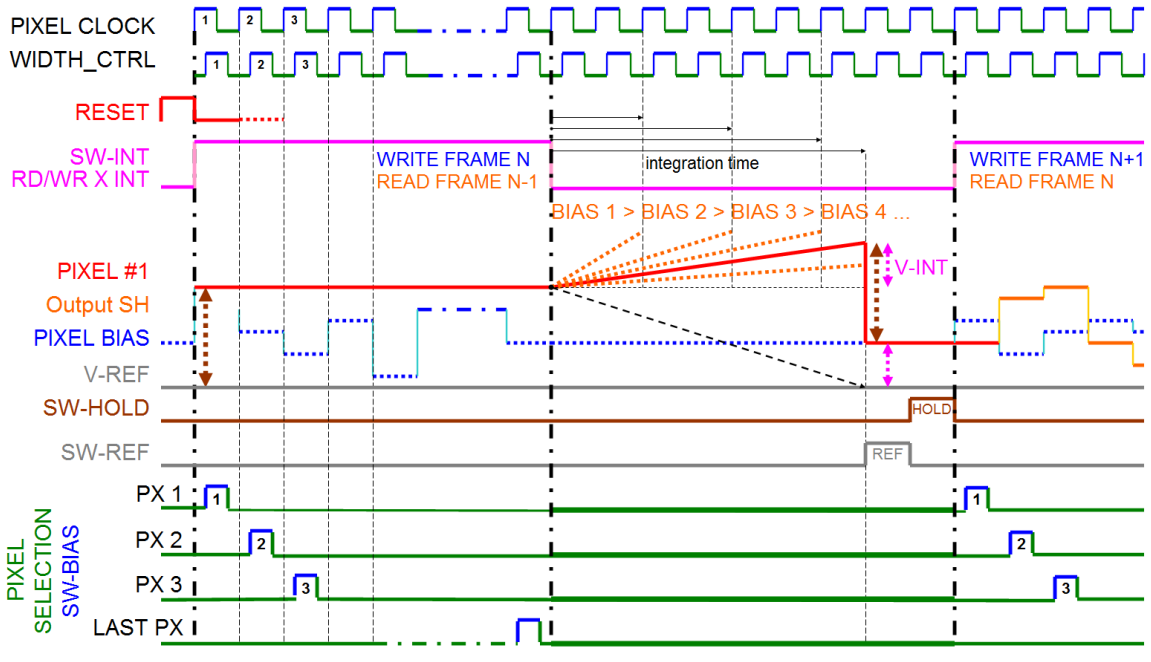


Figure 2.2. Timing diagram of main signals on ITP-ROIC.

Turning on the reference switch (SW-REF), the external reference voltage (V-REF), which is 0 volts, will be transferred to C-MEM and reflected over all of the detectors, resulting only in the integrated voltage in the opamp output. Then the SW-HOLD memorizes the value of the integrated voltage on C-HOLD to be read in the next frame.

The timing of one line-scan is used as the minimum integration time, allowing, if needed, synchronization and visualization of the specific unit cell integration values on these "hidden" lines on the frame grabber.

Also, the line-scan time, i.e., number of clock pulses, is the step of integration time parameter. The limitation of maximum integration time probably will occur when some noise/leakage current matches a small photocurrent and avoids the capacitor to integrate its charge. The actual value is limited in the program and when reached turns off the hold pulse. The pixel clock versus the desired FPS is related with the integration time. In the future, the current of the DWELL together with the integration capacitor and voltage range on CTIA define the pixel clock and the FPS.

2.1. Operational amplifier

Because of the unit cell area constraint, a two-stage operational amplifier (opamp) (Figure 2.3) with only seven transistors was designed and used to implement the CTIA. Table 2.1 shows the opamp specifications extracted from Spice simulations. The opamp supply voltage was defined as +/- 7.5 V and its bias current as 1 μA. To save space on layout, the output bias-current mirror transistor was implemented outside the unit cell, and the input bias-current was generated externally by a resistor on a 10x-size mirror transistor.

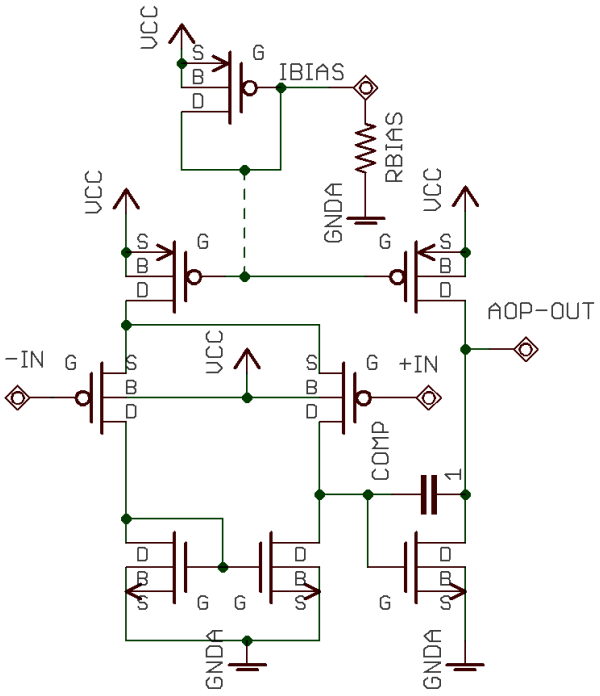


Figure 2.3. Electronic circuit of the two-stage operational amplifier adopted in the unit cell.

Dynamic range	-7.3 V to 6.7 V
Offset	116 µV
Power	95.9 µW
ft	42 MHz
Gain_dB	64.4
f3db	47 kHz
Phase margin	13.4 Deg
Slew rate (rise)	84 V/µs
Slew rate (fall)	- 132 V/µs

Table 2.1. Opamp specifications using Spice simulations.

2.2. Unit cell

The detailed electronic circuit diagram of the unit cell is shown in Figure 2.4, where one can note its devices and respective functions:

M3, M4, M5, M6, M13, M14, M15, the operational amplifier of CTIA.

Comp, frequency compensation capacitor.

C4, BIAS/ZERO capacitor

C2, integration capacitor.

C3, HOLD capacitor.

M10, the bias switch.

M9, the reference voltage switch.

M7, the integration switch.

M8, the hold switch.

M1, output buffer.

M2, column input-multiplexer switch.

M11, M12, unit cell address selector.

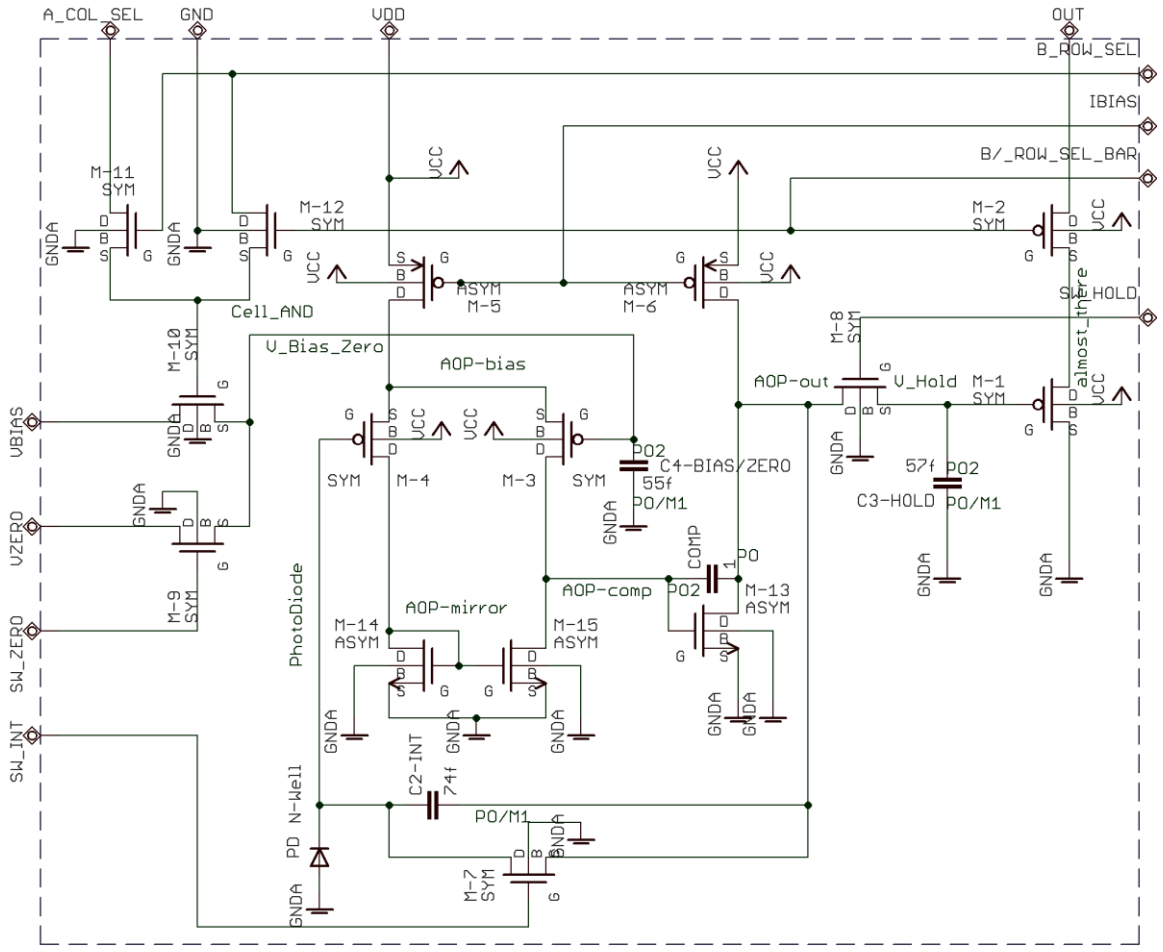


Figure 2.4. Unit cell electronic circuit diagram.

2.3. Column driver

The low voltage output of the row and column selector must be modified to high voltage to control the unit cells. We have used a standard level-shifter for the row select.

However, in addition to a standard level-shifter, the column select contains the control signal (width_ctrl) to avoid cross-talk of the bias voltage between two adjacent pixels while the pixel clock selects adjacent columns. In addition, the column driver contains an analog multiplexer to generate the video signal. The schematic of the column level-shifter is shown in Figure 2.5. As illustrated, the circuit includes one transistor that mirrors the column-bias current, the multiplexer switch, and a 2-input NOR-gate, which externally controls the width of the column selection pulse. The column bias transistors are mirrored on a 10x-size transistor that has a bias current of 20 μA defined by an external resistor to GND.

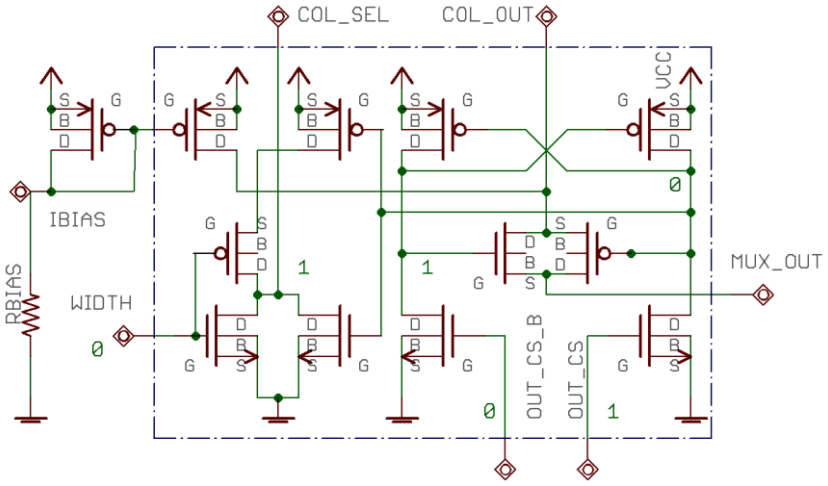


Figure 2.5. Level shifter, column-bias mirror, selector, width control, and MUX circuit.

Chapter 3

VLSI Design

3.1. DRC and minimum feature size

Tanner EDA tool [16] was chosen for the chip design, and for the manufacturing was the double-poly, four-metal layer, standard 0.35 µm mixed-signal 3.3/15 V TSMC high voltage CMOS process [45], presenting a manufacturing grid of 0.025 µm, internal unit (and mouse grid) of 0.001 µm, and contact size of 0.36 x 0.36 μm^2. Considering the small number of components, using the exact minimum feature grid size of 0.001 µm or even 0.01 µm could generate difficulties in design to snap shapes together. Thus, a grid of 0.05 µm was selected, allowing a better matching of shapes (Figure 3.1).

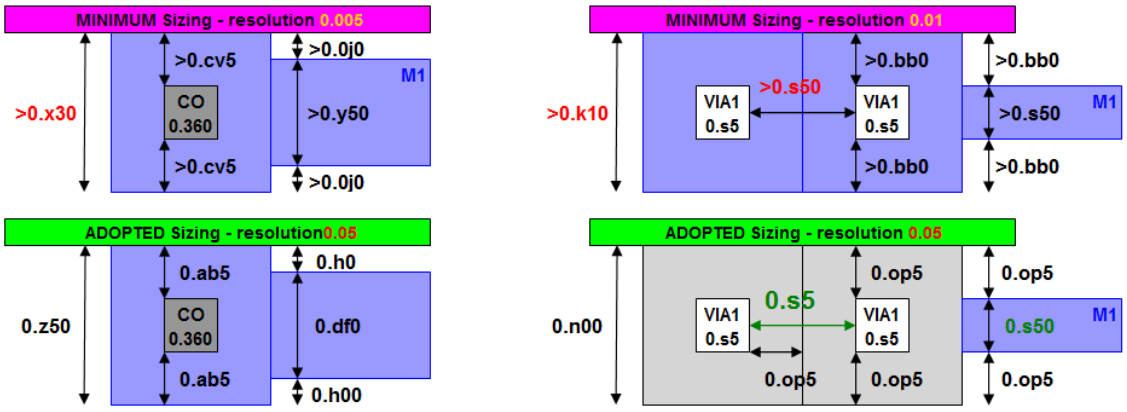


Figure 3.1. Minimum feature size, resolution, and adopted values (not to scale).

With the auto-DRC verification disabled due to the excessive computational effort required, a draft of the minimum features was necessary (Figure 3.2. Values omitted due to confidentiality contract-terms). As a tool to help with a semiautomatic visual DRC, one layer was created, and the minimum distance metal 1 to metal 1 layer was drawn. Working with the snap tool, the design process was facilitated.

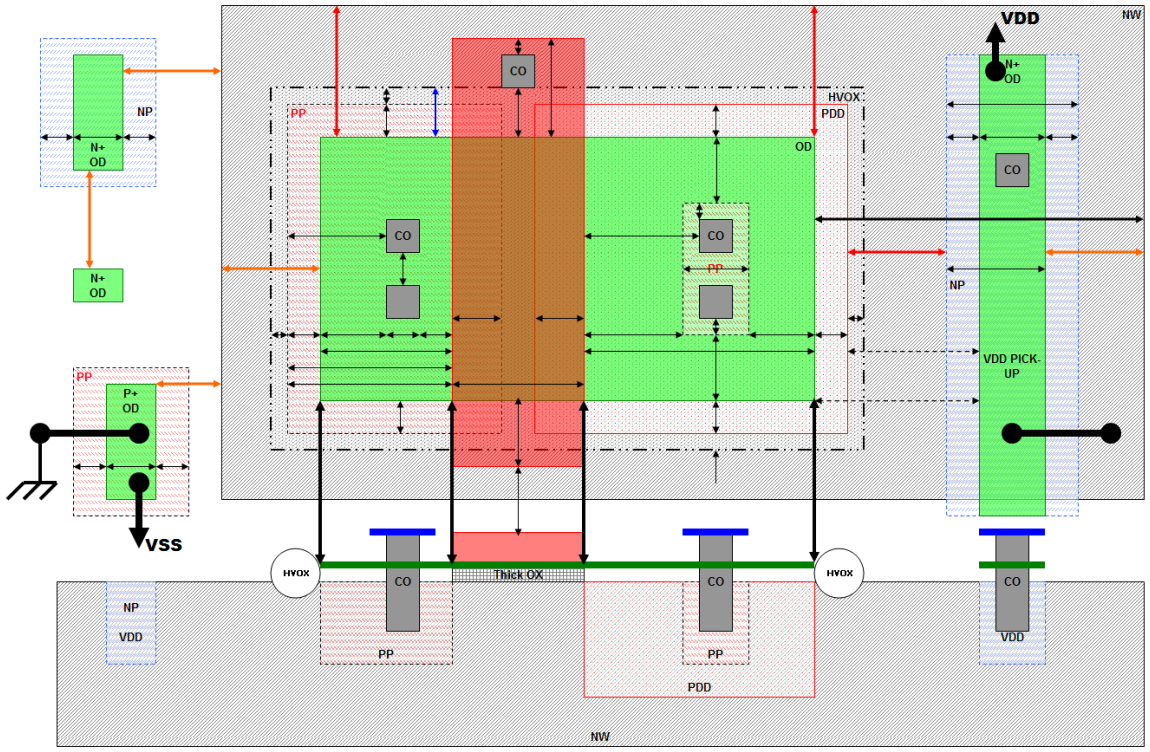


Figure 3.2. Draft of DRCs to be considered (not to scale).

3.2. Interlayer connections

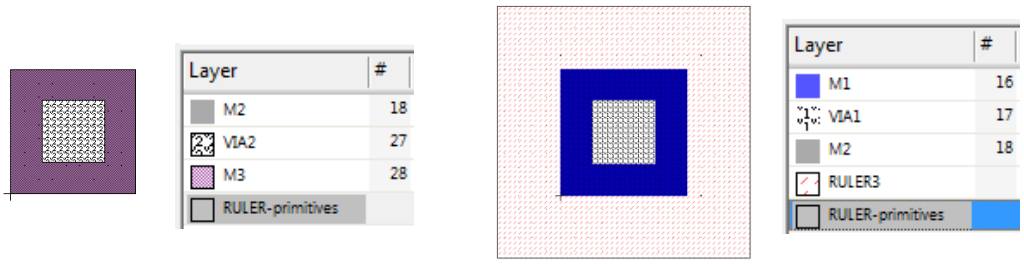
A decision was made to create design cells with all the necessary layers for particular applications, to reduce the possibility of omitting some required layer for the connection between layers, to reduce the DRC error notifications and its correspondent rework, and to take advantage of the hierarchical structure of design that existis in the adopted program.

The main cells created for interconnection layers:

- NP or PP to metal 1 using contact.
- Poly to metal 1 using contact.
- Metal 1 to metal 2 using via 1.

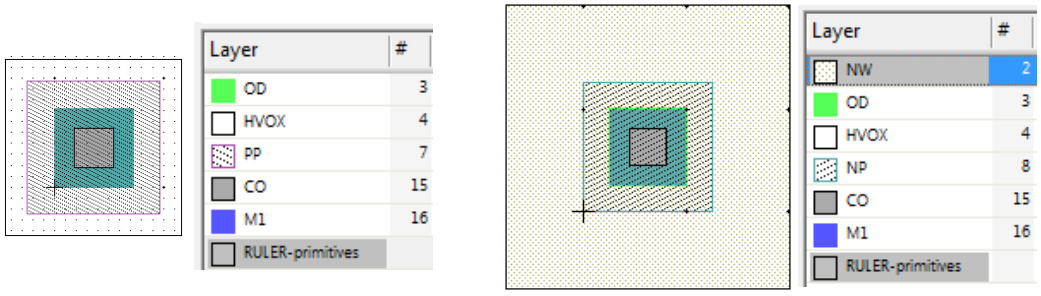
- Metal 2 to metal 3 using via 2.
- Pickup to VDD or GND.
- Contact to metal 1 on poly/poly2.

One can observe the RULER3 layer as the minimum distance between metal 1 objects.



(a) (b)

Figure 3.3. Metal 3 to metal 2 (a) and metal 2 to metal 1 connection (b).



(a) (b)

Figure 3.4. Ground pickup to metal 1 (a) and VDD pickup to metal 1 (b).

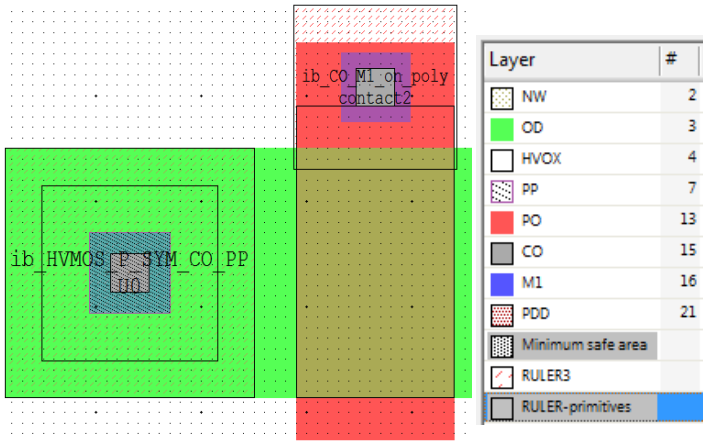


Figure 3.5. Active area and poly contacts to metal 1 cells.

For large interconnection between metal layers, one specific cell can be defined on setup for a semiautomatic matrix creation (Figure 3.6).

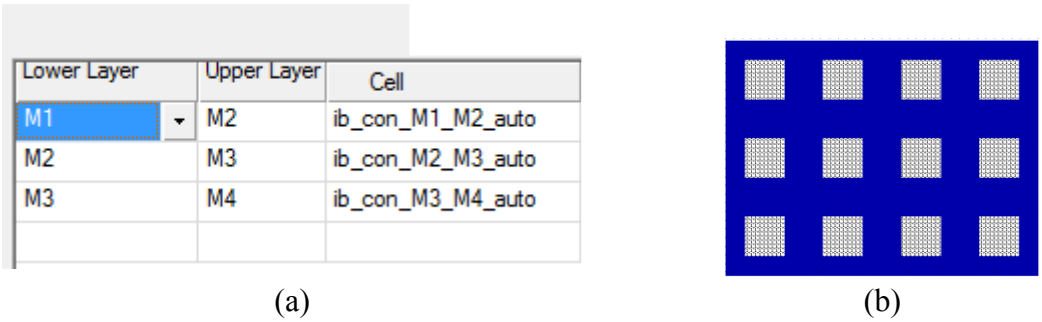


Figure 3.6. Setup definition of cells (a) for semiautomatic matrix creation (b).

3.3. Discrete devices and test structures

The manufacturing of individual devices, although they could be simulated, is important for replication of the designed core circuit in a way that any node could be accessed, measured, and analysed, as well as for new connections and circuit configurations that could be tested quickly without simulations or without manufacturing a new chip. Furthermore, photoelectric effects on diodes and transistors are not completely simulated on standard programs. Several test structures of individual devices and complete circuits were implemented on the test chip to characterize each one and to reconstruct the unit cell with discrete components, if necessary. The test structures on top of the chip (Figure 3.7) include:

- Two isolated internal pads for leakage and capacitance characterization.
- One poly capacitor for capacitance characterization.
- Seven types of photodiodes.
- Symmetric and asymmetric NMOS transistors.

- Symmetric and asymmetric PMOS transistors.
- One separated pad with ESD protection.
- A separated unit cell.

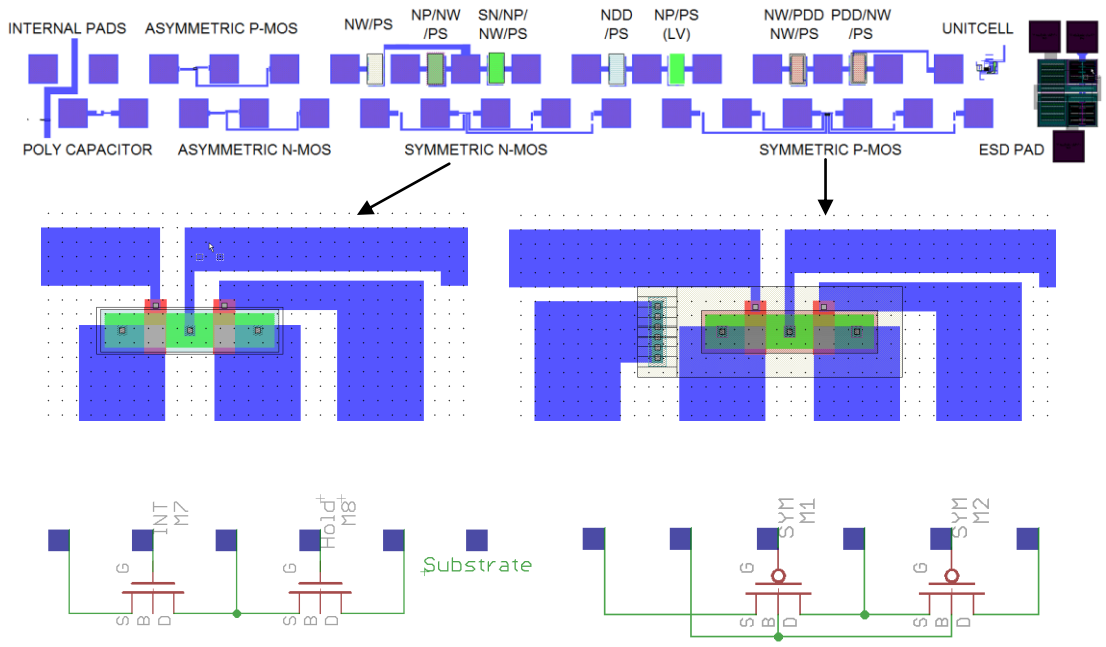


Figure 3.7. Photodiodes, discrete devices, and ESD pad test structures on top of the chip (top), symmetric NMOS and PMOS transistors layout detail (center), and circuit (bottom).

The seven photodiodes test structures present 48 x 98 μm^2 and the following layers:

- NWell/Psub.
- NPlus/NWell/Psub with silicon nitride layer.
- NPlus/NWell/Psub without silicon nitride layer.
- NDD/Psub (Ndeep-drain to Psubstrate).
- NPlus/Psub (low voltage device).

- NWell/PDD//NWell/Psub.
- PDD/NWell/Psub (float PN junction, for characterization of VDETCOM node with different voltage than the actual 0 V).

The asymmetric PMOS transistor has its own pad connected to the Nwell layer for electro-optical characterization, the requirement of which was noted in previous designs. The test structures on the right and left sides of the chip are:

- Two poly resistors.
- The unit cell opamp.
- The bias transistor (Figure 3.8).
- Four types of photodiodes.

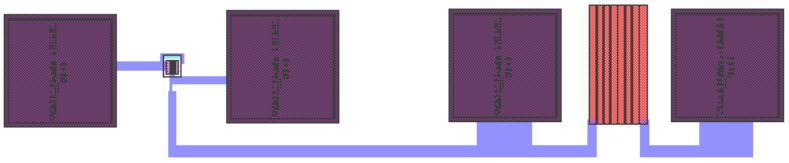


Figure 3.8. Bias transistor and poly resistor of 10 kΩ.

3.4. Photodiode

For the proof of concept and to demonstrate the functionality of the new ITP-ROIC without the direct implementation of the DWELL FPA, we have implemented the n+/n-well/p-sub diodes [9] as photodetectors in this project, as illustrated in Figure 3.9. This also allowed us to test and characterize the design at room temperature and to acquire an image at environment-illumination level with the use of single lenses.

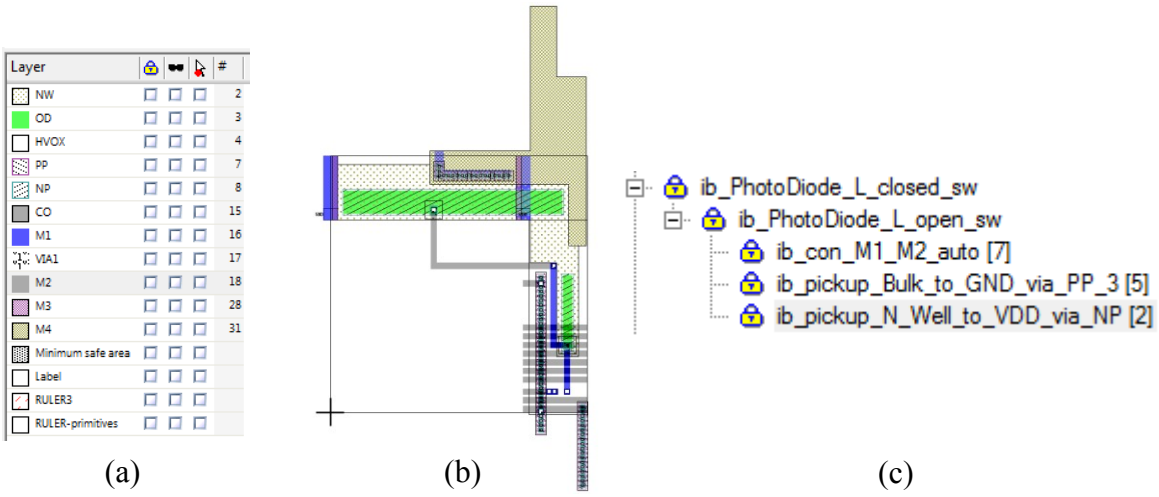
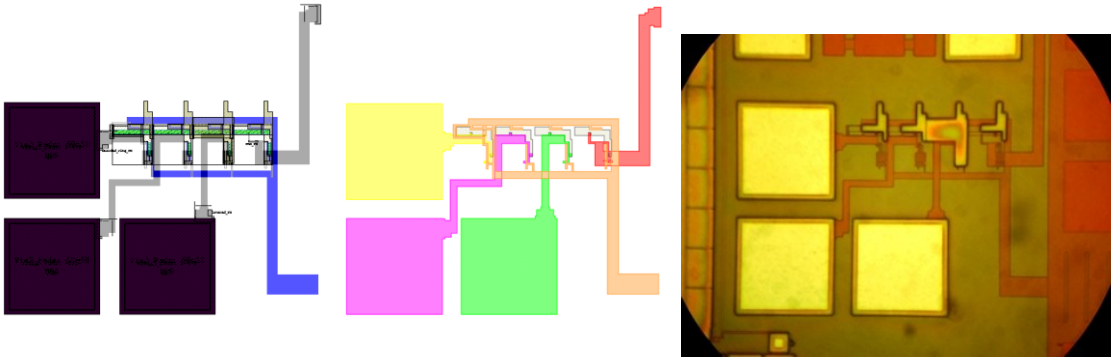


Figure 3.9. Photodiode design layers (a), cell (b), and its hierarchical design cells (c).

In this design, two access points were inserted to guarantee the connection of the photodiode, while a switch design cell allowed two versions of unit cells, one with connected photodiodes and another with an open circuit. For cross-talk reduction, one can observe the metal 4 layer covering the area not intended to be photosensitive, and one also can observe the substrate ground pickup. Several versions of this photodiode were designed for characterization as a copy of the original design, keeping dimensions, shapes, layers, connections, and the expected response characteristics. Figure 3.10 below (a) illustrates this test structure design, (b) shows the highlighted connections (with substrate connection rule disabled), and (c) presents its microphotograph. The photodiode from the unit cell (pink highlight in Figure 3.10 b) was connected to an internal pad. This same test structure was designed with a cover metal layer (green highlight in Figure 3.10 b) to permit the analysis of the scattering effect on the unit cell surroundings. For cross-talk analysis between pixels, one cell was designed with a guard-ring around the unit cell, (yellow highlight in Figure 3.10 b). Another photodiode structure was connected to an

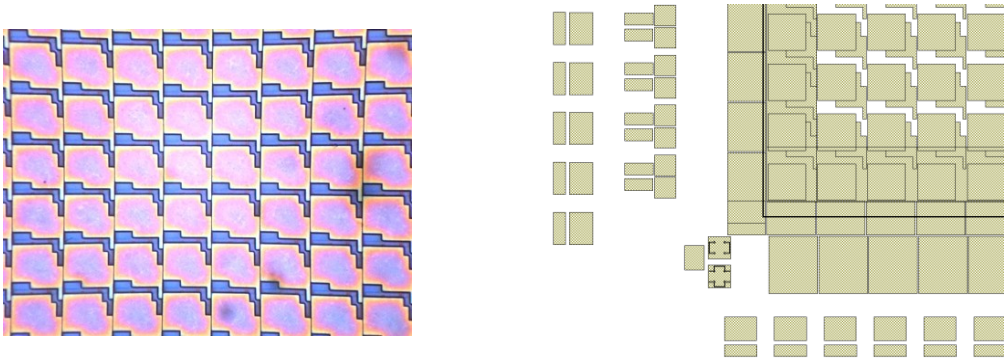
external pad that possesses the ESD protection (red highlight in Figure 3.10 b), aiming the verification of the ESD diode's influence that could trigger undesired side effects, such as a response to light or leakage.



(a) (b) (c)

Figure 3.10. Photodiodes test structures design (a), highlighting (b), and microphotograph (c).

A matrix of 98H x 97V pixels utilizing these photodiodes constitutes the FPA. The first and last columns, together with the last rows, were covered with metal layer 4 (M4), which resulted in a 96 x 96 active pixel FPA (Figure 3.11). In this way, the response from lateral scattering on the covered photodiode could be considered to compensate other's pixel's response.



(a) (b)

Figure 3.11. Active pixels matrix microphotograph (a) and margin columns/rows covering (b).

3.5. Current mirror

Each column of the FPA requires a current source for its biasing, and a 10:1 current mirror circuit was adopted to achieve this [17]. Figure 3.12 shows the layout of the input bias transistor with 50 µm on width size and the output bias transistor with 5 µm on width size. After the layout design, the type and size of the transistors, together with the information about the circuit nodes interconnections were extracted–using a specific tool on EDA–to generate a simulation Spice file. Simulation code using Spice (Figure 3.13) presents a source-gate voltage of 1.95 V for the desired drain current of 200 µA on the input transistor and 20 µA on the output (column) transistor (Figure 3.14).

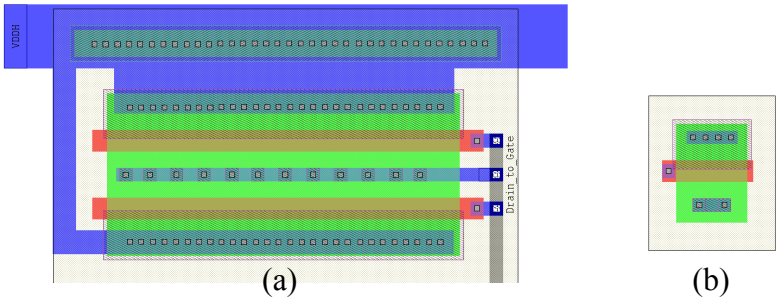


Figure 3.12. Layout of input bias transistor (a) and of output bias transistor (b).

```
*=============================================================================
*                                P- MOS VGS x ID CURVE for current mirror
*=============================================================================
.lib 'hv15.1' TT_hva
*| drain       gate          source   bulk     model    Lengh  Width
M8 GND         GND           VDD      VDD      pch_hva  l=1.5e-006 w=5e-005
*+ad=4.125e-011 as=6.5e-011 pd=2.83e-005 ps=5.52e-005  $(32.2 2.67 33.7 27.67)

M4 GND         GND           VDD      VDD      pch_hva L=1.5u W=5u *AS=13p PS=15.2u

*name          node+       node-          type     value
Vdd_out_ps     VDD         GND            DC       0V
*Vbias_ps         VDD         Gate           DC       0V
*----------------------------transient analysis---------------------------------------
*        sample time step     total simulation time to show
.tran    1us                  45ms
*.print  is(M8) iG(M8)  iD(M8)   iB(M8)

.dc Vdd_out_ps 0 4 0.05 *Vbias_ps 1 1.6 0.1
.print DC Is(m8) Is(m4)
*-------10--------20--------30--------40--------50--------60--------70--------80-----
```

Figure 3.13. Spice code for simulation of VSG x ID curve.

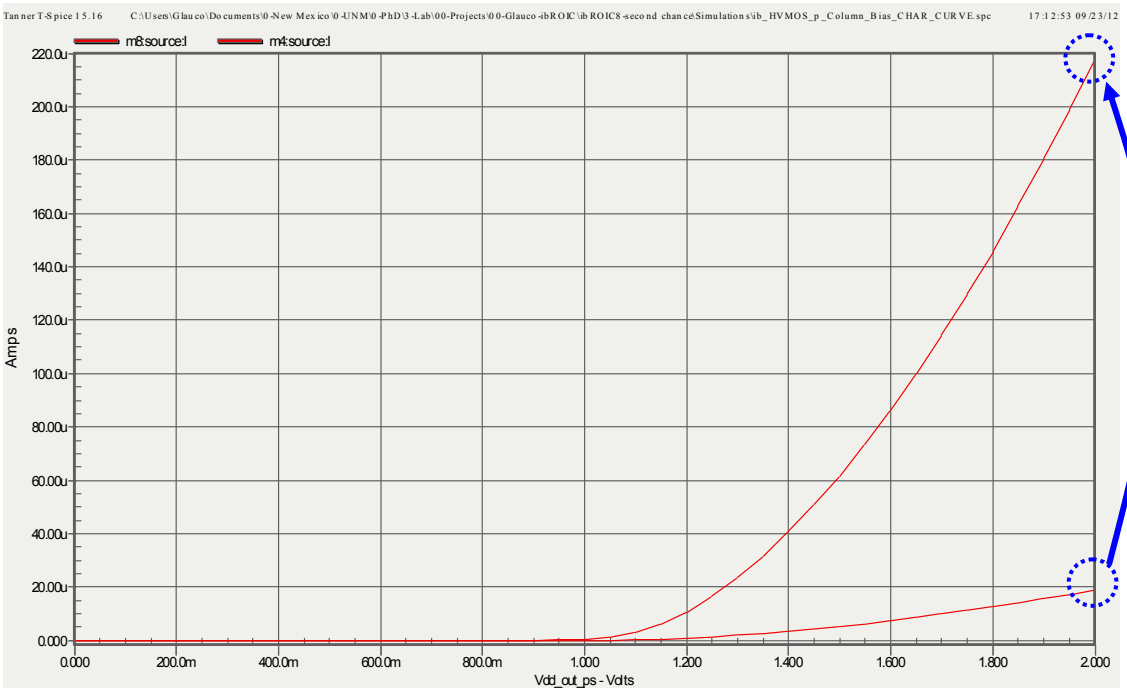


Figure 3.14. Simulated source-gate voltage versus drain current for the column-bias transistors.

3.6. Operational amplifier

The two-stage operational amplifier (opamp) was designed as part of the unit cell and its transistors were distributed as necessary to facilitate the interconnections. After the completition of the unit cell design and layout verification, a copy of the unit cell was made to delete the components not related with the opamp and a test structure design cell was defined (Figure 3.15). Inside this design cell, the bias mirror transistor was inserted and a ground guard ring was implemented. The non-inverting input, the invertin input, the output, and the bias mirror of the opamp were connected directly to external pads. In this way, an opamp with the same connections, dimensions, and positioning of components of that one in the unit cell, would be available for testing and characterization.

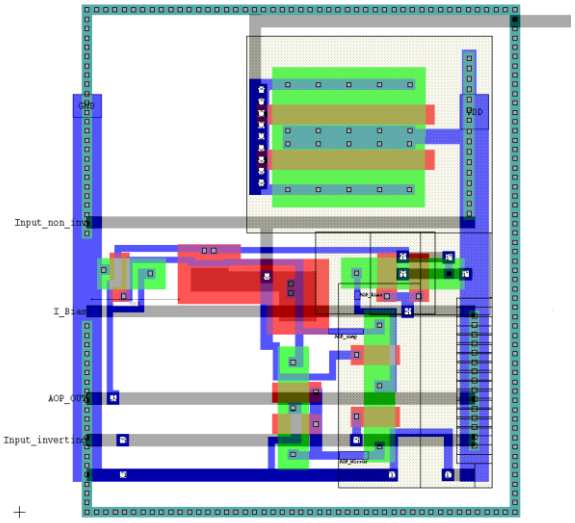
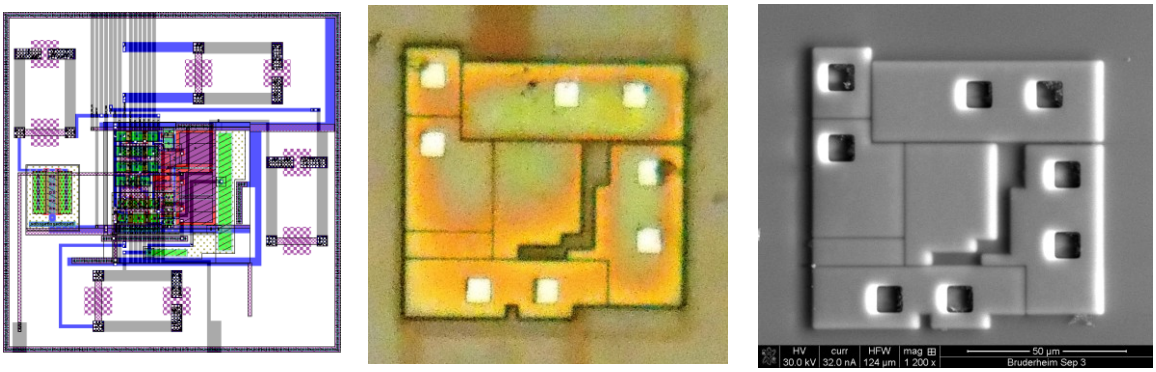


Figure 3.15. Unit cell two-stage operational amplifier layout.

3.7. Unit cell

The separated unit cell has 13 connections on ESD pads: one independent VDDH, six digital inputs, two analog inputs, two biases (one output), and access to photodiode and opamp output circuit nodes. Seeking to acquire experience with IC repair, “fuse” for etching and “jump” for metal deposition, test designs were implemented on key lines using the focused ion beam (FIB) tool. The windows on the silicon nitride layer of these structures can be seen in Figure 3.16 (c) by the scanning electron microscope (SEM).



(a) (b) (c)

Figure 3.16. Separated unit cell test structure design (a), microphotograph (b), and SEM (c).

Figure 3.17 illustrates the Spice simulation of the unit cell working as a buffer, with measurements on opamp output and unit cell output, for a complete input-voltage swing of 15 V (to substrate). One can note the unit cell minimum output-voltage of 4 V and maximum of 15 V, but due to the 3.5 V threshold voltage of the integration transistor, as the output of the opamp reaches 11.5 V, the integration transistor is turned off, opening the feedback circuit and saturating the opamp output.

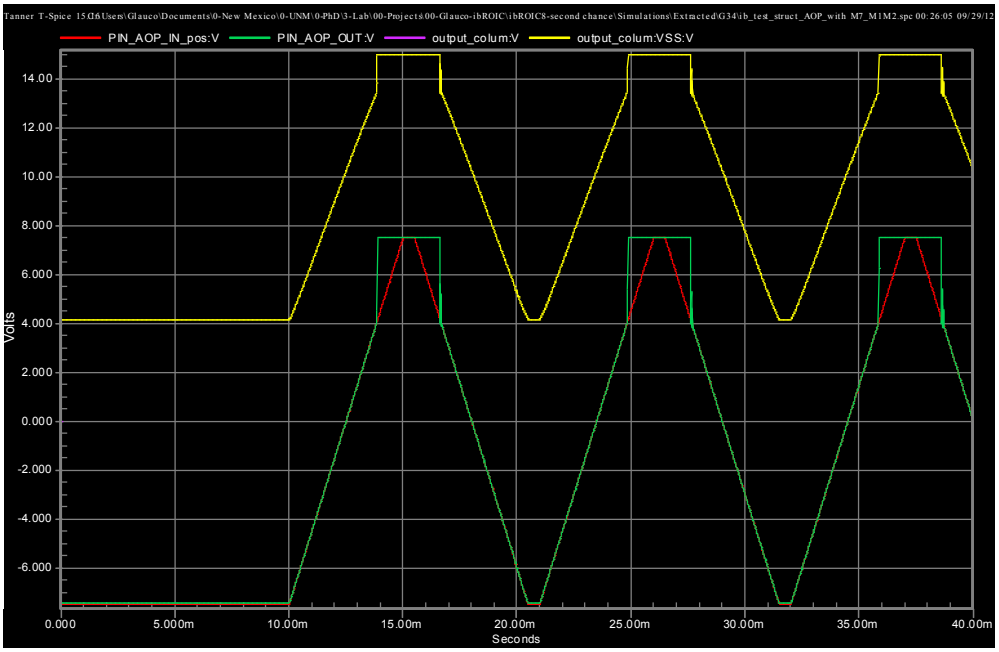


Figure 3.17. Spice simulation waveforms for unit cell output (top) and opamp output (bottom).

3.8. Row/column selector

The row and column selector consists of a 99-output shift register built with 100 D flip-flops (DFF) using the low voltage devices (3.3 V), with a minimum transistor width/length size of 0.9/0.35 μm/μm. Following the design for testability (DFT) technique, the DFF 99 (Figure 3.18) does not activate any column, but its output is driven directly to an external pad, as is its COL_OUT input. In this way, it was possible to verify the functionality of the column selector, to monitor the waveform controlled by

the width_ctrl pin, and to test the output buffer. Figure 3.19 shows the waveforms of the column selector in Spice simulation.

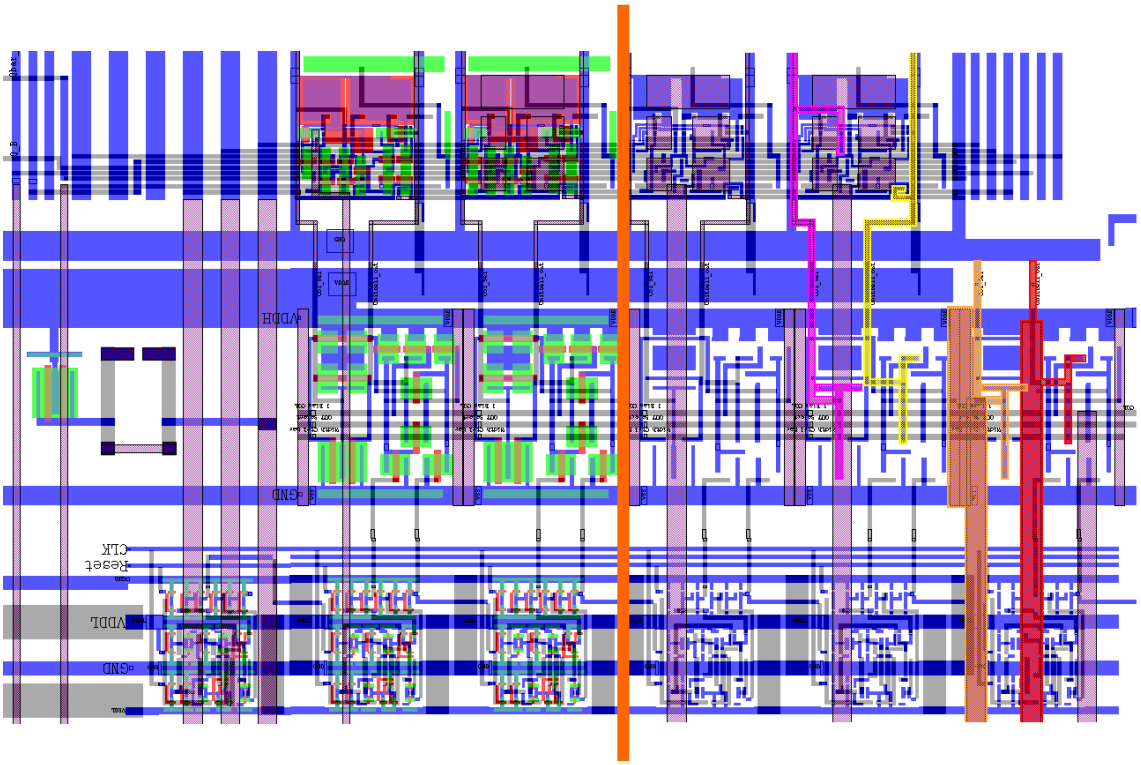


Figure 3.18. CS 0-1-2/level shifter 1-2 (left) and CS 97-98-99/level shifter 97-98-99 (right).

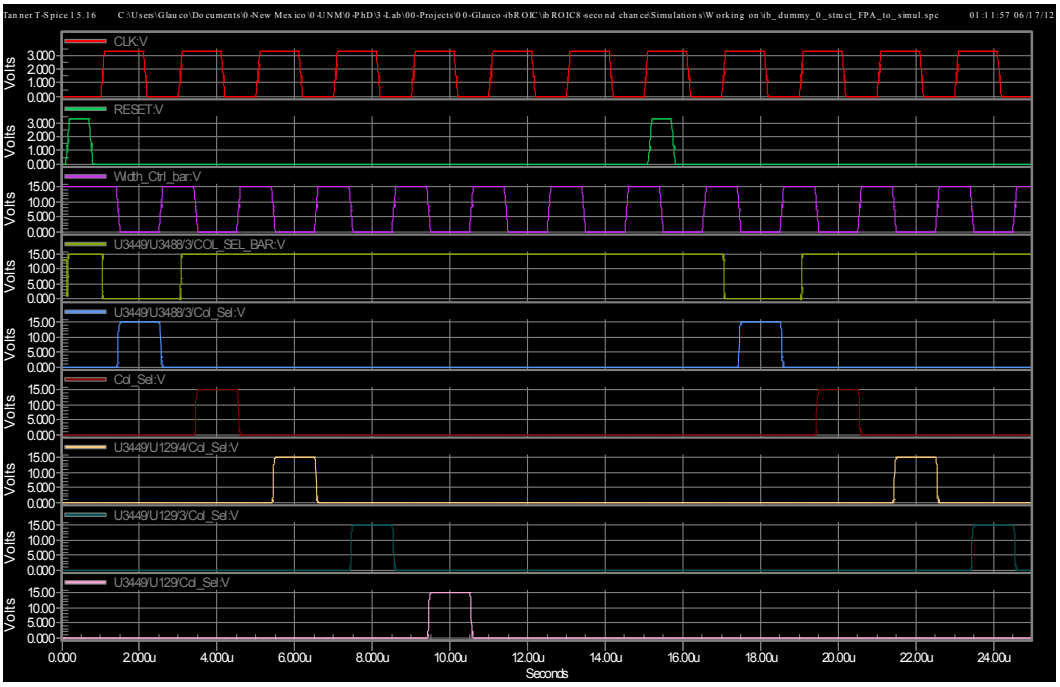


Figure 3.19. Waveforms of the column selector in Spice simulation.

3.9. Column driver

The layout of column driver block is shown in Figure 3.20. M10 and M11 are the level shifter input transistors, while M6 and M5 are the output transistors. M4 is the column mirror transistor, activated together with M9 and M3, the switch of multiplexer that receives the signal from unit cell output and transfers to out_select node. M1, M2, M7, M8, M12, and M13 constitute the 2-inputs NOR-gate for width control on Col_sel pulse.

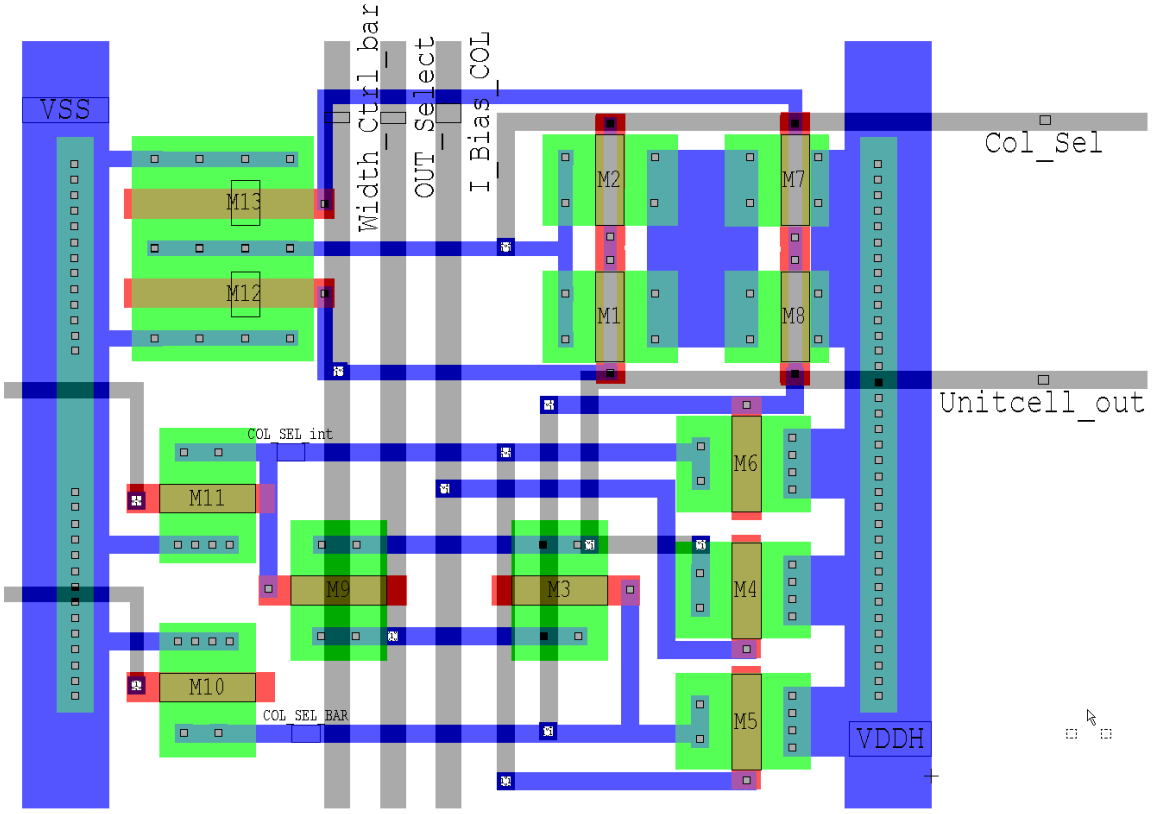


Figure 3.20. Level shifter, column-bias mirror, selector, width control, and MUX layout.

3.10. Row0_UNM as 19 x 5 matrix

Considering the low possibility of failure of the photodiode's response, the first row was designed with an open "switch" between the photodetector and the unit cell.

In this way, the individual pixel biasing control still could be demonstrated in a 19H x 5V image (Figure 3.21) using only one row with dedicated synchronization signals.

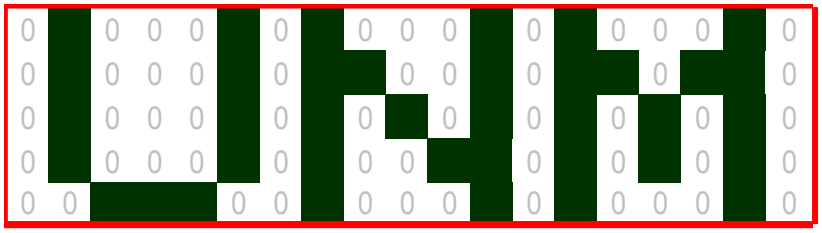


Figure 3.21. Matrix 19 x 5 pixels built from Row0_UNM.

To prove the integration process without the internal photodiodes in this first row, input nodes in Columns 97 and 98 were connected to pads, in a way that external current or photocurrent could be applied (Figure 3.22). Finally, a comparison between unit cells with and without photodiode response could be performed with this design specification.

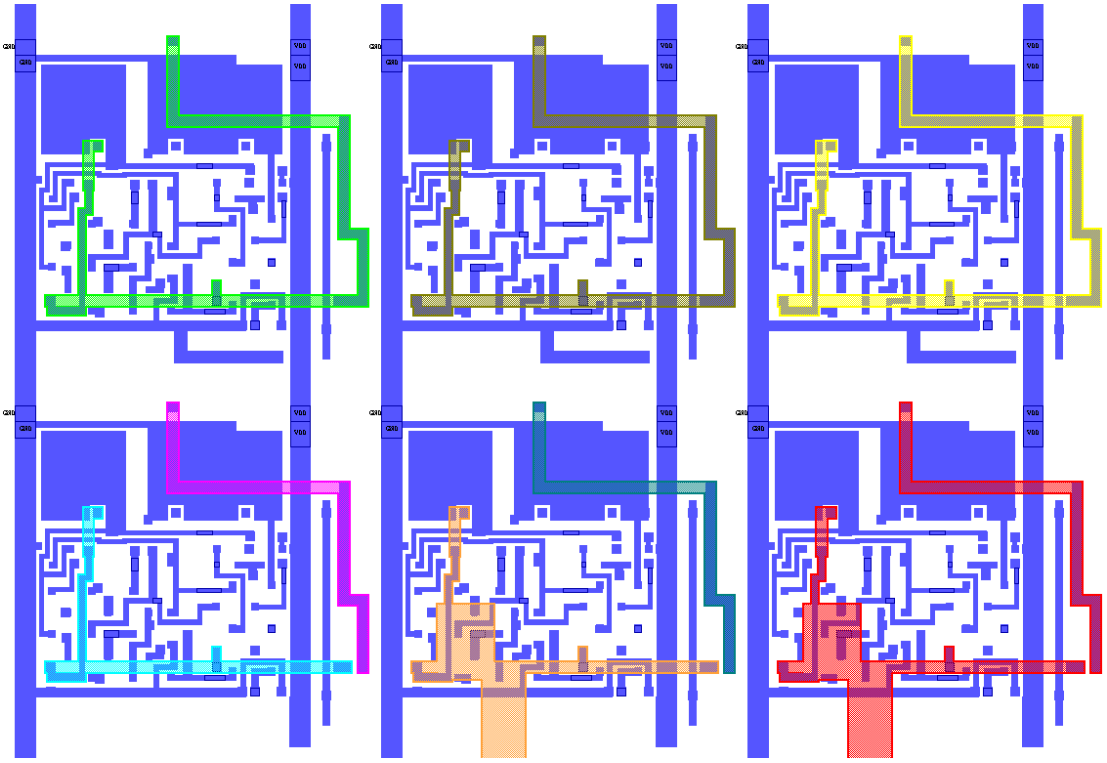
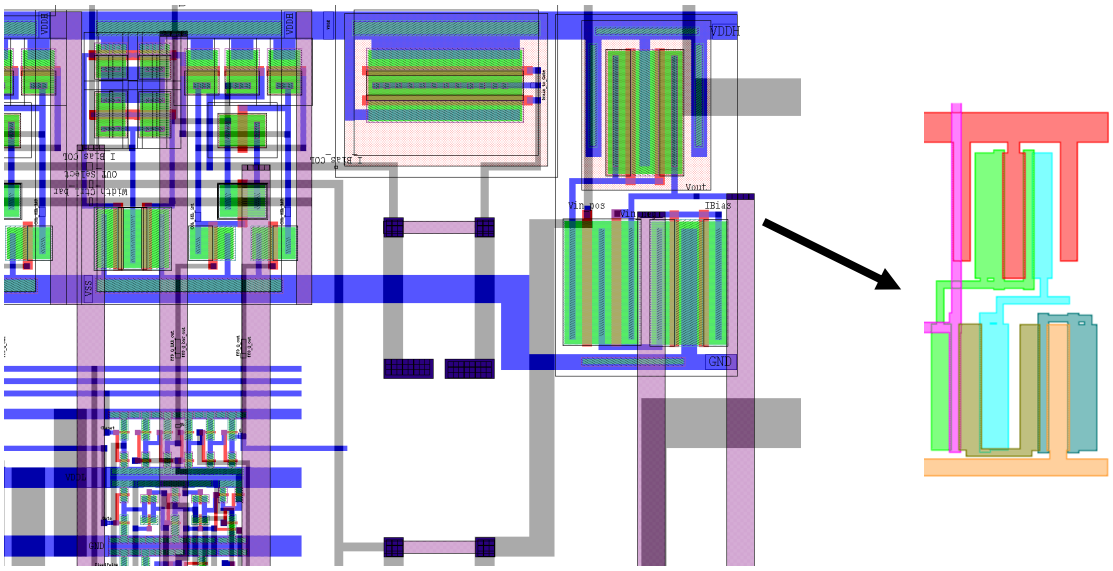


Figure 3.22. Row with photodiodes connected (top), without photodiode connection (bottom), and CTIA inverting input connected to pad (orange and red).

3.11. Output buffer

The output video amplifier consists of a single-stage opamp that was made as a buffer. It receives the signal of each column through the switches of the columns multiplexer. The output video buffer uses the high voltage VDD (+/- 7.5 V) and it draws 13 µA current for its bias. Figure 3.23 shows the design of the output video buffer and its highlighting for connection verification.



(a) (b)

Figure 3.23. Output buffer design (a) and highlighting (b).

3.12. Interconnection between blocks

After the design of unit cell, photodiode, test structures, FPA, level shifters, bias mirror, and output buffer, it was necessary to interconnect the power grid and input/output signals to external pads on the ring pad. Horizontal and vertical signal buses were designed to distribute these signals between columns and rows, as well as to the pads.

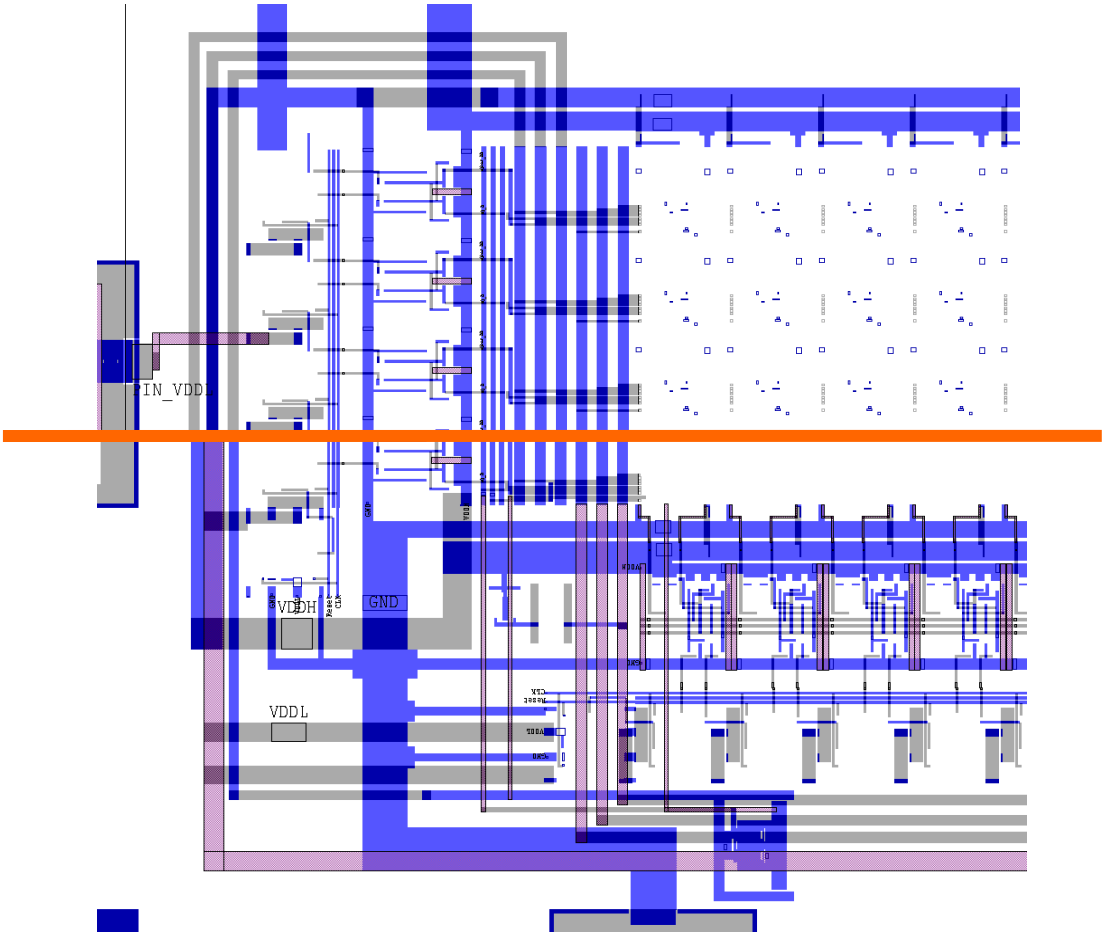


Figure 3.24. Top and bottom interconnection between blocks (two images mounted).

Highlighting of interconnection between blocks helps to identify open/short circuits, as well as the different signals distribution (Figure 3.25).

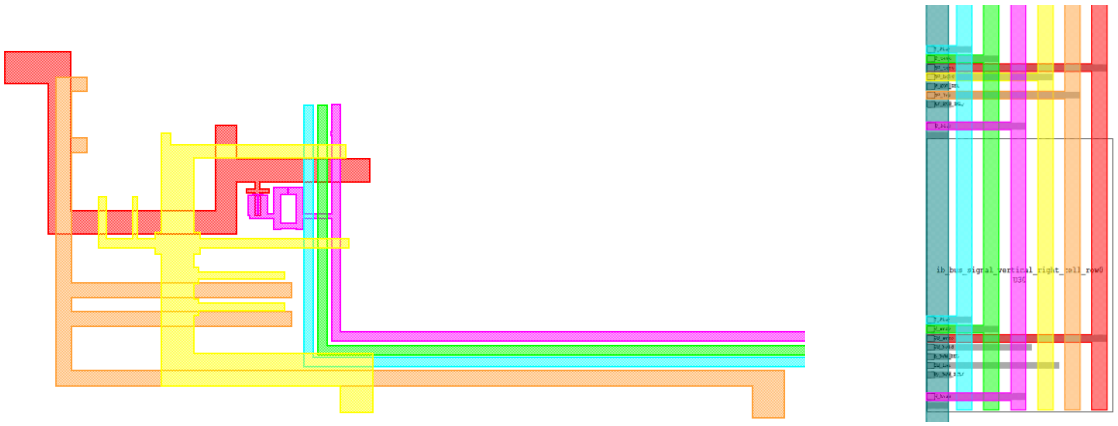


Figure 3.25. Highlighting of interconnection between blocks.

3.13. FPA simulation

Because of the large number of unit cells on the FPA, the simulation could take days and could present a similar response on thousands of pixels, and it would be difficult to trace this large number of signals and to analyze the process. Likewise, to build a smaller FPA design with only the unit cells could not detect connection problems on signal distribution lines of the final chip design. Consecutively, a 4 x 4 matrix of sensors positioned only on the corners of the 98 x 98 matrix was designed for the simulation of the FPA (Figure 3.26), keeping the signal distribution blocks and using new dummy-designed cells.

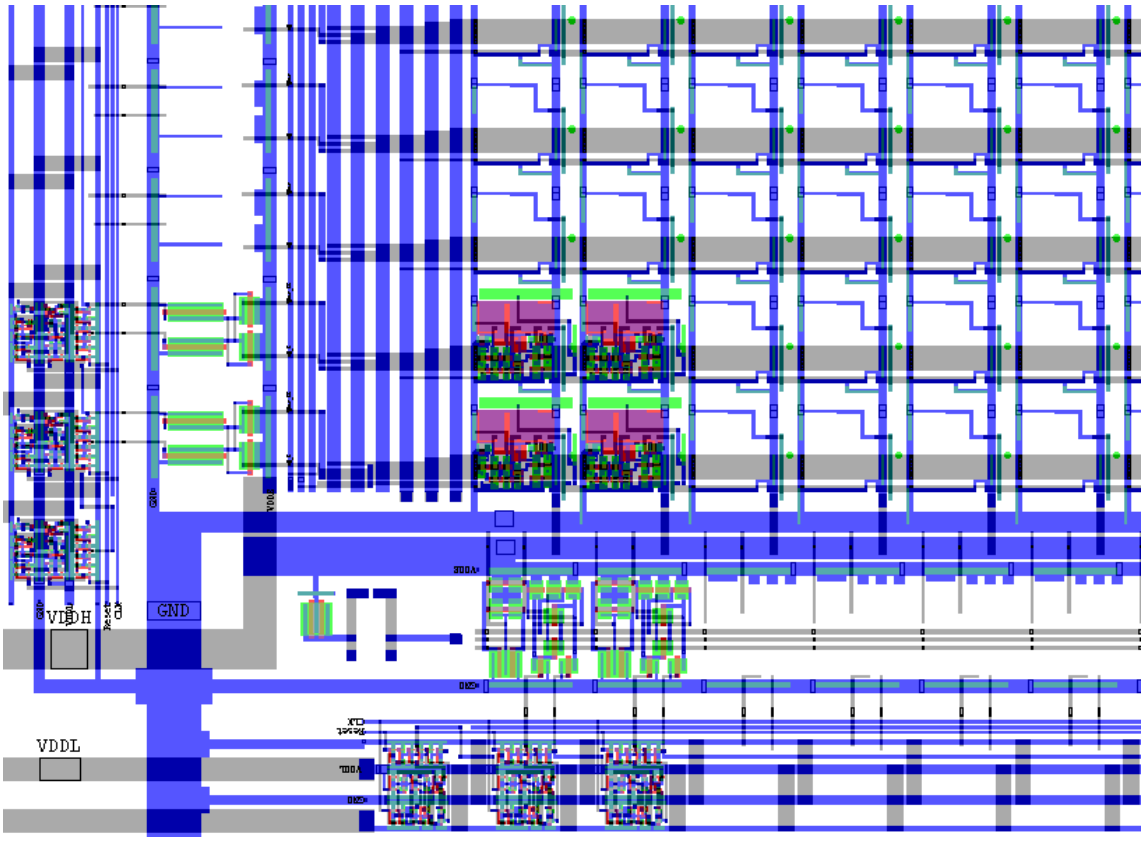
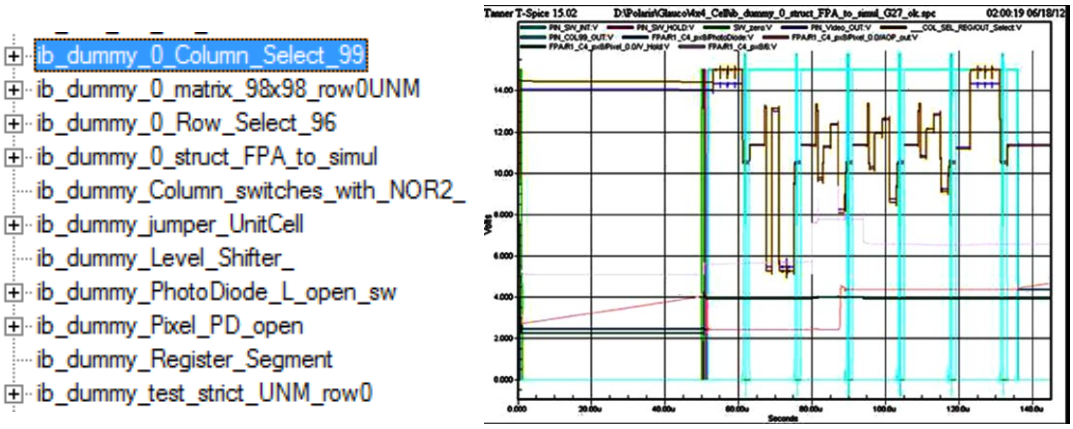


Figure 3.26. A 4 x 4 matrix with dummy-designed cells interconnecting the active cells.

Employing the hierarchical structure of design cells, these dummy blocks were created from a copy of the final design cell and were edited to contain only the necessary direct connections for passing through the signals to the next cell, as a bridge block. Moreover, any added design problem on these dummy blocks could be detected more easily with a smaller number of nodes. These design cells are listed in Figure 3.27, together with the simulation result of the 4 x 4 pixels dummy chip.



(a) (b)

Figure 3.27. Dummy-designed cells (a) and 4 x 4 matrix Spice simulation (b).

3.14. Future FPA

It is worth nothing that because of inadequate planning, the future application of this design on a 100% fill factor DWELL-FPA could present violations of design rules checking (DRC) and/or open/short circuits. Consequently, the DRC was checked against a 6H x 3V design cell with dislocated, flipped columns, and an overlapped power grid (Figure 3.28). Attention was taken regarding the metal layers on matching connections and minimum distance rules, the joined N-Wells areas, the minimum distances between the active area and poly layers, and to the shared positions of pickup to ground contacts.

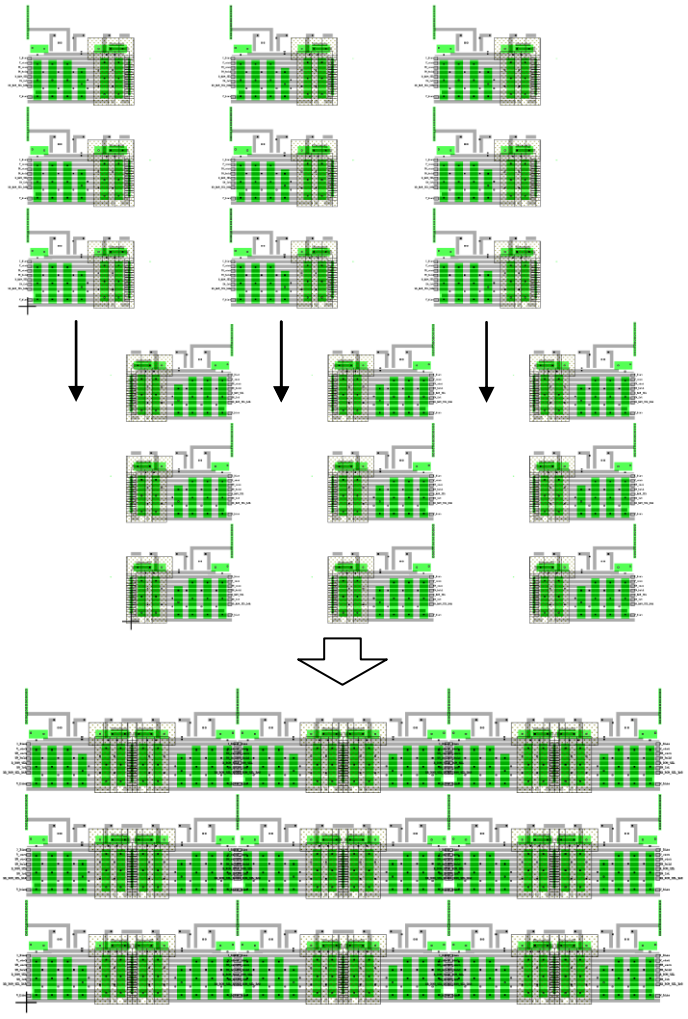
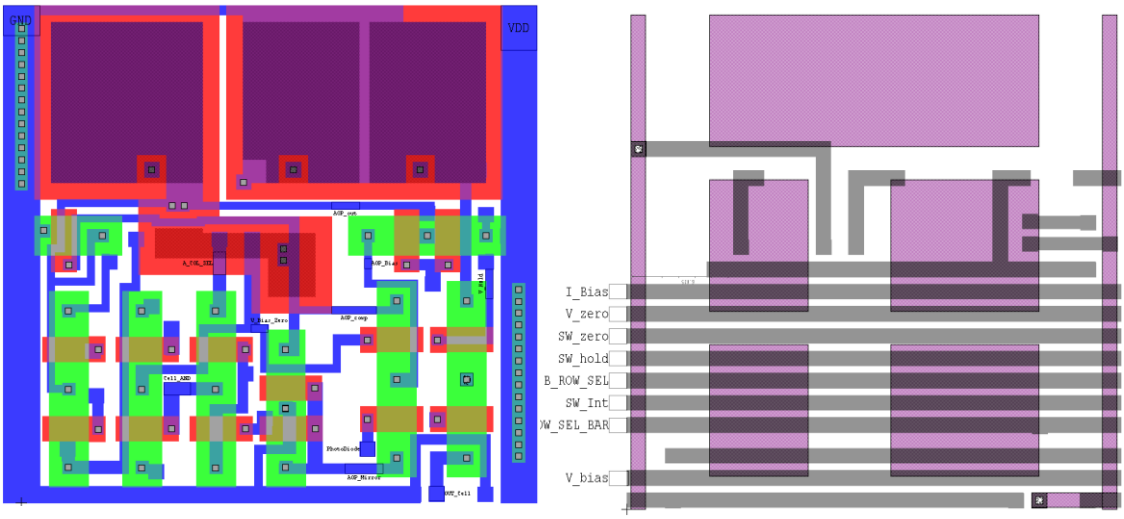


Figure 3.28. Dislocated (top), flipped (midle), and overlapped columns (bottom) for 100% fill factor FPA.

3.15. Final design

The unit cell was designed with 17 transistors with a minimum width/length feature size of 2.36/1.5 μm/μm and three poly capacitors (Figure 3.29 a) to fit in a 30 x 30 μm^2. The power grid is distributed by vertical grids. Eight horizontal and two vertical lines conect the input/output signals (Figure 3.29 b). The ITP-ROIC final layout of the chip is shown in Figure 3.30.



(a) (b)

Figure 3.29. Unit cell main layers layout (a) and signals connections (b).

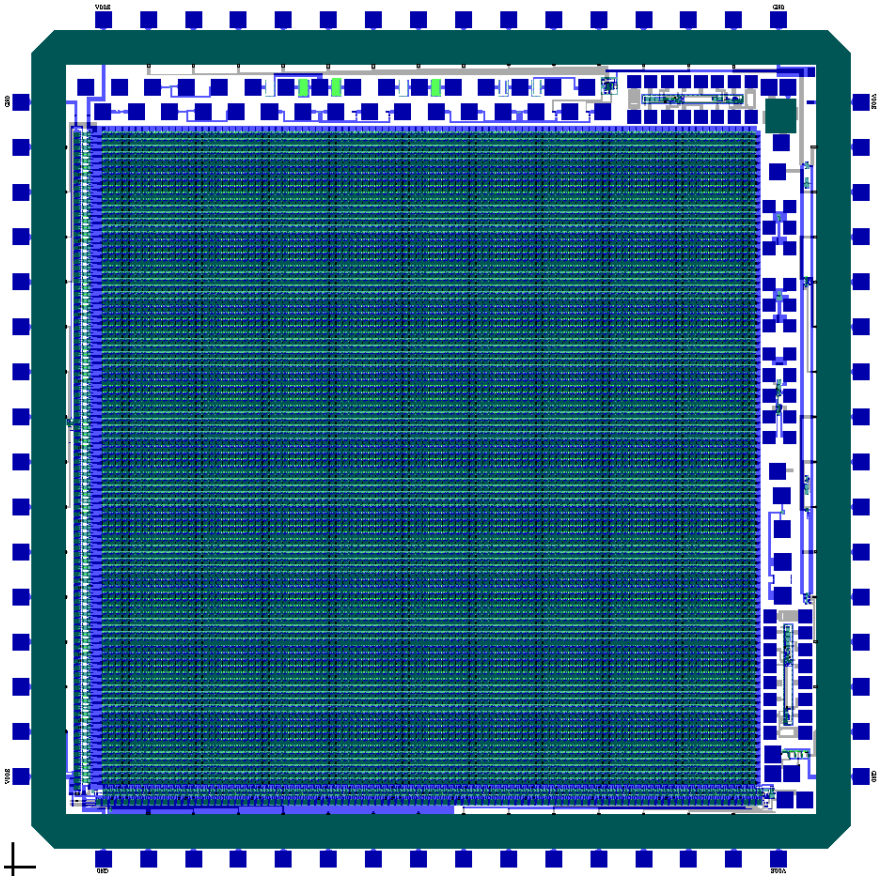


Figure 3.30. ITP-ROIC final chip layout.

Chapter 4

Test system hardware

The actual hardware system (Figure 4.1) operates with a minimum of one rotary switch and five push buttons, already onboard, together with the LCD display on a context menu, maximizing its functions and operation but allowing external boards to be added, offering up to 16 inputs for optional configurations and/or parallel operation of push buttons, slide switches, and rotary switches.

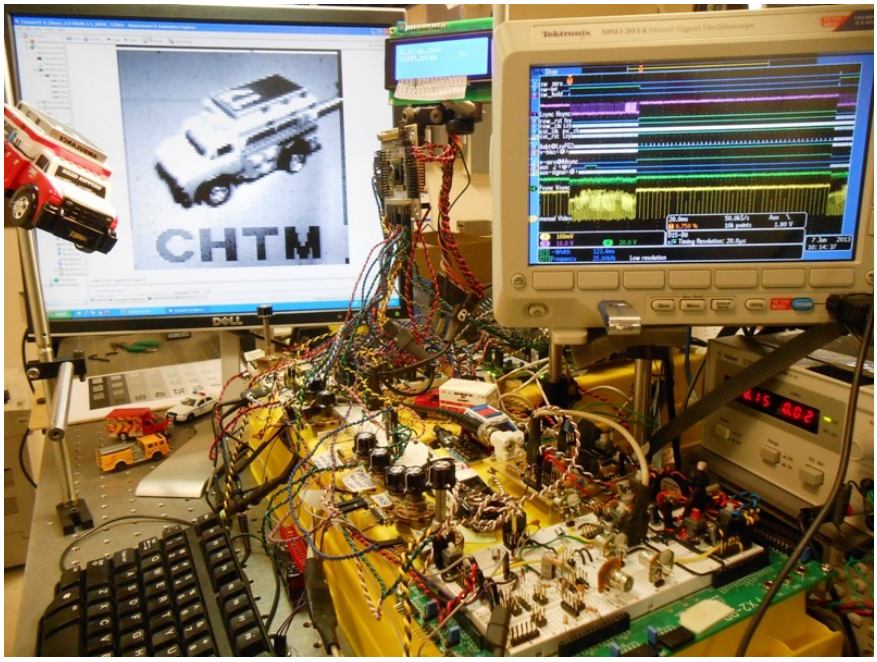
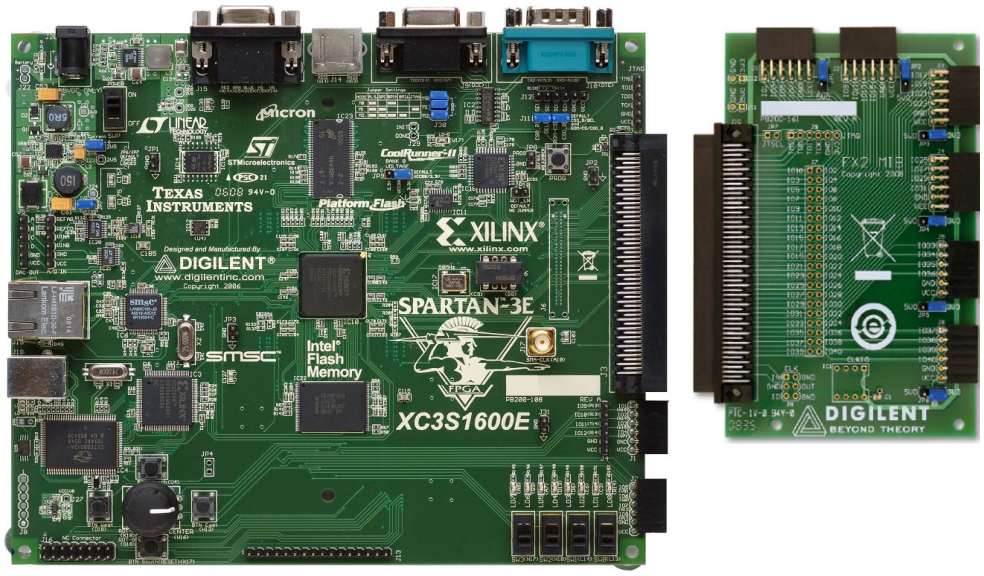


Figure 4.1. Actual version of the test and characterization system hardware.

4.1. FPGA board

Several analog and digital signals are necessary for generation so that the ITP-ROIC can be tested. For the hardware main control system, a MicroBlaze Development Kit Spartan-3S1600E from Xilinx [18] was chosen because of its low cost [19], stand-alone characteristic, key features for signals generation, image acquisition and storage, as well as for processing and display (Figure 4.2 a). It presents 1,600k gate Spartan 3E, 50MHz

of clock generation, 64 Mbyte x 16 bits DDR SDRAM, 16 Mbits SPI serial Flash, 4 outputs serial peripheral interface-based (SPI) 12 bits digital-to-analog converter (DAC), 2 input SPI-based 14 bits 1.5 Mega samples per second (MSPS) analog to digital converter (ADC), 2 lines x 16 characters liquid crystal display (LCD) display, VGA display port, 10/100 Ethernet PHY, two 9-pins RS-232 ports, PS/2 keyboard, 10 switches, 8 LEDs, 12 digital high-speed IO pins, among others features. This board also has a 100-pin Hirose FX2 connector, in which an FX2 module interface board (MIB) was connected [20], expanding the system with more 32 high-speed IO pins (Figure 4.16 b).



(a) (b)

Figure 4.2. Spartan 3E-1600 board (a) [18], and FX2 module interface board (b) [20].

4.2. Power supply and safety interlock

The main power supply with an adjustable current limit was set to 18 V and supplies several LM317 [21] for regulation of 15 V, 7.5 V, 5 V, 3.3 V, for which typical application circuit and features are shown in Figure 4.3. Also, -5 V was supplied. An intermittent beep circuit on the power supply and blinking LEDs were implemented to

remember to turn off the power supply when no more tests were necessary. Additionally, a safety interlock circuit senses the power supply voltage, sending a digital signal to the FPGA board as a feedback for the software to turn off the generated signals, avoiding control signals on test circuit when the power supply is off.

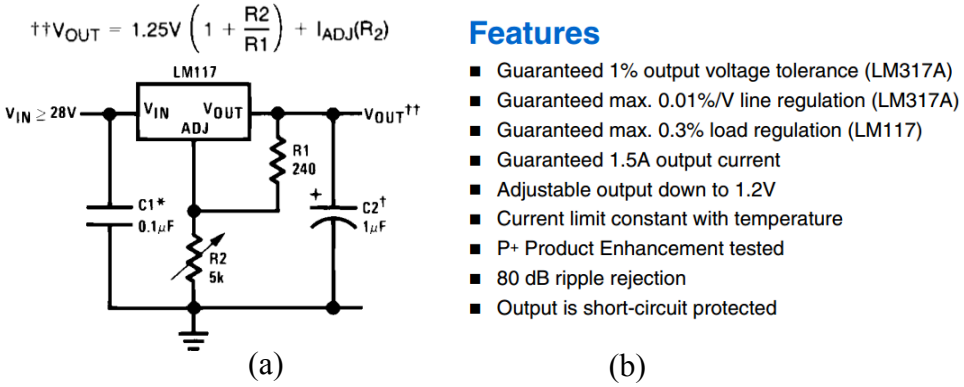


Figure 4.3. LM317 typical circuit application (a) and regulation features (b).

4.3. Digital inputs/outputs

The main board has four slide switches, five push buttons, one rotary switch, as illustrated in Figure 4.4, which are used for system reset, for selection of screens on LCD, for adjustment of parameters, and for internal selection of test circuits via a context menu. In addition, the main board provides 12 high-speed IOs, of which four are used as output for the frame grabber synchronization signals, and eight are used as extra input for testing

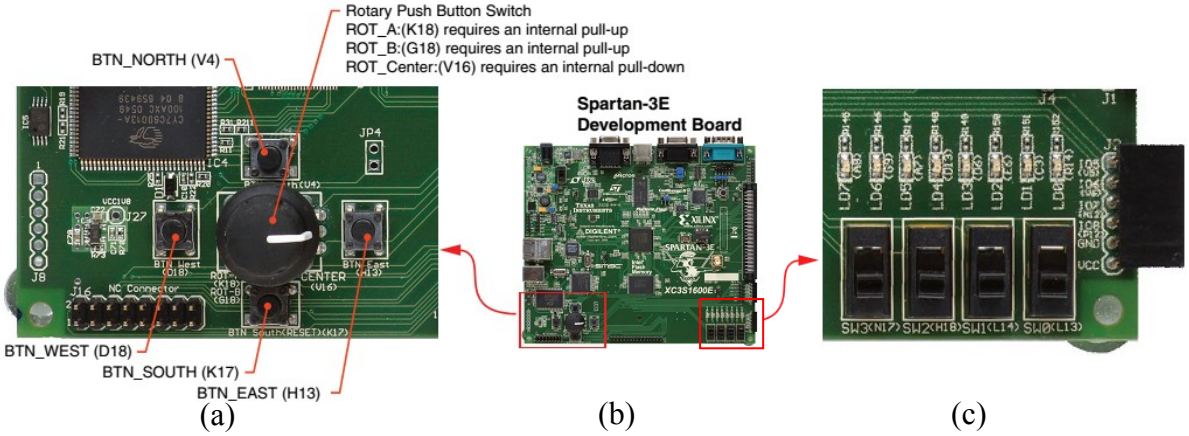
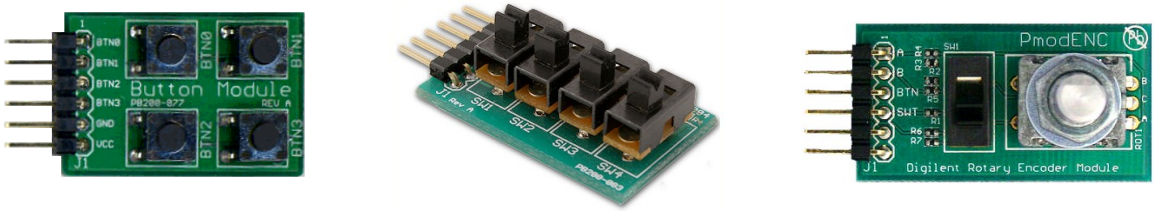


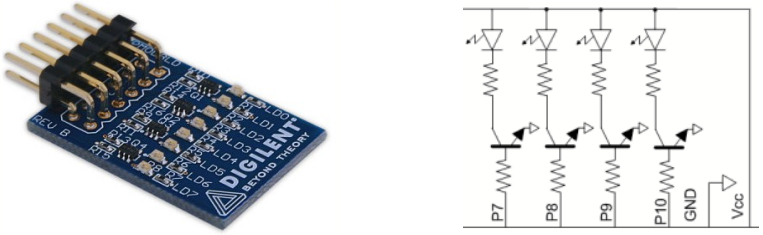
Figure 4.4. Push buttons and rotary switch (a), main board (b), and slide switches (c) [18].

On the module interface board (MIB), in use are 22 output control signals, two digital inputs, and eight inputs for testing push buttons and slide switches, comprising 32 IOs. External dedicated modules (Pmod) were used as input for push buttons, slide switches, and rotary switches, as shown in Figure 4.5. In addition, all outputs have Pmod buffered LEDs (Figure 4.6), which help the visualization of events of low frequency, such as the frame signal.



(a) (b) (c)

Figure 4.5. Pmod push button (a), slide switch (b), and rotary switch (c) [22].



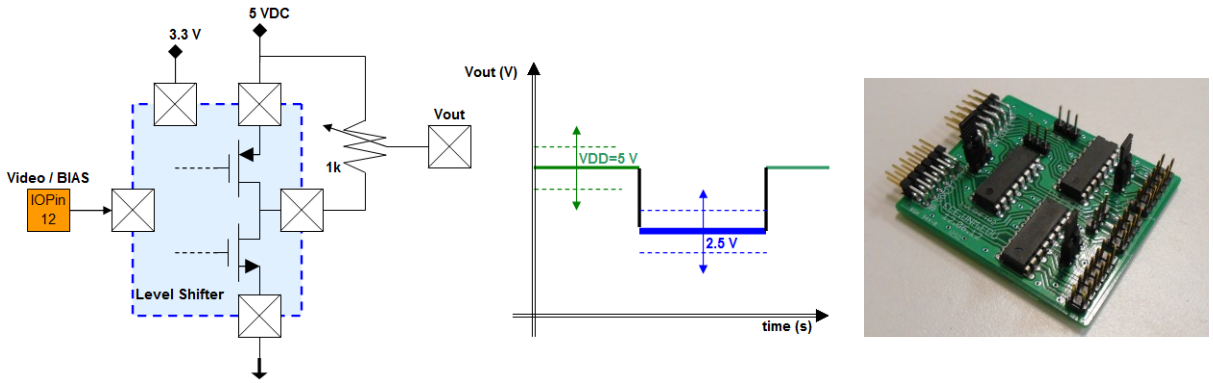
(a) (b)

Figure 4.6. Pmod LED (a) and buffer circuit (b) [22].

One digital input on MIB receives the synchronization signal from the mechanical laser chopper in TTL level, and a resistive divider is used to reduce the 5 V pulse originated from this signal to the 3.3 V of the FPGA input. For the unit cell testing procedure, the chopper generates the starting signal for a sequence of pulses synchronized with the laser light.

4.4. Digital output level shifter

A CD4504B [23] has been used for the digital level shifter, which converts the 3.3 V of the FPGA board to 15 V on digital control inputs of the FPA, such as the SW-REF, SW-INT, and SW-HOLD. In a like manner, the level shifter with associated circuitries was used for maximum and minimum output-voltage level control for the individual pixel BIAS, as illustrated in Figure 4.7.



(a) (b) (c)

Figure 4.7. Digital level shifter circuit (a), voltage levels control (b), and designed PCB (c).

4.5. Electronic switch

A high frequency electronic switch [24] controlled by an SW_INT signal opens the circuit to V-BIAS to avoid an internal short circuit with V-REF on some nonstandard operation tests, as illustrated in Figure 4.8 (a). Another electronic switch controlled by a "clamp" signal generates an adjustable reference value during the start of line (Figure 4.8 b), to define the black level of the acquired image, which is essential for the correct operation of the low-cost AC-coupled adopted the frame grabber.

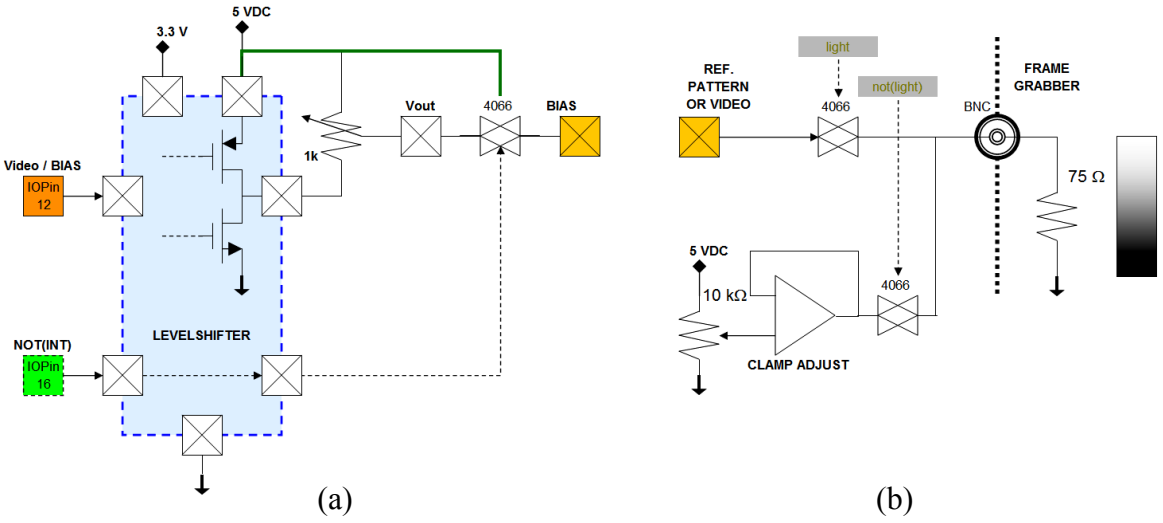


Figure 4.8. Safety electronic switch for BIAS (a) and clamp reference value switching (b).

4.6. DAC

A digital-to-analog converter (DAC) on the Spartan 3E board was used to generate specific voltage values and ramp waveforms. An operational amplifier was used to adapt the DAC voltage range of 0 V to 3.3 V to the necessary voltage range 0 V to 15 V.

Complete knowledge and domain over the functionality of the DAC, with the precise control of the bias voltage value on each pixel at its clock timing, was essential for the main ITP-ROIC feature. Furthermore, the ramp generation allowed clock feedthrough analysis on the gate of the transistors and allowed individual voltage definition that permits future on-system image processing, and also allowed fixed pattern-noise (FPN) compensation and nonuniformity correction (NUC) on acquired images.

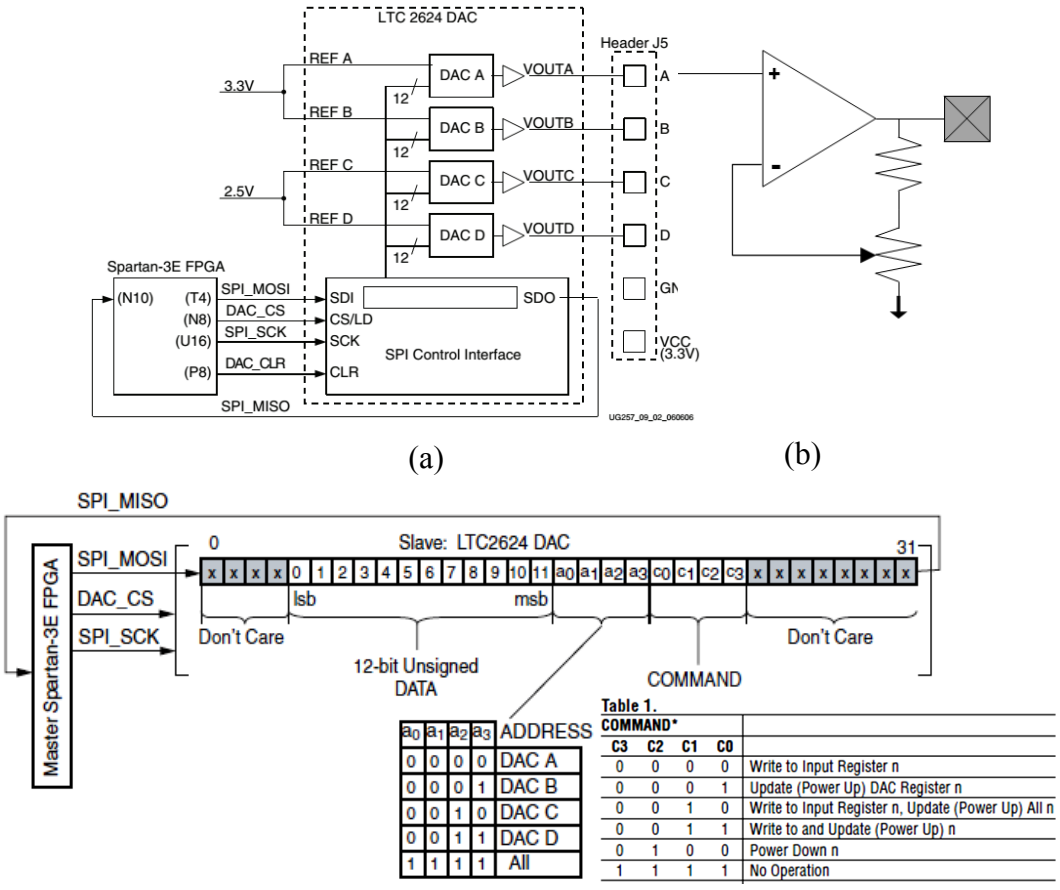


Figure 4.9. DAC block diagram (a), analog level adapter (b), and DAC serial coding (c) [18].

The DAC presents a word depth of 12 bits, which means 4,096 levels of 805.664 µV over the 3.3 V end of scale. Seeking a match of numbers in the simplest way, without losing resolution, a counter 0 to 3,000 was defined instead of a counter 0 to 4,095, on a voltage range of 15 V, resulting in 5 mV of resolution per step (0.033%). This end-of-counting number (3,000) generates 2.416992 V on DAC output and required a gain of 6.206060 for the operational amplifier. On the other hand, it was necessary to match the pixel frequency and correlated bias writing frequency, with the necessary number of clock pulses to program the serial DAC. The serial DAC needs a minimum of 24 clock pulses to write the command, the address, and the value into one converter. So, it was decided to

use 100 clock pulses to program the four DACs at the maximum frequency of 50 MHz, resulting in 2 μs of resolution (conversion time), meaning 500 kHz of pixel clock. For 10,000 pixels (near 98 x 98), the minimum time for writing all biases is 20 ms. Considering the maximum of 245 ms of integration time, the frame time is 265 ms, resulting in 3.78 FPS minimum, sufficient for live video testing.

4.7. Analog output level shifter

Similar to the DAC output signal conditioning block, an analog level-shifter circuit was implemented to change the output voltage range from the FPA (5 V to 12.8 V) to the input voltage range of the frame grabber (0.3 V to 1.4 V). Figure 4.10 illustrates this signal conditioning. The start of the FPA output range is subtracted, then a gain adjust is applied to match the voltage ranges, and finally a start-of-scale value is added to adjust the black level on the frame grabber.

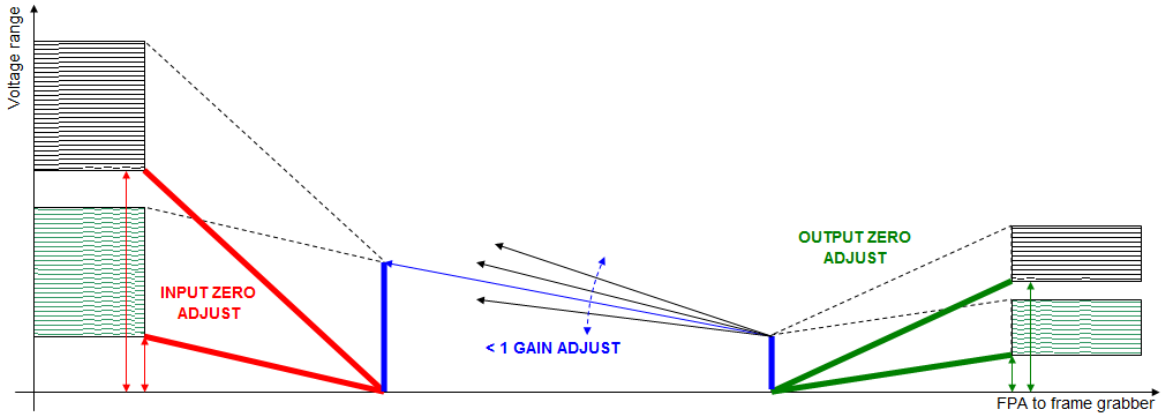


Figure 4.10. Analog-level shifting illustration.

This interface permitted a basic and quick calibration, necessary to achieve a better contrast response on the acquired images at local illumination. Using V-BIAS = 2.5 V for all pixels, the lenses are covered to create a dark image and to adjust the zeros on both interface and frame grabber. With a white carton positioned at a focal point of

approximaly 50 cm, the span (gain) is adjusted for the maximum reflected light from the diffuse incandescent illumination.

4.8. Signal buffer

TL082 opamp [25] has been used as a buffer to increase the impedance of oscilloscope probe, from 10 MΩ to 1 TΩ. It is important to realize that the measurement of 1 V of BIAS over the photodiode of the unit cell can drain 100 nA by the normal 10 MΩ of oscilloscope's input impedance. As illustrated in Section 6.1, the photodiode generates only 0.1 nA of current at room illumination, and in this way, the oscilloscope measurement quickly saturates the CTIA integration. The same 1 V over 1 TΩ of the buffer drew only 1 pA, which is a value 100,000 times smaller and is near the dark current of the photodiode.

This circuit required two separated and uninterrupted connections to the power supplies of 18 V and -5 V to allow measurement of the FPA's operational voltages, which range from 0 V to 15 V.

4.9. VGA output

The Spartan 3E board has a DB15 video graphics array (VGA) standard output-connector (Figure 4.11), which receives signals from five output pins of the FPGA. Three pins are defined for the red, green, and blue (RGB) analog signals, and two have horizontal and vertical synchronization function. As shown in Figure 4.12, the onboard resistors of 270 Ω, combined in series with the 75 Ω termination built into the VGA cable, ensure that the 3.3 V from the LVCMOS33 I/O standard level generates the VGA-specified 0 V to 0.7 V range. With this configuration, eight basic colors can be generated by the 3-bits

word (Figure 4.13) and used for a simple graphic user interface (GUI) in an external monitor for parameters configuration. Moreover, connecting the three signals to the DAC output of this board, 8-bits grey level (256 levels) could be used in an autonomous way to display the acquired image from the FPA, which means no computer, no frame grabber and no third-party software would be necessary to display the image, and the FPGA system would be portable.

Figure 4.11. DB15 VGA connector and pinout [18].

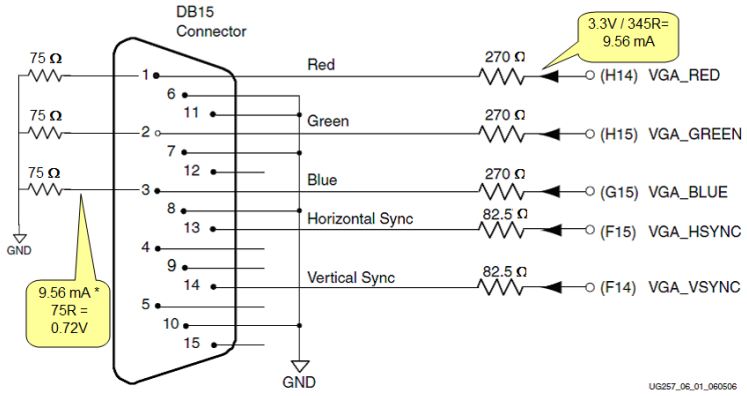


Figure 4.12. Voltage levels for VGA specification [18].

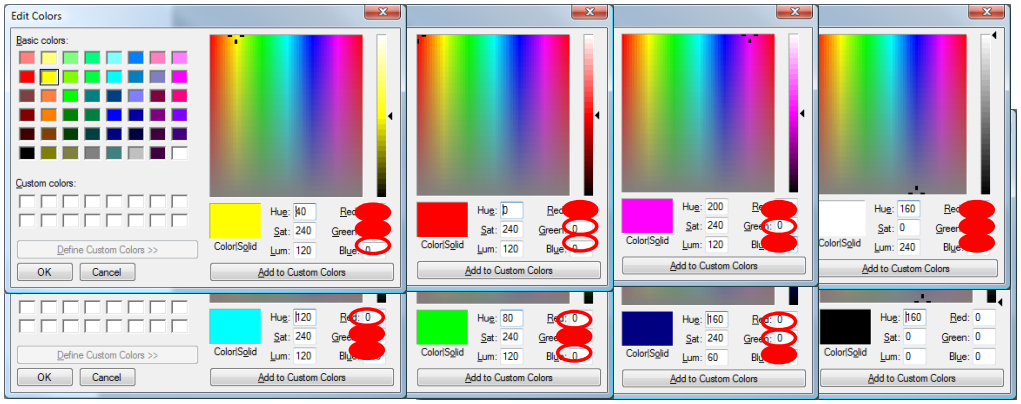
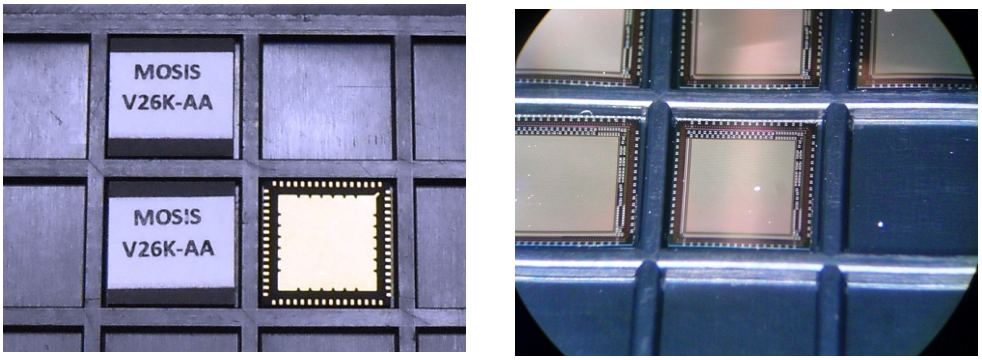


Figure 4.13. Generated colors with 3-bits word on VGA input.

4.10. System interconnections

Forty dies of ITP-ROIC were manufactured and received from MOSIS, five of which came wire bonded on a quad-flat no-lead (QFN) package of 64 pins, at 0.5 mm pitch, and 35 of them came on bare dies (Figure 4.14).



(a) (b)

Figure 4.14. ITP-ROIC QFN package (a) and bare dies (b).

4.10.1. QFN package PCB

The QFN packages were soldered on commercial PCB adapters for SMT devices [26], together with the 0.1" (2.54mm) straight-header male pins [27] for cable connections, as illustrated in Figure 4.15, where one also can note the flipped design image for pinout. Although this option offered a die connection with a ready, professional wire bonding, the necessary manual soldering process was found to be more difficult than expected due to the small dimensions of the package. In addition, in the case of damage to the chip, all the material and time invested on this PCB manufacturing would be lost. Furthermore, in this package we have access only to the main signals of the design, and the test structures with internal pads would be useless.

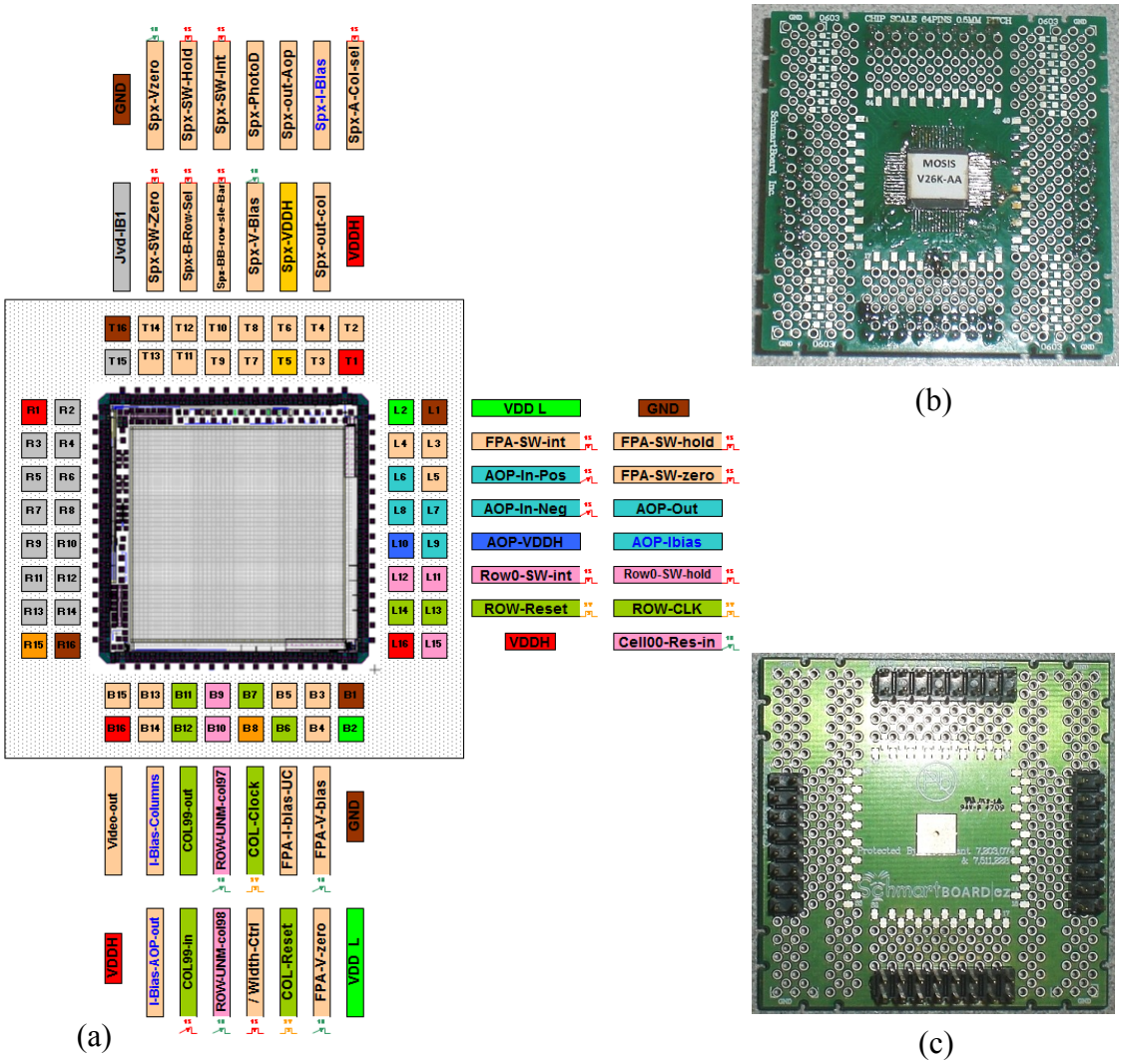
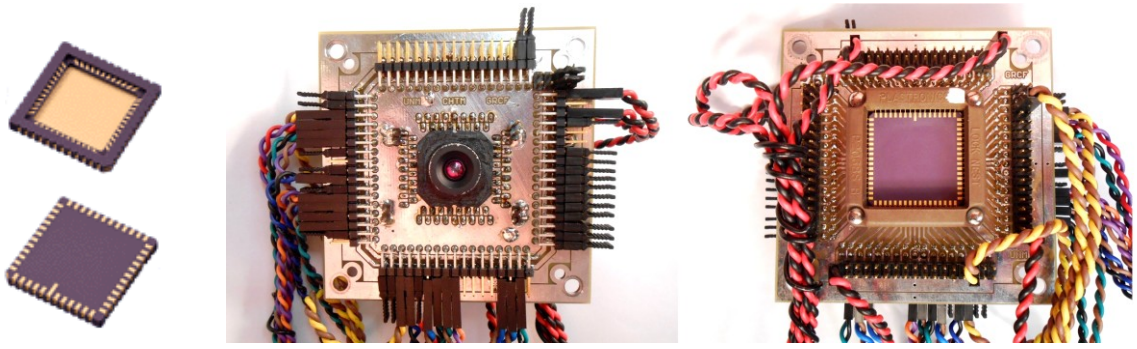


Figure 4.15. PCB for QFN package pinout (a), top (b), and bottom view (c).

4.10.2. LCC carrier PCB

The bare chips were mounted and wire bonded to a 0.4 x 0.4" (10.16 mm^2) open-cavity leadless chip carrier (LCC) package of 17 x 17 pins, with a lead pitch 0.050" (1.27 mm) [28] (Figure 4.16 a) for use with zero insertion-force (ZIF) sockets [29] on a specifically designed PCB as shown in Figure 4.16 (b-c). On the front side of the socket PCB, 0.1" (2.54 mm) right-angle header male pins [30] were mounted, permitting cable connections with minimum interference on the front path, necessary for illumination access to the

chip. The back side has straight pins, with the same connections as the front side, permitting not only cable attachment but the connection of this board on level-shifter boards or on signal-buffer daughter boards.



(a) (b) (c)

Figure 4.16. LCC carrier (a), specific designed PCB, front (b) and ZIF socket on back (c).

The header pins on both sides of the board can receive jumpers [31] dedicated to ground connection where necessary. The interconnection cables were made with pre-crimped wires with female terminals, twisted with the ground wire to minimize noise generation and terminated on a 0.1" (2.54 mm) crimp connector housing [32]. These resources and features constitute a technique that allows great speed and flexibility for establishing a desired test setup for specific characterization. Furthermore, the relative low cost of components permitted the building of several setups for the test structures, including interconnection of different setups.

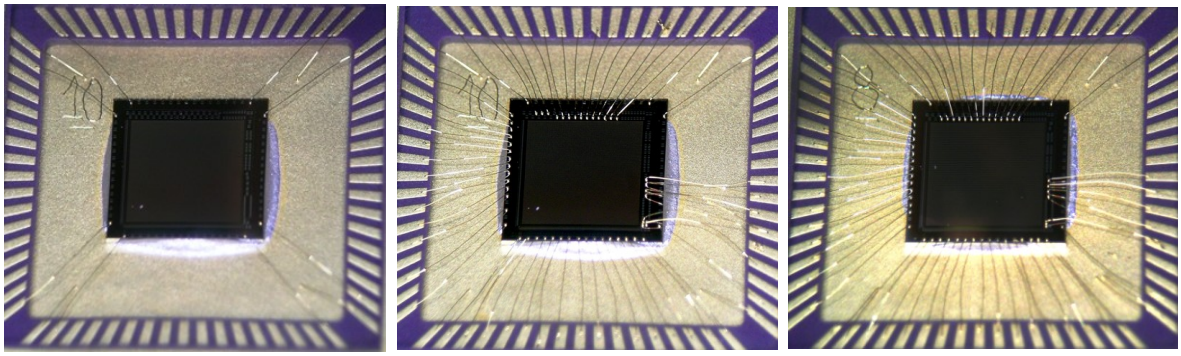
4.10.3. Wire-bonding

As explained earlier, it was decided to wire bond the dies on a 68-pins LCC package and to use sockets on specifically designed PCB for the carrier. This permitted, without the limitation of external pads and packages, the design of a great number of internal test structures. The wire bonding was executed on a semiautomatic wire-bond station,

illustrated in Figure 4.17.

Figure 4.17. Semiautomatic wire-bond machine.

Initially, the backplane of the carrier that is attached to the die substrate by a conductive glue is wire bonded to a specific carrier pad. Next, the ground and VDDH are wire bonded, as shown in Figure 4. (a). Finally, the FPA, test transistors, and test photodiodes are wired, as shown in Figure 4. (b). One can note the numbering on the backplane of the carrier for die tagging (Figure 4. a-c).



(a) (b) (c)

Figure 4.18. Wire bonded ground and VDD (a), die 10 (b), and die 8 (c).

Illustrated in Figure 4.19 are the pinout of ITP-ROIC FPA, separated unit cell (top), ESD-pad (right side, top), photodiodes (right side, bottom), and bias transistor (right side, center).

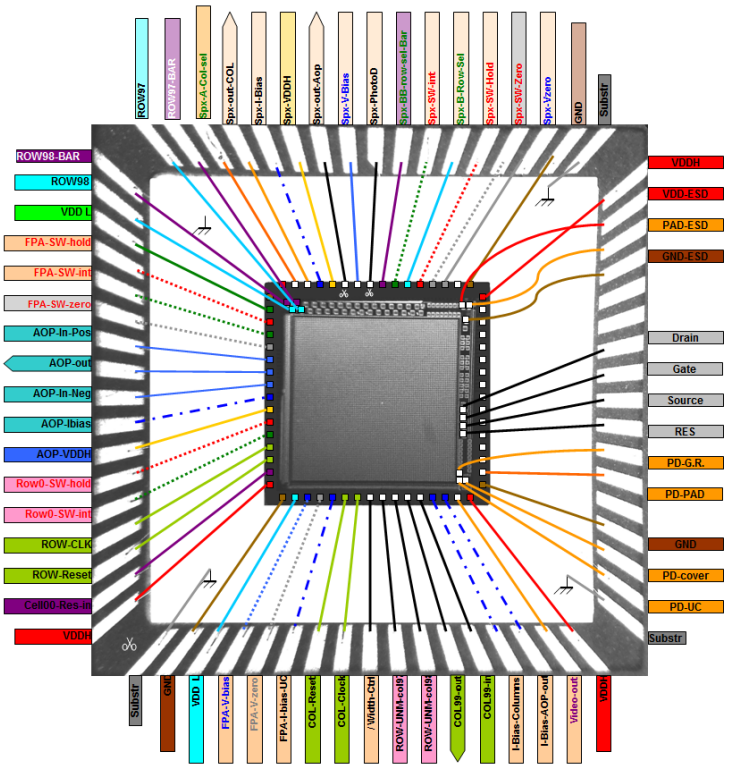


Figure 4.19. Pinout of ITP-ROIC FPA and test structures version 1.

4.11.LCD

The two-line, 16-character liquid-crystal display (LCD) module is driven by a Toshiba HD44780 controller chip, and has well known hardware connections and control commands [33], as illustrated in Figure 4.20.

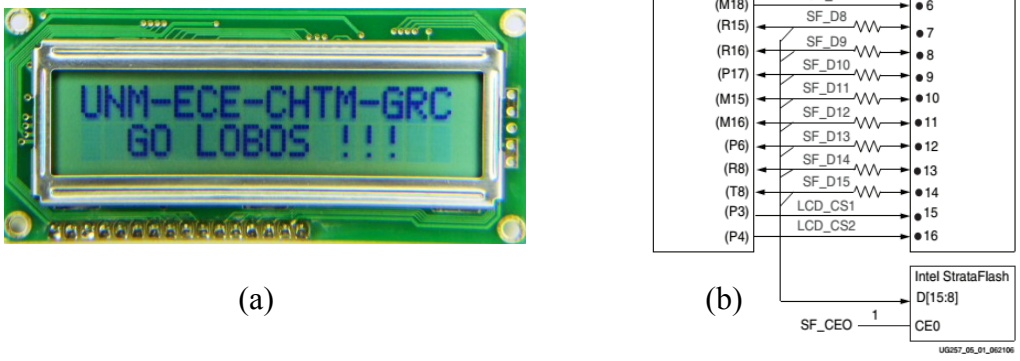


Figure 4.20. LCD initial screen (a) and pinout (b).

4.12. Infra-structure hardware

Several instruments and equipments were required for the measurement, testing, and characterization of devices, circuits, and system. In addition to the basic bench instruments, such as power supplies, a soldering station, a multimeter, a function generator and an oscilloscope, specialized instruments and software were used in ITP-ROIC operation, testing, and characterization, such as a probe station, a wire-bonding machine, a source-measure unit, a laser light, an energy meter [34], and frame grabber. These main resources are discussed below.

4.12.1. Oscilloscope

Initially, a four-channel oscilloscope was used [35], but as the number of digital signals increased substantially, a 16-channel digital input, four-channel analog input mixed-signal oscilloscope was specified for purchase [36]. The main signals for synchronization, separated unit cell, and FPA control were kept on screen while four digital channels were used with dedicated pins from the FPGA board to visualize any desired internal signal waveform by means of its own FPGA software selection.

4.12.2. Probe station

The Signatone S-251-6 probe station with PSM-1000 microscope [37], shown in Figure 4.21, proved to be a useful tool for quick access, measurement, and I-V curve characterization of individual devices. Three new probes were specified and purchased for the characterization of the symmetric transistors. Unfortunately, care must be taken with the probes, because, even with pressure control and limitation, some damage can occur to the pads, and therefore, the number of measurements on each point might be

limited.

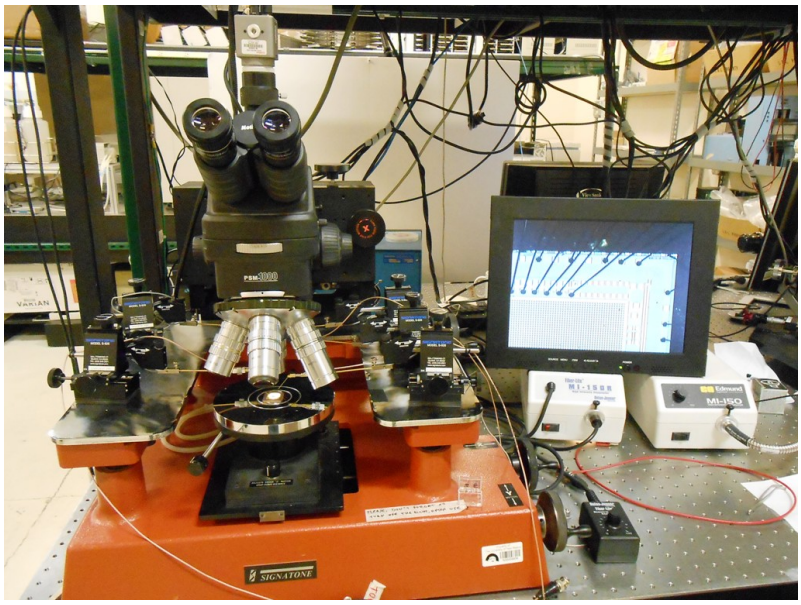


Figure 4.21. Probe station with integrated video camera to monitor and to computer.

This was one more justification for the using the wire bonding procedure on the chip carrier and socket PCB, even though it was more time consuming and costly and required training and experience.

4.12.3. Video camera and software

To promote a fast, easy way of image documentation of devices and structures analyzed on the probe station, a video camera and image-acquisition software were priced, purchased, and installed [38]. The control interface, video, and file-manipulation windows are shown in Figure 4.22. This newly implemented resource on the Midinfrared Image Characterization and Application Laboratory (MICA) lab also allowed the image from the microscope to be viewed on a monitor, thus offering a way to view simultaneously the region of interest, to follow the procedures, and to learn about the measurement and characterization processes.

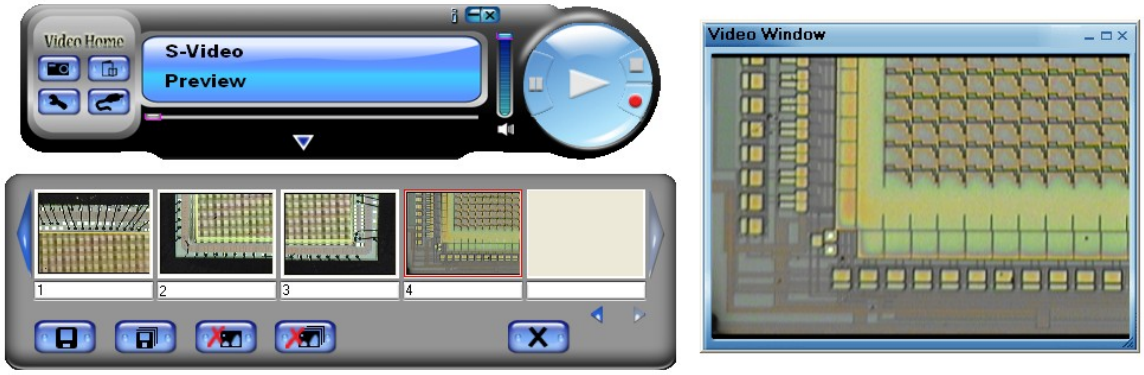


Figure 4.22. Grabee software for image and video acquiring from video camera on probe station.

4.12.4. Source-measure unit

"A current-voltage characteristic or I-V curve (current-voltage curve) is a relationship, typically represented as a chart or graph, between the electric current through a circuit, device, or material, and the corresponding voltage, or potential difference across it." [39]. It is essential to know the operational specifications of the finger CMOS diodes on internal pads, which are designed to protect the chip against electrostatic discharge (ESD). The intent is to recognize the functionality of the finger CMOS diodes and their influence on input/output signals. This allows one to determine its leakage current, its reverse breakdown voltage, its direct threshold voltage, and its correlated draw current. For this measurement, Keithley 236 [40]was used as an I-V curve device, and LabView was used as a software interface to control its parameters via the IEEE-488 interface. Figure 4.23 shows the circuit diagram of this measurement procedure, and Figure 4.24 shows the parameters' adjust screen, as well as the block diagram, which was adapted to allow the adjustment of output current up to 100 mA.

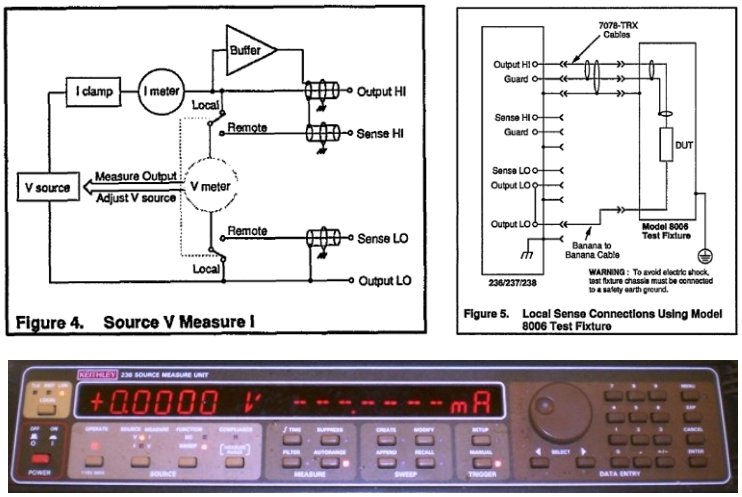
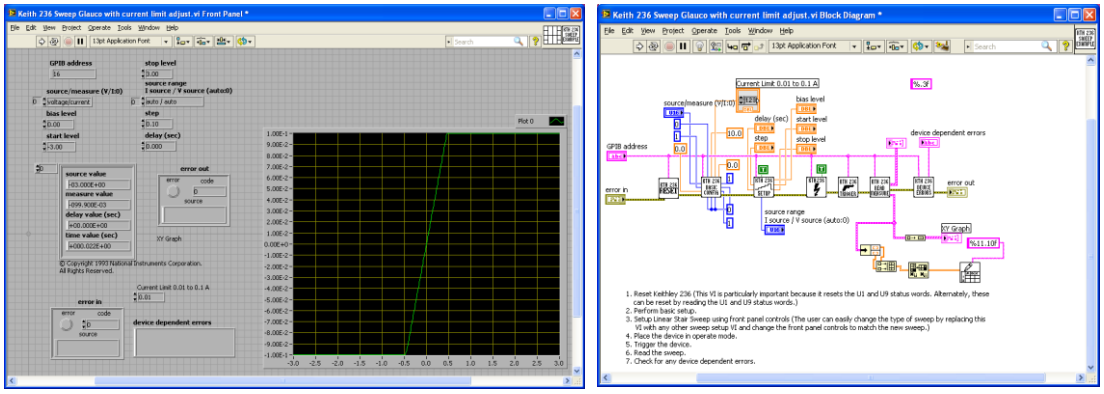


Figure 4.23. Keithley panel and I-V measurement circuit diagram [40].



(a) (b)

Figure 4.24. NI-LabView GUI for Keithley parameters' adjust (a) and its block diagram (b).

4.12.5. Laser

Intending to characterize the photodiodes and separated unit cell, a stable, well-known intensity and wavelength light must be applied on a specific sensitive area. Selected was the Melles Griot 05-LHP-141 Helium-Neon Laser, which generates a polarized light with a wavelength of 632.8 nm, a beam diameter of 0.8 mm, and 4 mW (Figure 4.25). An electromechanical chopper, with adjustable frequency from 4 Hz to 4,000 Hz, was used to interfere on the laser path so that the influence of environmental response could be compensated.

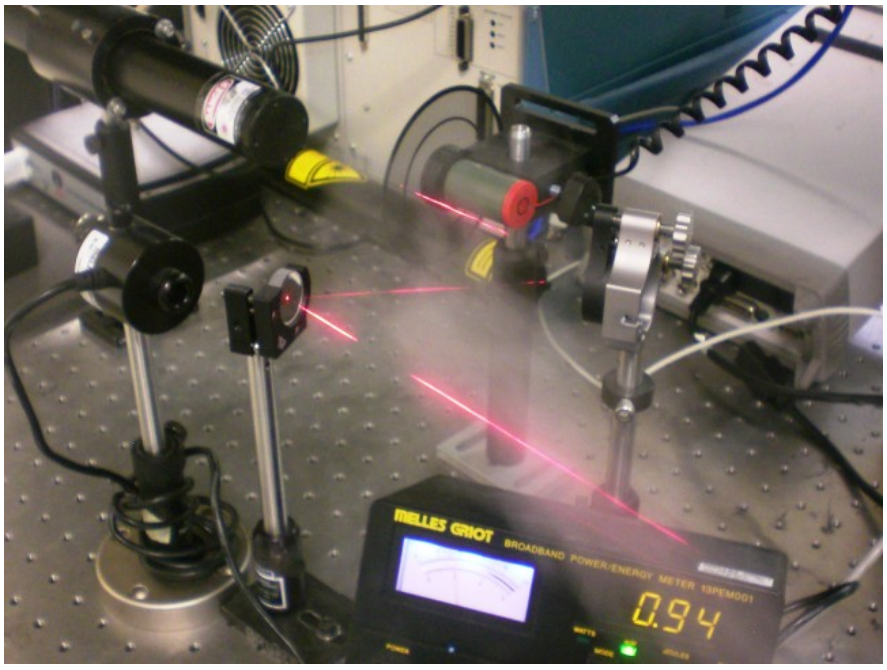


Figure 4.25. Laser setup for electro-optical response characterization.

4.12.6. Optics

Two types of measurement using the laser were considered: a uniform light distributed over all of the FPA and a light beam concentrated on the photodiode of the unit cell. With the size of the FPA being 3.92 x 3.92 mm^2, a circular light beam will be 5.5 mm in diameter with uniform distribution. In the same way, a 5 x 5 μm^2 photodiode of the unit cell requires a circular beam 7 μm in diameter. A desired beam of 5.5 mm in diameter means a magnification of 6.89 in relation to the 0.8 mm-diameter of the laser. Choosing the first plano-convex lens with a focal distance of 25.4 mm (lens 1 in Figure 4.26), and using this magnification, the second plano-convex lens results in a focal length of 175 mm (lens 2 in Figure 4.26). Aiming to use this same optics structure to generate the 7 μm, and considering that a 7 μm focal length lens is difficult to purchase or position, a practical and creative option was to use another 175 mm focal-length lens–in a quick-

release magnetic mount–(lens 3 in Figure 4.26) to focus the 5.6 mm diameter collimated beam at 175 mm of distance.

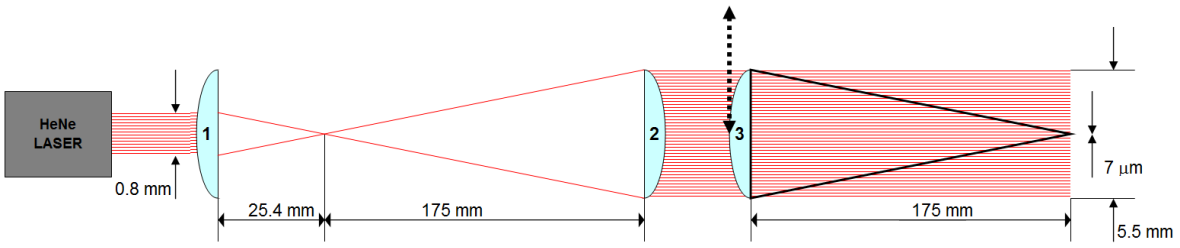


Figure 4.26. Laser optics specifications.

A 30 mm cage plate structure was used to allow automatic alignment of the beam and to facilitate the alignment verification using hanging targets with a 0.9 mm pinhole. Figure 4.27 shows the beam chopper, intensity control, optics input alignment point, and lens tube–for focal distance adjust–of the 5.5 mm diameter beam.

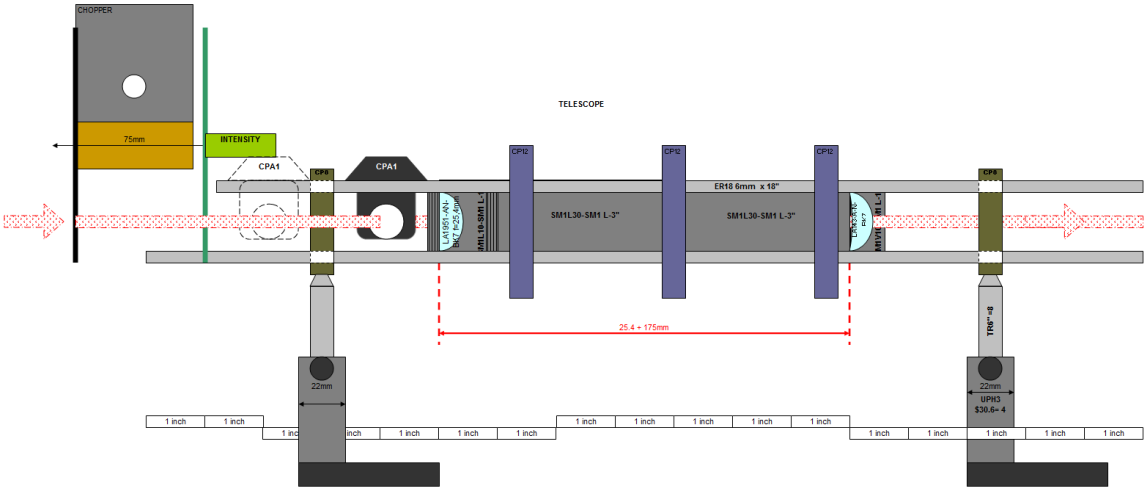


Figure 4.27. Laser optics setup input.

Figure 4.28 illustrates the cube beam splitter inserted to permit a video camera and respective magnification optics (shared from another probe station) to visualize the x-y-z micro positioning of the 7 µm-diameter beam over the photodiode of the pixel. The light energy will be measured with the insertion of the power-meter sensor in the beam path

immediately in front of the FPA under testing, and a second beam splitter facilitates the light power monitoring. The same rods, cage plates, posts, and post clamp were designed to hold the FPA under testing on the micrometrical positioning system.

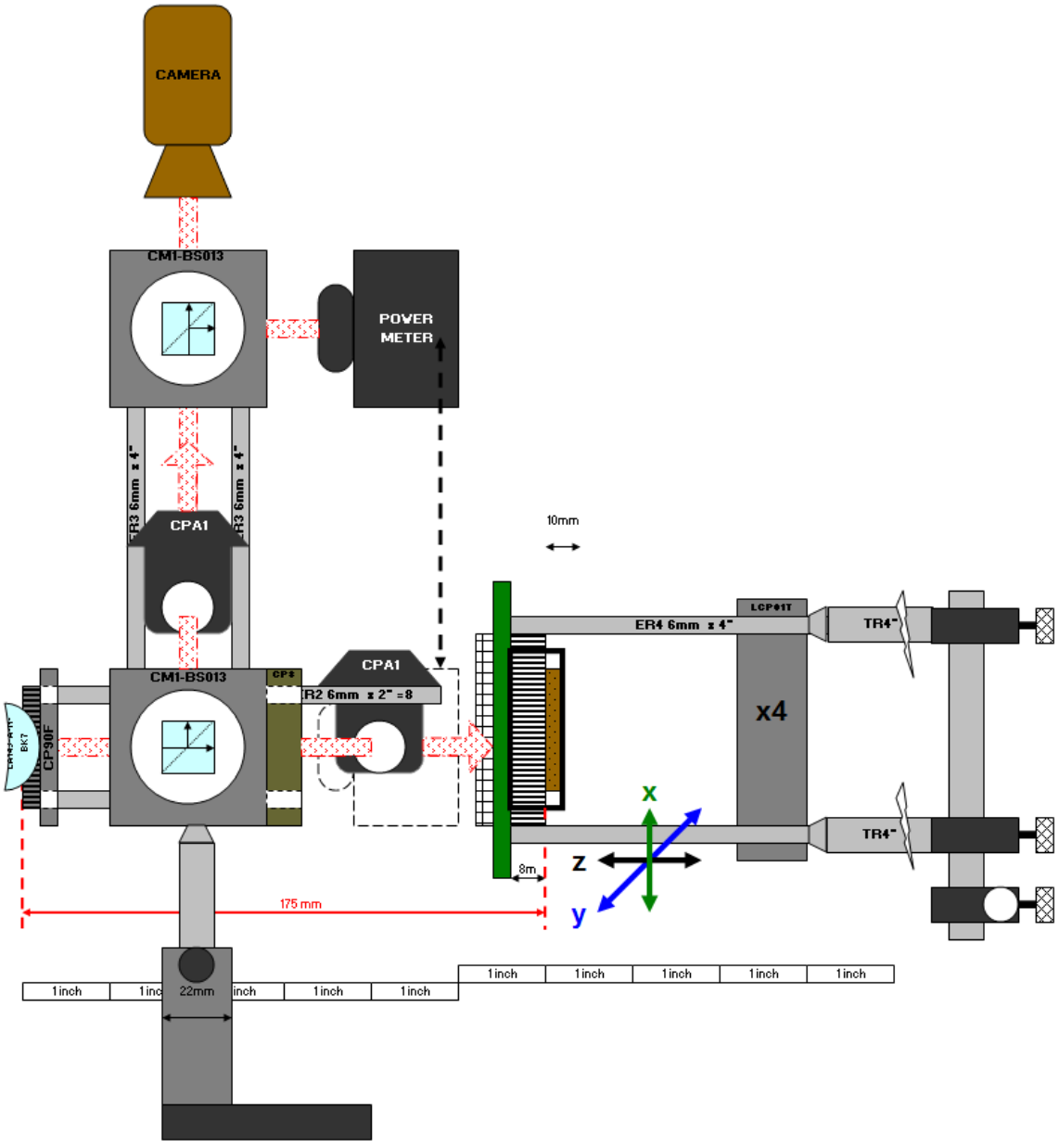


Figure 4.28. Laser optics setup output.

Chapter 5

Test system software

The VHDL-based software has 26 main digital output signals (Table 5.1), with 87 adjustable parameters used for the testing system. The 856 digital, vector, and string-type signals were created during the development, and any of them could be driven, as necessary, to the 26 physical signal outputs. Due to the nature of VHDL language and the FPGA structure, the software blocks easily resemble hardware blocks and are detailed as follows:

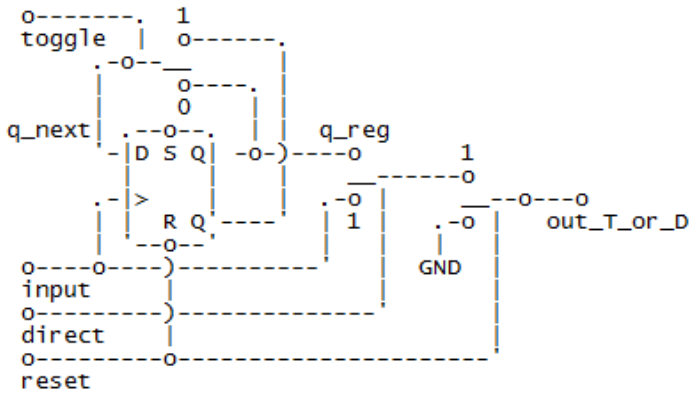
Sync	Unit cell	UC and FPA (shared)	FPA	Auxiliary	Frame grabber
Pixel_clock	**ROW_sel**	**SW_zero**	ROW_RST	**EXT_SYNC**	Clamp_size
Sub_clock	**ROW_sel_BAR**	**SW_hold**	ROW_PT	**Light**	**Lsync_FG**
Msync	**COL_sel**	**SW_bias**	COL_RST	**V_test_line**	Image_bias
Fsync	**SW_INT**	**V_zero**	COL_PT	**H_test_line**	
Lsync		**V_bias**	**Width_ctrl**		

Table 5.1. Digital outputs, related internal signal names, and pulse-generated signals (bold).

5.1. Digital inputs conforming

It was necessary to use a routine for debouncing the signal from the push buttons, slide switches, and rotary switches, avoiding in this way unintended signals or incorrect counts from the mechanical bouncing of the contact on these devices. This function starts to count the clock pulses when the input changes its state and only after a predetermined number of clock pulses, and if the input keeps its state, the output will respond.

A toggle function was developed to allow the use of one push button as a selective switch, operating similarly to the slide switch. The toggle function is a D-type flip-flop with an inverted output feed backed to the data input. In this way, each pulse on the clock input inverts the output. This block has an option to bypass the clock pulse, returning the push button to its original functionality. Also, another input disables the toggle function, keeping the last state as a memory, if necessary.



(a)

```
3732  ---------10--------20--------30--------40--------50-
3733
3734  toggle_east: entity work.toggle(beh)
3735  port map (-- THERE      =>          HERE!
3736           --in-<-<-<-<-<-<-<-<-<-<--out--------
3737           input          =>       east_bt_signal,
3738           reset          =>       SYSRST         ,
3739           toggle         =>       high_level     ,
3740           direct         =>       low_level      ,
3741  --           |     |
3742  --         ___V_____V___
3743  --        [             ]
3744  --        [_____________]
3745  --           |     |
3746  --           V     V
3747           ---out--------->->->->------in---------
3748           out_T_or_D     =>       east_BT_toggled
3749           );
3750  ---------10--------20--------30--------40--------50-
```

(b)

Figure 5.1. Block diagram (a) and instantiation (b) of toggle function.

A versatile device for pulse generation is the rotary switch, the principle of which is a cam connected to a shaft that is used to operate two switches (Figure 5.2). Both switches are closed in the stationary detent position. Then, depending on which way the shaft is rotated, one switch will open before the other. In the same way, continuing the rotation, one switch will close before the other [41].

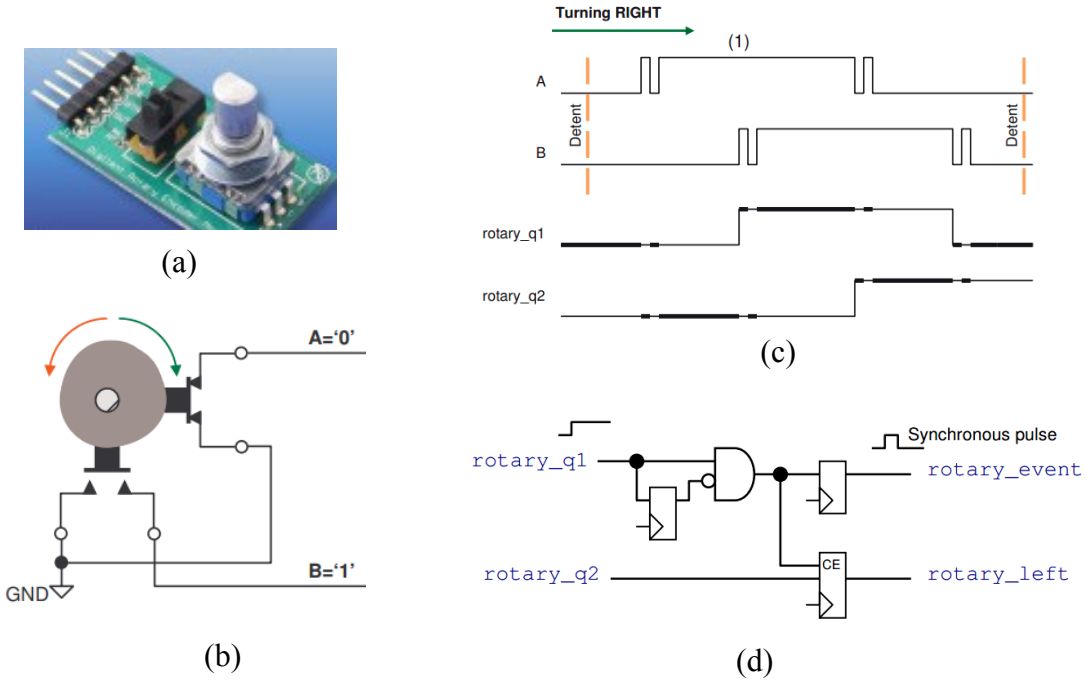


Figure 5.2. Rotary switch (a), cam operation (b), debouncing signals (c), and event pulse and direction (d) [41].

Another digital input receives the signal directly from the 3.3 V power supply and controls an implemented AND-gate on each signal output (Figure 5.11). When the power of the device under test (DUT) is manually turned off, after tests are executed, the FPGA system, which is always on to preserve the programming on RAM memory, automatically turns off all signal outputs as a safety measure except for the oscilloscope synchronization output.

5.2. Parameter up/down counter

One essential characteristic of this test system is that all parameters can be adjusted online and locally. This is crucial to change the waveforms and to allow immediate visual analysis of the cause and effect between the signals and the hardware response.

For each variable that controls one parameter of a signal, a memory was built, based on an up-down counter (Figure 5.3). It is reset upon start-up or manually, in which state the output goes to an initial value that is defined by constants on compilation or is originated by the setup block, as necessary. The minimum and maximum values that can be reached are defined by constants in the compiled program, but they can be defined by other counters, if necessary. They receive the up/down and clock signals from the rotary switch conditioning block, and in this way, the value is automatically increased or decreased according to the rotary switch movement. These counters work closely with the LCD screen selector (Figure 5.8), described in Section 5.6, which enables the up/down counting of pulses from the parameter/value rotary switch. Each counter generates internally a three-character string for displaying the correlated values on the LCD screen based on a double-dabble algorithm [42], which converts the 10-bit binary signal (0 to 1,023) to a 12-bit binary coded decimal (BCD) consisting of three BCD digits (000 to 999).

5.3. Multiplexer

One basic and simple structure used extensively on different applications is the multiplexer, the output of which is selected by an up/down counter. The first application and most simple version is contained in one up/down counter; its output selects a high

level to enable one of the parameter counters, as illustrated in Figure 5.4.

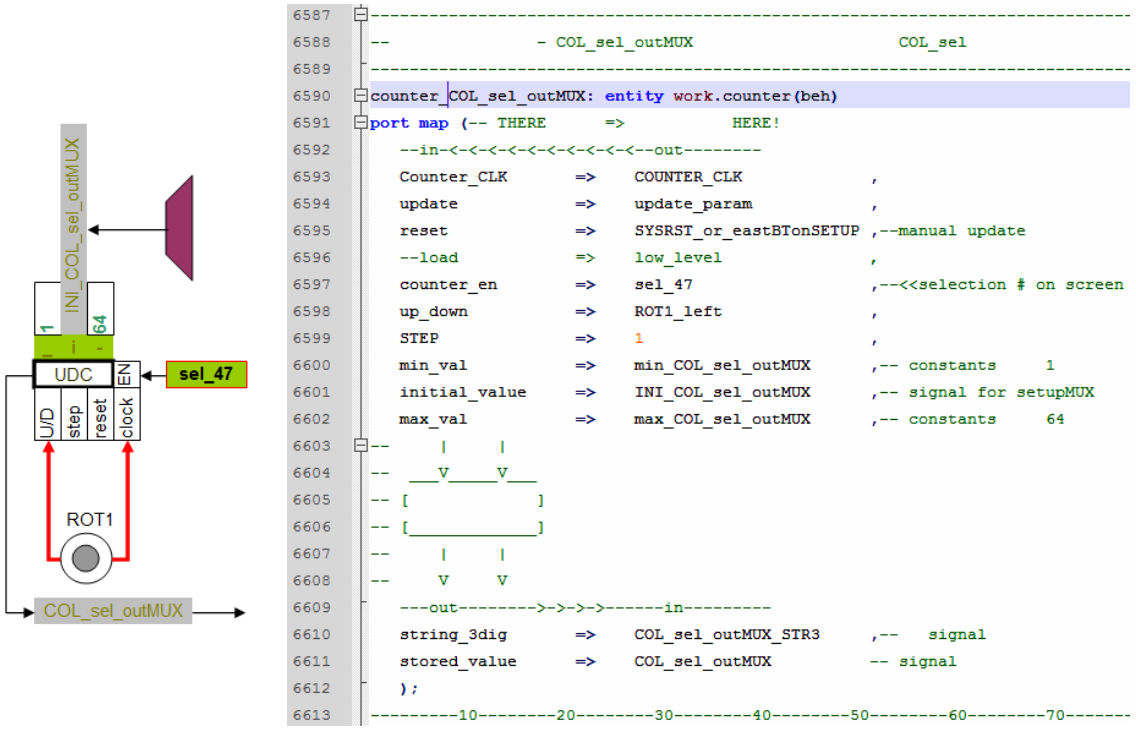


Figure 5.3. Parameter counter block diagram (a) and instantiation (b).

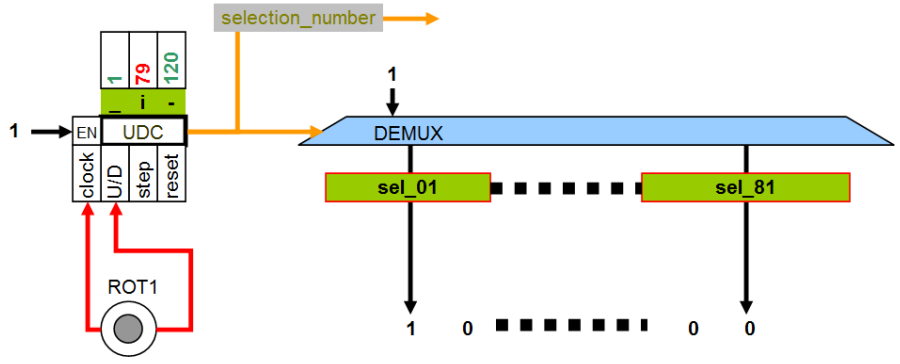


Figure 5.4. Parameter counter selection multiplexer.

One multiplex version, referred to as table mux (orange trapezoid shape), is used to select values that are not direct multiples of one another, where an up/down counter cannot be used, i.e., on clock division (Figure 5.6) and step definition of the ramp counter (Figure

5.16). Others applications of the multiplexer block are the LCD screen labels and variables selection, the setup parameter selection (purple trapezoid), the digital or output signal selection (blue trapezoid), internal signals test switching, and context menu switching, explained with details on following sections. The great advantage of this structure is that it increases its flexibility and that digital signals can be selected along with vectored variables and screen label strings.

5.4. Clocks generation

The pixel clock (Figure 5.5) is an important signal, and its value, together with other factors, defines the frames-per-second (FPS) rate. The pixel clock is generated by the division of the sub_clock (Figure 5.6), which, in turn, is generated by the division of the system clock (50 MHz). The sub_clk is used in the SPI DAC to generate one analog BIAS value at each pixel clock. In addition, multiples of clk_pixel were crated to chopper signals on unit cell characterization.

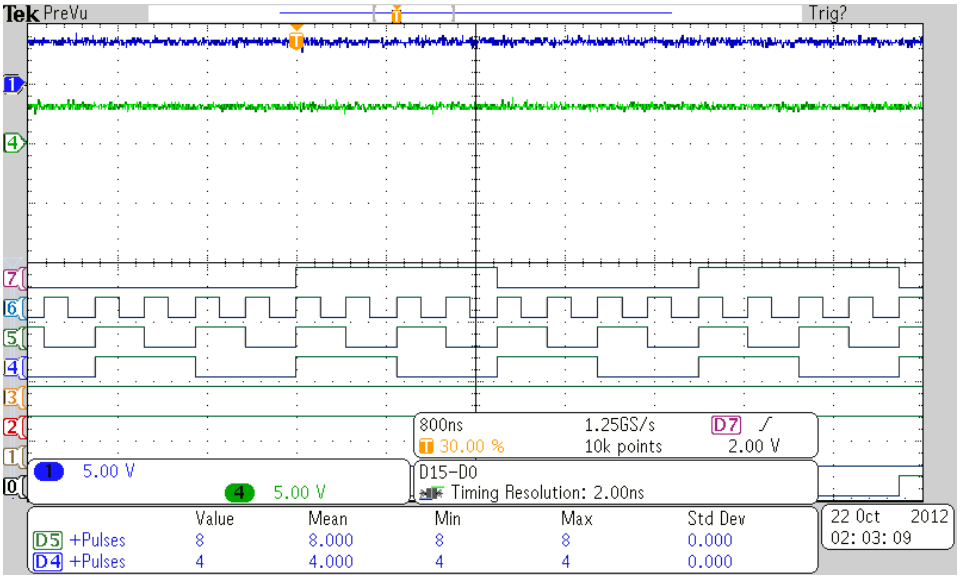


Figure 5.5. Clock generation and division waveforms.

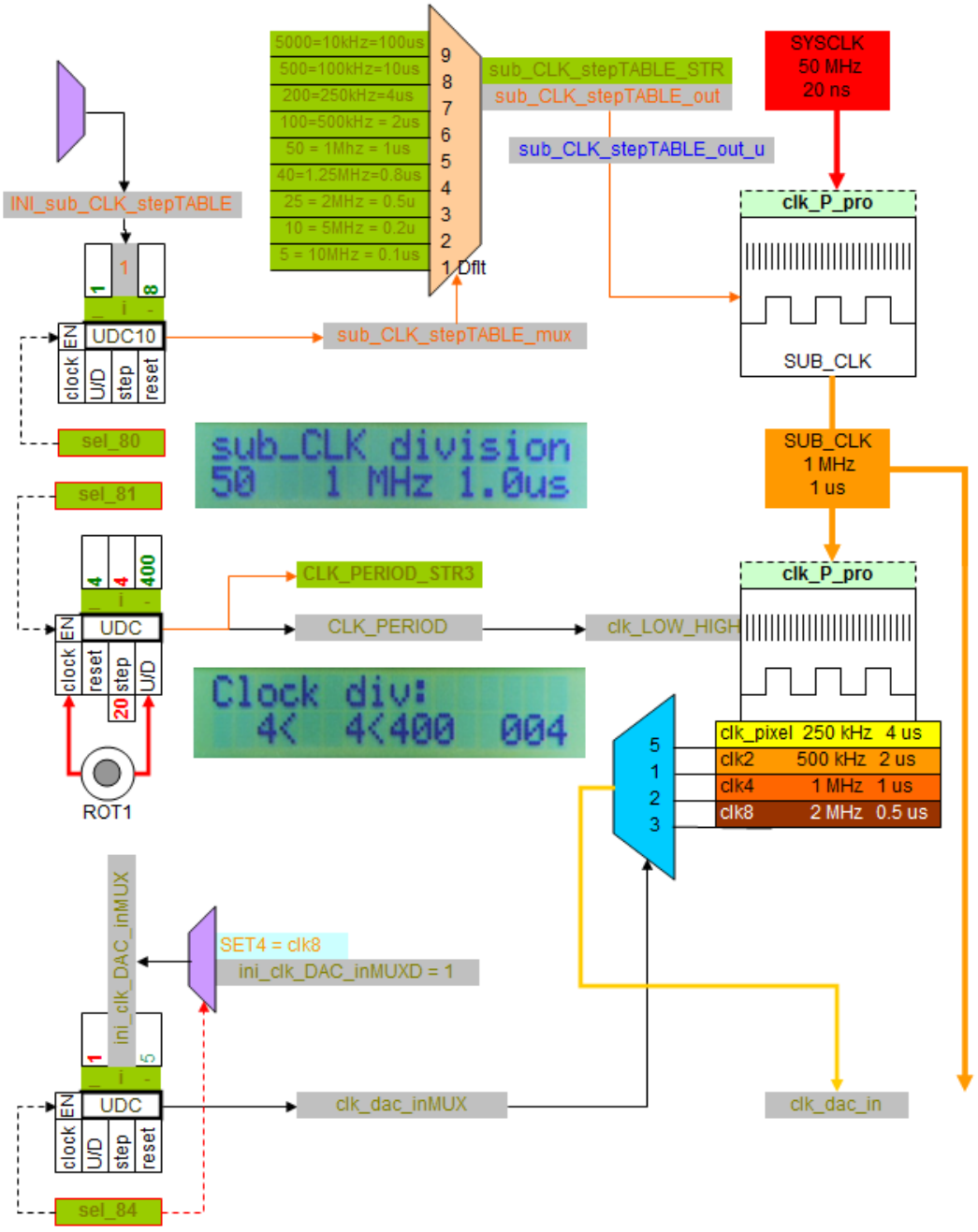


Figure 5.6. Block diagram of clock generation and division.

5.5. LCD controller

The two-line x 16-character liquid crystal display (LCD) hardware module receives three control signals–command/data, read/write, and LCD enable/disable–a clock, and eight bits of data (Figure 5.7 a), which are sent by the LCD controller block.

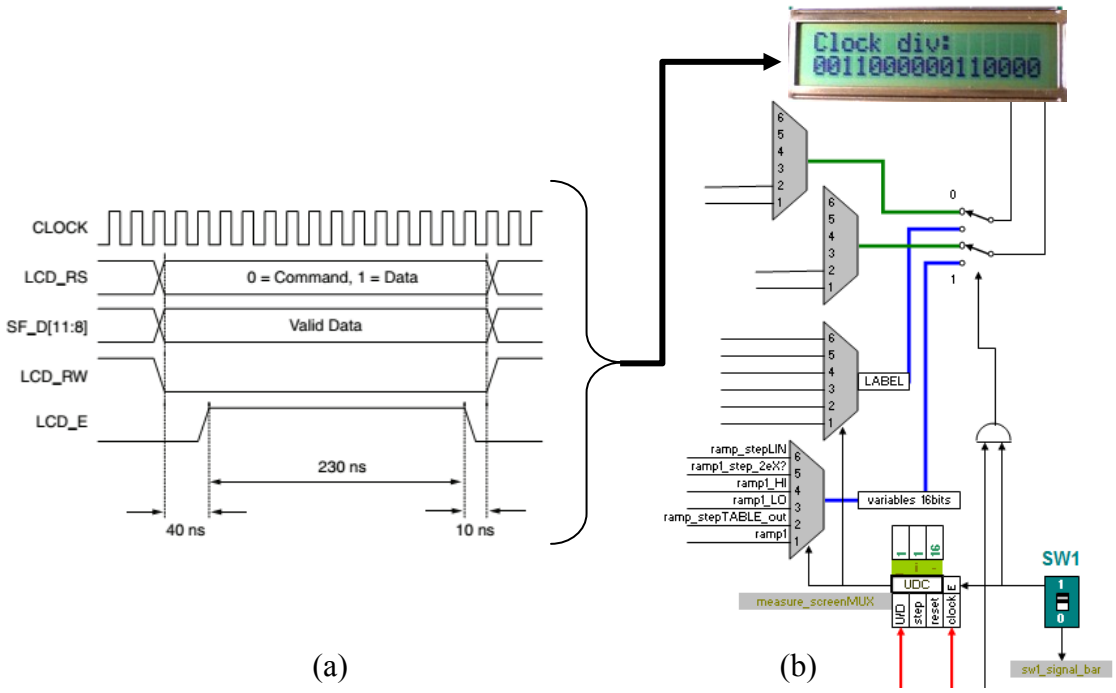


Figure 5.7. LCD signals from controller block (a) [18] and manual selection of internal number measurement (b).

This block receives two strings of 16 characters that are written on RAM memory of the LCD module [43], which constantly reads its content for display. This asynchronous process updates the screen as soon as the value of some parameter changes on the up/down counters. Adaptations of the original code were made, allowing two more lines of 16 bits to be shown on the LCD screen as 0's and 1's, for verification of numbers and variables inside the program as binary numbers (Figure 5.7 b) .

5.6. LCD screen selector

Keeping in mind the development of a simple test system independent of third-party software/hardware (i.e., computer and GUI), the onboard LCD receives two lines of strings that are updated with labels or variable values defined on compilation. The rotary switch has a push button that alters its function between parameter (screen) selection and

value modification of the desired parameter (Figure 5.8). Several parameters can be grouped and adjusted in one screen, depending on connected hardware.

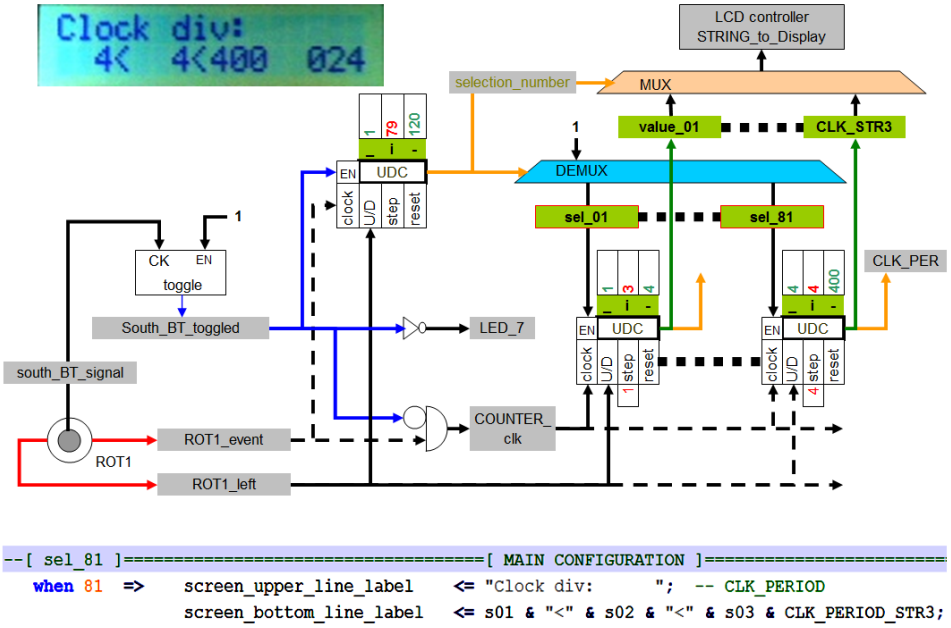


Figure 5.8. Block diagram of LCD screen selector and adjustment of parameters.

The label of each line, although it must be defined on the source program and compiled, is easily and directly edited. The characters typed inside the double quotation marks are converted inside the main code from a string type to the correspondent binary code, which will be sent by the LCD controller block, read, and correctly interpreted by the LCD board.

5.7. Context menu

After reaching the limitation of available connections for the desired number of switches and push buttons, a context menu was created on the LCD display (Figure 5.9), in the way that any number of desired virtual switches could be created using minimal hardware. In this case, the screen selector signal (sel_160) also enables a toggle function to the four context push buttons, each selecting an internal connection and the selection

label to be displayed.

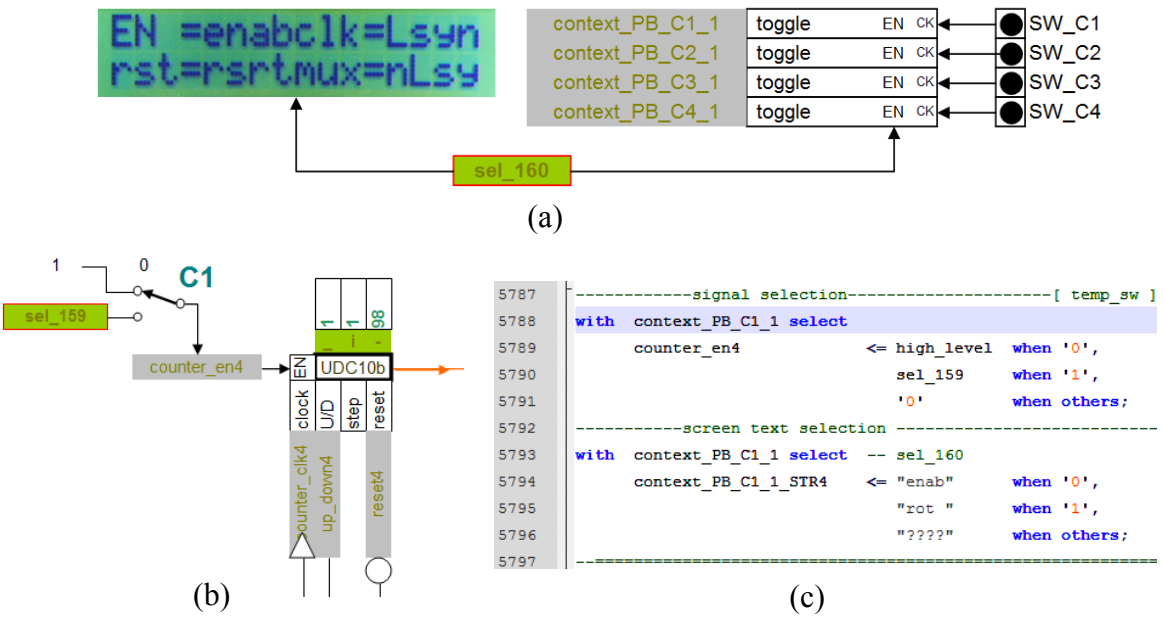


Figure 5.9. Context menu and switches (a), circuit under testing (b), and correlated VHDL code (c).

5.8. Pulse generator

There are 18 pulse generators (Table 5.1) based on a counter process controlled by a clock and by a reset/start signal, the origin of which can be selected by software on a specific screen via a multiplexer (Figure 5.10). The size, position, and high-level size of the periodic pulse are defined by their respective parameters, also adjusted online.

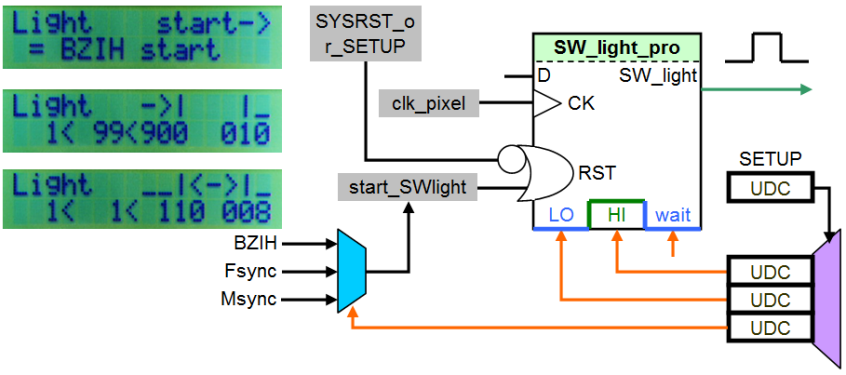


Figure 5.10. Block diagram of pulse generation and its parameters.

With these functionalities, several signals could be started at the same time to test the unit cell and, the relative position between the pulses can be adjusted online as desired to obtain a variable test pattern, with immediate waveform response from the hardware for visual analysis of their interaction.

Two specific counters generate a vertical line and a horizontal line in the video output, with adjustable position and size on screen. A simple AND-gate on these signals generated an adjustable square signal to synchronize an external laser light to a specific pixel or to a region of interest. Furthermore, this signal was used to define a region of different bias values to enhance the response and to discover specific features of the object in the acquired image.

5.9. Setup

After a desired waveforms configuration and parameter values were reached for a specific characterization, the demand for saving these values in a setup option for replication of the experience was noticed. In this first version, the new values are defined in a parallel multiplexer (purple trapezoid shape in Figure 5.11) on the main program and are compiled, the development of which required less effort and time than developing a FLASH memory access block to save these parameters.

5.10. Output control

Seeking more flexibility of operation and increased power of analysis, and also to avoid additional hardware for the limited number of IO pins, each pulse output could be turned on/off or inverted by software in the related parameter screen. A multiplexer was implemented for these functions (Figure 5.11) and to offer easier access to any internal

signals, which could be visualized by the 16-channel oscilloscope without changing the position of the probe.

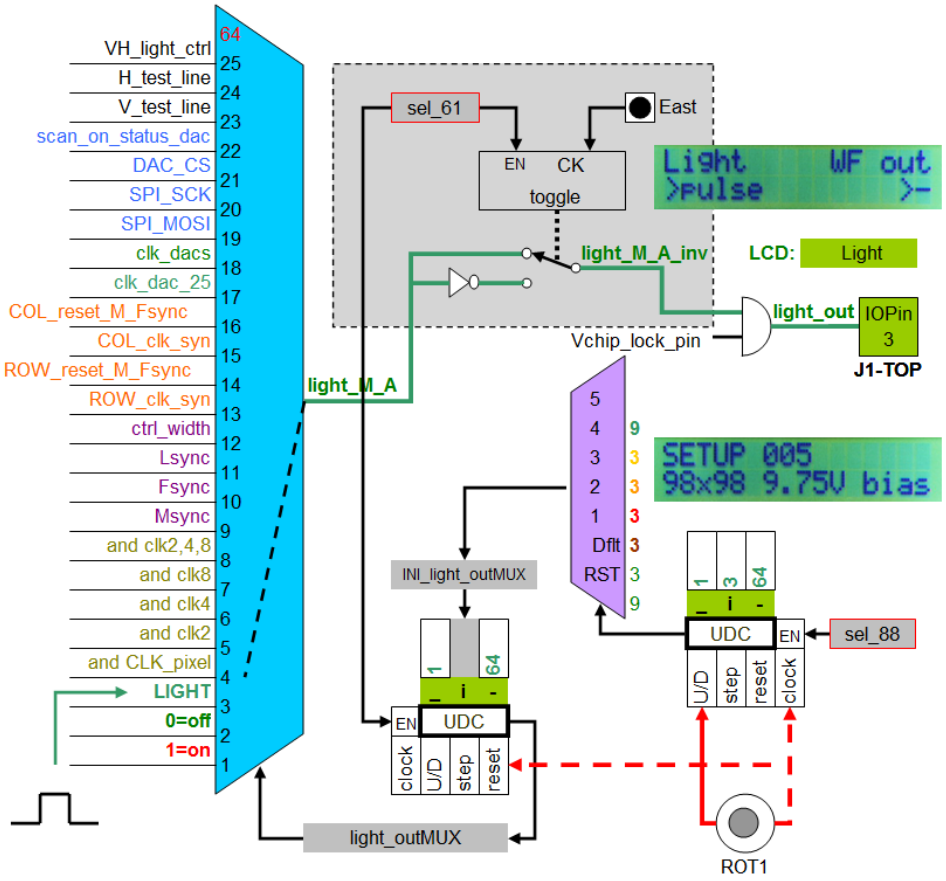


Figure 5.11. Block diagram of output control with setup multiplexer.

5.11.SYNC to oscilloscope.

One output pin was chosen from the numerous generated signals of the FPGA to be connected to the auxiliary input pin of the oscilloscope to synchronize the signals without the effort of locating the desired signal on the hardware and the repositioning of the probe. Furthermore, using one multiplexer controlled by a specific screen, virtually any internal signal could be accessed to synchronize the oscilloscope. One specific pulse signal (EXT_sync) also was designed to permit a more practical delay operation similar to the one existing in the oscilloscope.

5.12. Frame time calculation

The test system offers the possibility to adjust the desired number of horizontal active and dead pixels (columns), of vertical active and dead pixels (rows), of duration (or size), of the high-level phase on pulses, and duration and position of the clamp signal. The number of pixels defines the line-sync (Lsync) signal duration, and the number of rows defines the duration of the frame-sync (Fsync) in terms of clock pulses. A main sync (Msync) signal generates the synchronization for the start of the frame, the writing/reading BIAS phase and, significantly, the integration time-phase duration, which for value modification is based on row time. Any of these parameters, if changed, alters the duration of the frame time and requires a matching of their values. This was achieved by the development of a math block to calculate the necessary number of pulses to match the size of the Fsync_wait and the Msync_wait; the relationship between the signals for this process is illustrated in Figure 5.12.

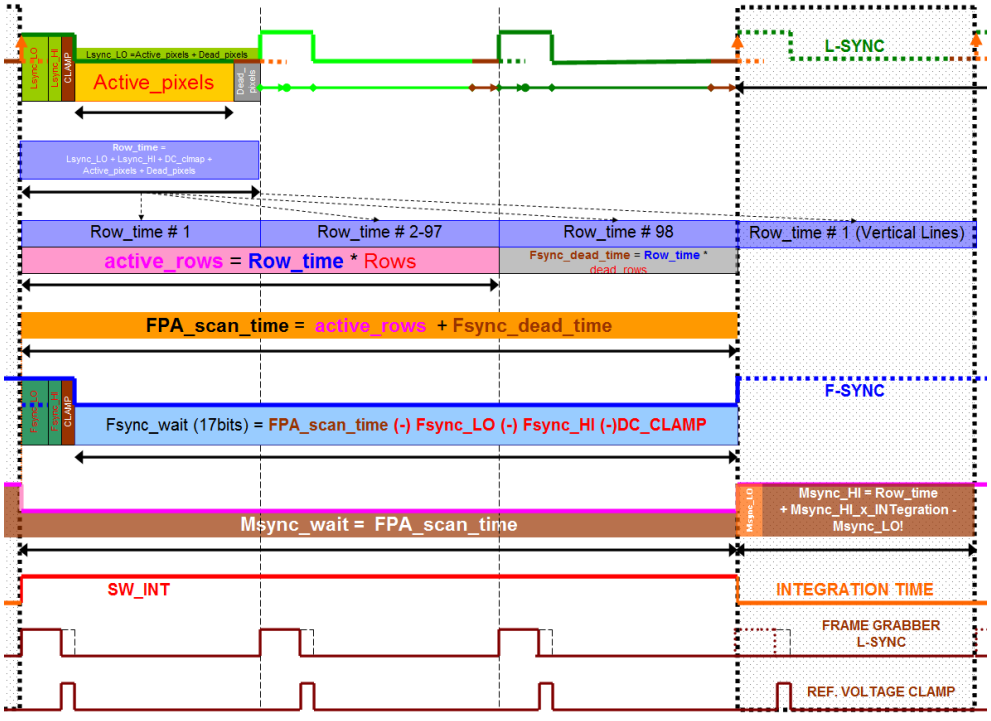


Figure 5.12. Timing diagram and relationship of variables for frame time calculation.

5.13. Pulse train

Once the 99th output of the column selector activates an external analog input to the output buffer via the multiplexer, a specific number of clock pulses is necessary to reach this column. The creative solution was to use the same pulse generator block with its high-level phase containing 99 pulses (or any number of columns), while controlling an AND-gate that switches the pixel clock signal to the output. With adequate adaptations, the number of pulses could be adjusted as a parameter on both column or row-pulse train counters, and any pixel now can be reached in the matrix for individual verification. Figure 5.13 shows the start signal, the column/row reset signal (necessary on start of counting), the AND-gate output as a status signal, and the train of pulses that goes to the column selector clock on FPA.

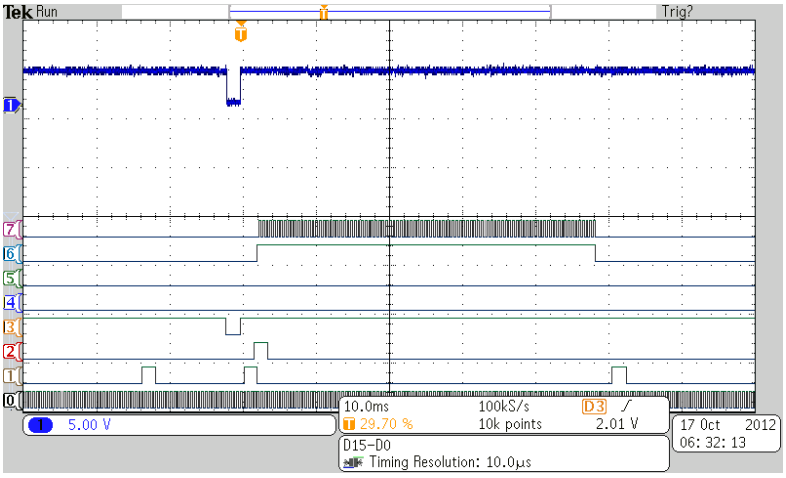


Figure 5.13. Timing diagram of a pulse train for selection of Column 99.

5.14. Scan word

Once the patterns are stored in a vector or string format, it is necessary to adopt a parallel-to-serial converter to generate each pixel BIAS in the matrix. The code of each line is sent to this converter by a multiplexer controlled by a line counter, with appropriate synchronization signals. A state machine (Figure 5.14) is initialized by the

falling edge of a start signal, reading the bits on the code_word signal and presenting this bit on output at each pulse of the input clock. Several input words can be scanned to the respective output in parallel, so this block can be used to generate the bias, the pixel clock, the line-sync, and the frame-sync for testing of a 19 x 5 pixel matrix to the frame grabber. In addition, this same block, as detailed later, generates the serial code for the DAC, together with the chip-select signal and clock.

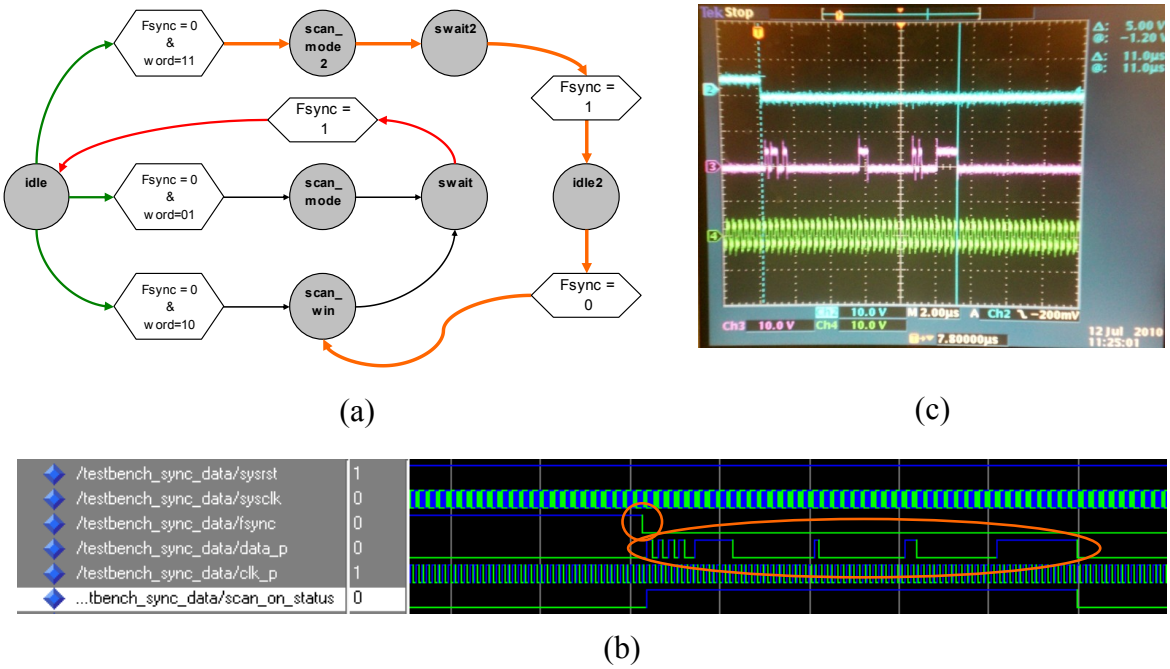


Figure 5.14. State machine diagram (a), simulation (b), and waveform (c) of the scan_word.

5.15. DAC ramp generator

To generate a ramp on an analog signal, the same up/down counter block was used as a variable memory, with small adaptations. On this block, minimum and maximum values, the step (or number to be added/subtracted), and the clock division on this counting process can be defined. As illustrated in Figure 5.15, working on these parameters to be sent to the DAC, the slew-rate and voltage limits of a digital pulse can be controlled.

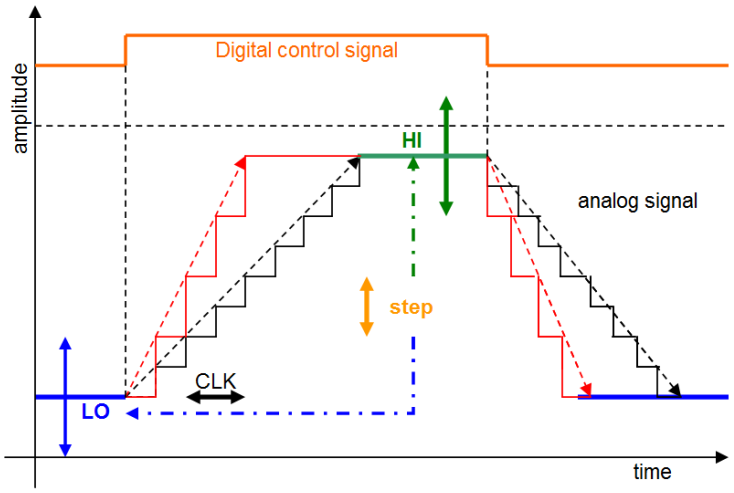


Figure 5.15. Ramp generation parameters.

The digital signal controls the up/down input, defining the ascendant or descendant ramp. As described in Section 4.6, a counter of 0 to 3,000 (instead of 4,095), representing a voltage range of 0 V to 15 V, results in 5 mV (0.033%) of resolution per count (step). As shown in Figure 5.16, this number is generated by a counter of 0 to 300 in step of two counts and multiplied by 10. Inside the counter, the number is divided by two, which is an easy software operation. For example, 298 counts divided by two results in 149; that string will be displayed as "14.9V" after the concatenation of "14", ".", "9", and "V" characters. The 3,000 counter will have 2,980 counts, which multiplied by 5 mV/count results in 14.9 V. In this way, the LCD will directly display the adjusted voltage on minimum, maximum, and step parameters. Figure 5.18 shows the VHDL instantiation code for the minimum voltage counter, as well as shows the strings concatenation code for display into the LCD. The LCD picture shows the minimum, maximum, and step parameters of Ramp 1 in volts.

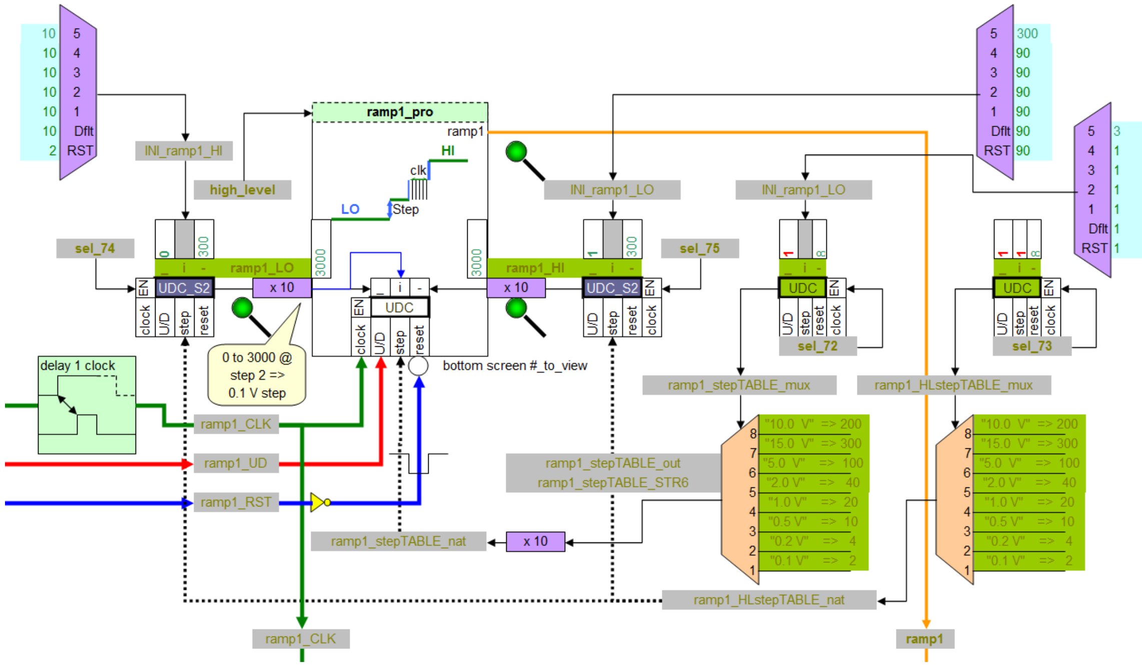
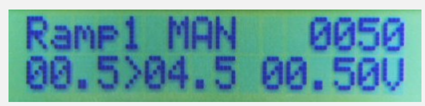


Figure 5.16. Block diagram of ramp generator.

```
--------------------------------------------[ ramp1_LO ]----------------------------------------------------
counter_ramp1_LO: entity work.counter_STR_by2(beh)
port map (-- THERE       =>          HERE!
         --in-<-<-<-<-<-<-<-<-<--out--------
         Counter_CLK        =>     COUNTER_CLK          ,
         update             =>     update_param         ,
         reset              =>     SYSRST               ,
         --load             =>     low_level            ,
         counter_en         =>     sel_74               ,--<--------< selection # on screen
         up_down            =>     ROT1_left            ,
         STEP               =>     ramp1_HLstepTABLE_nat,     --ramp1_stepTABLE_out   ,  -- natural --2            ,
         min_val            =>     min_ramp1_LO         ,     --CONSTANT  - natural   s118
         initial_value      =>     INI_ramp1_LO         ,     --signal from setup     CONSTANT  - natural   s119
         max_val            =>     max_ramp1_LO         ,     --CONSTANT  - natural   s120
--                |      |
--             ___v______v___
--            [              ]
--            [______________]
--                |      |
--                v      v
        ---out-------->->->->------in---------
        string_3dig        =>     ramp1_LO_STR3         ,     --signal    string divided by 2 =>  298 / 2 = 149 => 14.9V
        stored_value       =>     ramp1_LO                    --signal    unsigned(16 downto 0)
         );
         ramp1_LOx10        <=     ramp1_LO * 10;
         ramp1_LO_nat <= to_integer(unsigned(ramp1_LOx10)); --from unsigned 17 bits to natural     [ unsigned_to_natural ]
----------------------------------------------------------------------------------------------
         ramp1_LO_STR3_dec    <= ramp1_LO_STR3(3)   ;
         ramp1_LO_STR3_unit   <= ramp1_LO_STR3(1)  & ramp1_LO_STR3(2)  ;
---------10--------20--------30--------40--------50--------60--------70--------80--------90--------100--------113
```




```
-----[ sel_70 ]XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
      when 70  =>      screen_upper_line_label     <= "Ramp1 MAN    " & ramp1_STR4 ;
                       screen_bottom_line_label    <= ramp1_LO_STR3_unit & "." & ramp1_LO_STR3_dec & ">"
                        & ramp1_HI_STR3_unit &  "." & ramp1_LO_STR3_dec & " " & ramp1_STR4_12 &   "." & ramp1_STR4_34 & "V";
```

Figure 5.17. Minimum voltage counter instantiation (center), LCD screen with Ramp 1 parameters (top), and screen labels/values on code (bottom).

5.16. DAC programming

A parallel-to-serial block was used to generate the serial command word for the digital-to analog converter (Figure 5.18), which consists of a command (4 bits), an address (4 bits), followed by data value (12 bits), and "don't care" (4 bits). The system clock of 50 MHz provides the maximum frequency to write the command word on the DAC, and one more bit was added on each of the four concatenated command words to match the desired number of the 100 system clock division, which defines the pixel clock frequency of 500 kHz and its period time of 2 µs.

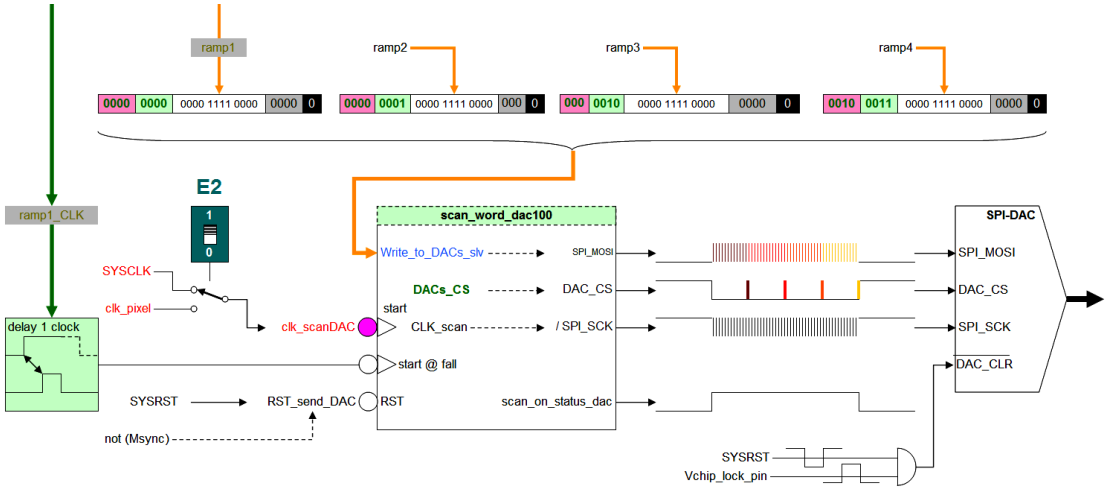
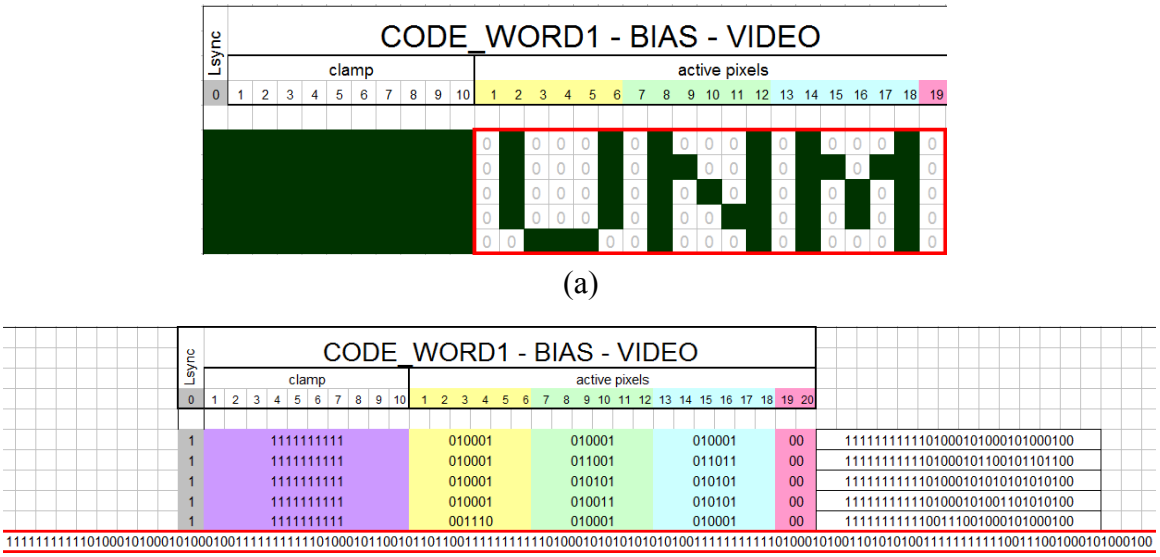


Figure 5.18. Block diagram of DAC programming function.

The start pulse, coming from the Ramp 1 counter clock, activates the scanning of the 100-bit word to the SPI_MOSI node (command input). The one-clock delay block allows the Ramp 1 counter to update its output before the scan_word block begins reading. Inside the scan_word block, another 100-bit fixed word is read to generate the chip-select signal, which starts the conversion process on DAC. In addition, the scan_word block controls the system clock to the DAC, avoiding pulses and noise generation when no conversion is necessary, and generates a status pulse. The /DAC_CLR signal is the active-low, asynchronous reset input to the DAC.

5.17. Row0_UNM backup plan

As described in Section 3.10, considering the failure of the photodiodes response, the first row was designed without photodiodes, presenting only the analog memory that could maintain different voltage values on each pixel, could work as a buffer, could sample-and-hold, and could demonstrate the individual bias feature. Once the first row possesses 96 active pixels, a specific pattern of synchronization signals is generated by the scan_word block to create a matrix of 19 horizontal pixels and 5 vertical pixels (95 total pixels). The desired pattern was drawn on Excel software, using the conditional formatting feature on each spreadsheet cell for the number "1," facilitating visualization. These binary numbers were automatically concatenated (Figure 5.19) to be copied to the VHDL source code.



(a)

(b)

Figure 5.19. Pattern drawing tool (a) and concatenated binary number (b).

Figure 5.20 shows the video waveform of another generated pattern, together with the pixel clock, line-sync, frame-sync, and master-sync, with the clamp signal added at the start of the line sweeping.

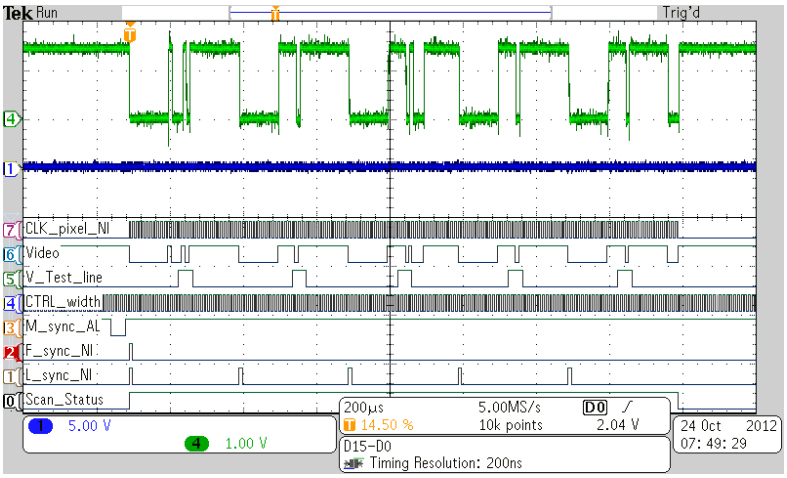


Figure 5.20. Video waveform of 19 x 5-pixel generated pattern.

5.18.98 x 98 image pattern

To demonstrate the individual bias definition on each pixel, a binary image pattern was created with Excel software as a tool for bits concatenation and string creation. The desired text was written in a text box and used transparent color as a guide for a manual bits definition (Figure 5.21). Then, the image was sliced in strings of similar sizes and shapes to reduce the number of constants in the source code (Figure 5.22).

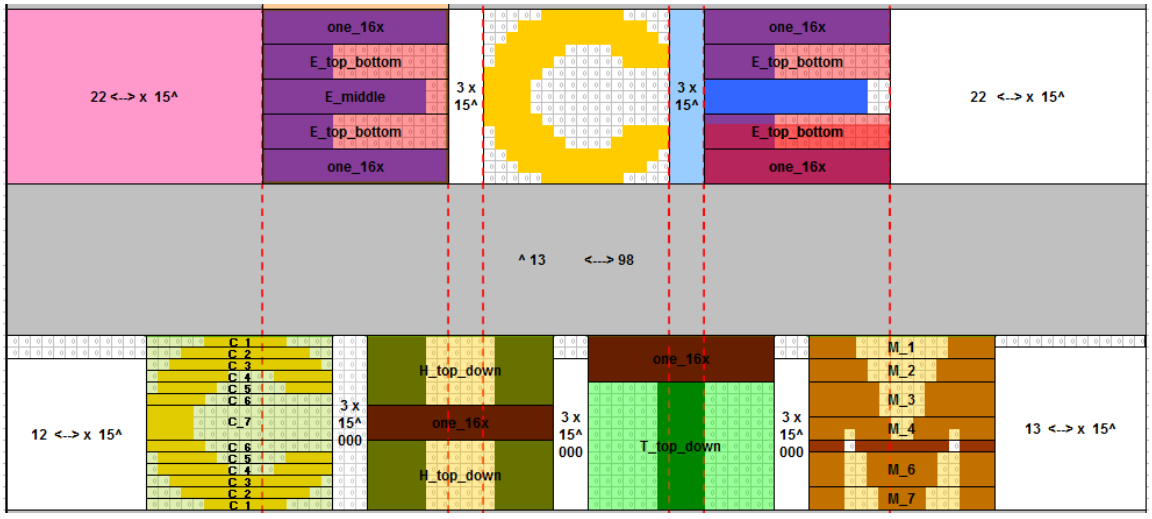


Figure 5.21. Slicing of binary image pattern for concatenation and definition of code.

```
1255    U_top       :  std_logic_vector(15 downto 0):=  "1111100000011111";
1256    E_top_bottom:  std_logic_vector(15 downto 0):=  "1111110000000000";
1257    E_middle    :  std_logic_vector(15 downto 0):=  "1111111111111100";
1258    C_1         :  std_logic_vector(15 downto 0):=  "0000011111110000";
1259    C_2         :  std_logic_vector(15 downto 0):=  "0000111111111100";
1260    C_3         :  std_logic_vector(15 downto 0):=  "0001111111111110";
1261    C_4         :  std_logic_vector(15 downto 0):=  "0111111000011111";
1262    C_5         :  std_logic_vector(15 downto 0):=  "0111110000001111";
1263    C_6         :  std_logic_vector(15 downto 0):=  "1111100000000000";
1264    C_7         :  std_logic_vector(15 downto 0):=  "1111000000000000";
1265    H_top_bottom:  std_logic_vector(15 downto 0):=  "1111100000011111";
1266    T_top_bottom:  std_logic_vector(15 downto 0):=  "0000001111000000"
```

Figure 5.22. Constant vector components of binary image pattern.

The scan_word block was used to read each line of the code to the video output, which is controlled by the reset signal that is connected to line-sync signal and by the clock signal, which is connected to the pixel clock. The desired line code comes from a word multiplexer controlled by a counter, the count of which is increased by the line-sync signal and is reset by the frame-sync signal (Figure 5.23).

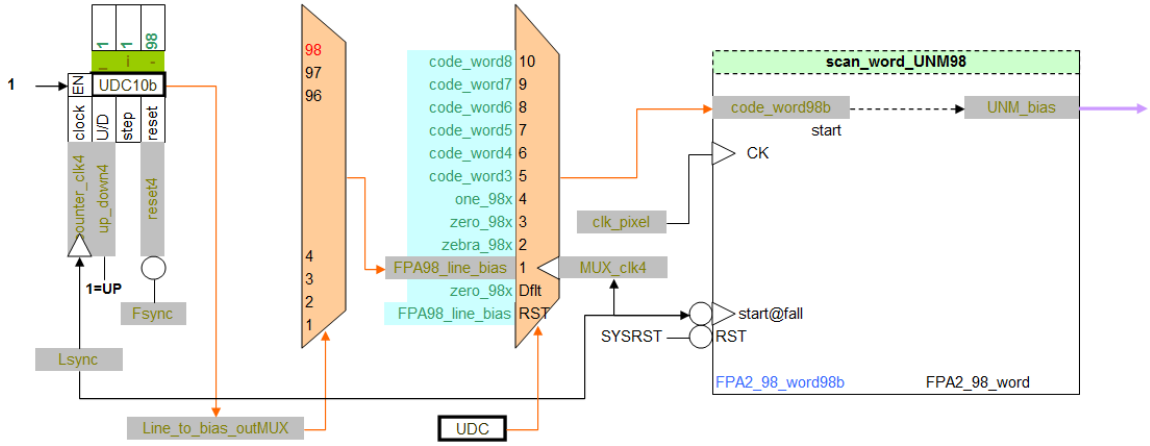


Figure 5.23. Image pattern scanner for binary bias generation.

5.19. ROI biasing

To generate not only a fixed image but to demonstrate online sizing and positioning of a region of interest (ROI) with different bias for image enhancement and object location, specific signals were generated. One pulse generator is started (reset) on the line-sync pulse and receives its clock from the pixel clock signal, generating a pulse inside the line

timing, presenting a vertical line on the FPA and consequently on the screen of the frame grabber. Another pulse generator is started at the frame-sync pulse, and its clock comes from the line-sync signal, generating a horizontal line on the FPA/frame grabber (Figure 5.24). These signals also can be used for testing the video reception and synchronization, without the requirement of passing the ITP-ROIC for processing. The combination of the vertical test line and horizontal test line generates a squared window signal that is used to define a region of interest for biasing. The size and position of this region can be adjusted (Figure 5.25), even permitting the selection of just one pixel. In this case, this signal can control a light over the FPA to measure the response of one pixel without the requirement of optics manipulation or focusing.

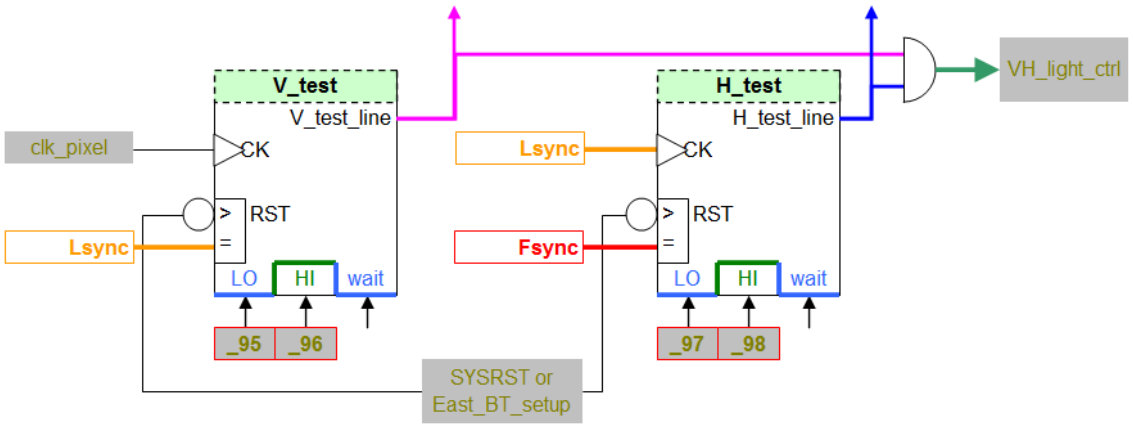


Figure 5.24. Positioning and sizing of vertical, horizontal, and squared ROI windows.

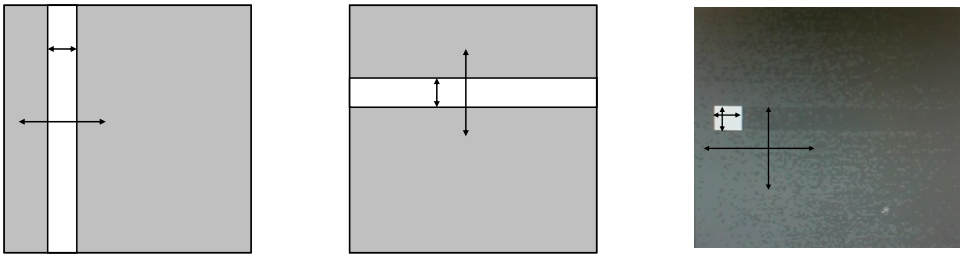


Figure 5.25. Positioning and sizing of vertical, horizontal, and squared ROI windows.

5.20. VGA controller

As described in Section 4.9, the Spartan 3E board uses minimal hardware to connect the FPGA pins to an external monitor, which can receive signals defining eight colors on VGA resolution (640 x 480 pixels). This is the starting point for displaying an image using only the FPGA hardware resources, avoiding the requirement of an external computer, frame grabber, and proprietary software. More importantly, the final application of image acquisition requires autonomous operation. A VGA controller that generates the pixel clock and the vertical and horizontal synchronization signals [44] was tested, and its timing specifications are shown in Table 5.2 and Figure 5.26.

Symbol	Parameter	Vertical Sync			Horizontal Sync	
		Time	Clocks	Lines	Time	Clocks
T_S	Sync pulse time	16.7 ms	416,800	521	32 µs	800
T_{DISP}	Display time	15.36 ms	384,000	480	25.6 µs	640
T_{PW}	Pulse width	64 µs	1,600	2	3.84 µs	96
T_{FP}	Front porch	320 µs	8,000	10	640 ns	16
T_{BP}	Back porch	928 µs	23,200	29	1.92 µs	48

Table 5.2. VGA timing for 640 x 480 pixels [44].

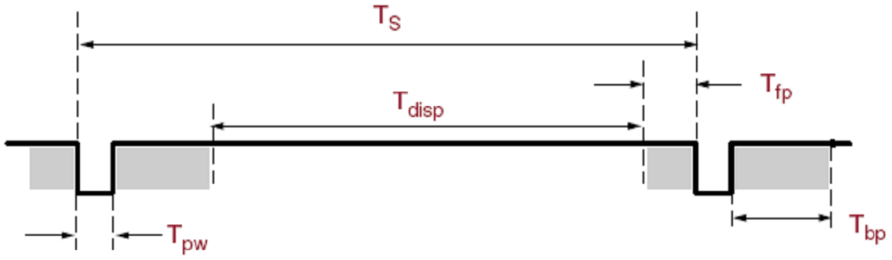


Figure 5.26. VGA control timing [44].

5.21. UCF file

The user constraint file (UCF) offers versatility and portability for the VHDL code, defining the interconnection between the signals in the source code and hardware pinout of the FPGA. This file also defines hardware specifications for the inputs/outputs, such as the voltage range (TTL, LVCMOS25, LVCMOS33), the slew rate (slow/fast), and the output drive current (2, 4, 6, 8, 12, 16 mA). The VHDL code can be used with any hardware, requiring only changing the interconnection names on the file. But it is important to manipulate the names' definition to simplify any desired change of internal signals routing to the external pin, as well as to easily identify the board connector. Figure 5.27 shows the internal signal names; Figure 5.28 presents the I/O port name on code (bridge between signal and pinout); and Figure 5.29 illustrates the FPGA pins.

```
11409   --xxxxxxxxxxxxxxxxx     connector J4    xxxxxx
11410   ------------------------- T O P -------------
11411            IOPin25     <= SW_bias_ext_out      ;
11412            IOPin27     <= SW_zero_out          ;
11413            IOPin29     <= SW_int_out           ;
11414            IOPin31     <= SW_hold_out          ;
```

Figure 5.27. Internal signal connected to in/out port on code.

```
1479    -------------------------connector J4
1480      IOPin25     :  out   std_logic ;
1481      IOPin26     :  IN    std_logic ;
1482      IOPin27     :  out   std_logic ;
1483      IOPin28     :  IN    std_logic ;
1484      IOPin29     :  out   std_logic ;
1485      IOPin30     :  IN    std_logic ;
1486      IOPin31     :  out   std_logic ;
1487      IOPin32     :  IN    std_logic
```

Figure 5.28. Port defined with the physical connector name on the board.

```
186     NET "IOPin25"       LOC = "c14" | IOSTANDARD = LVCMOS25 | SLEW = SLOW | DRIVE = 8;
187     NET "IOPin27"       LOC = "A16" | IOSTANDARD = LVCMOS25 | SLEW = SLOW | DRIVE = 8;
188     NET "IOPin29"       LOC = "E13" | IOSTANDARD = LVCMOS25 | SLEW = SLOW | DRIVE = 8;
189     NET "IOPin31"       LOC = "B11" | IOSTANDARD = LVCMOS25 | SLEW = SLOW | DRIVE = 8;
```

Figure 5.29. Board connector name attributed to FPGA pinout.

Chapter 6

Results

A microphotograph of the die, with a total size 5.14 x 5.14 mm^2, is shown in Figure 6.1, together with the identification of the main circuits. Table 6.1 summarizes the features of the 96 x 96 pixel test prototype chip, which has been designed and fabricated via MOSIS [45] in a double-poly, four-metal layer, standard 0.35 µm mixed-signal 3.3/15 V TSMC high-voltage CMOS process.

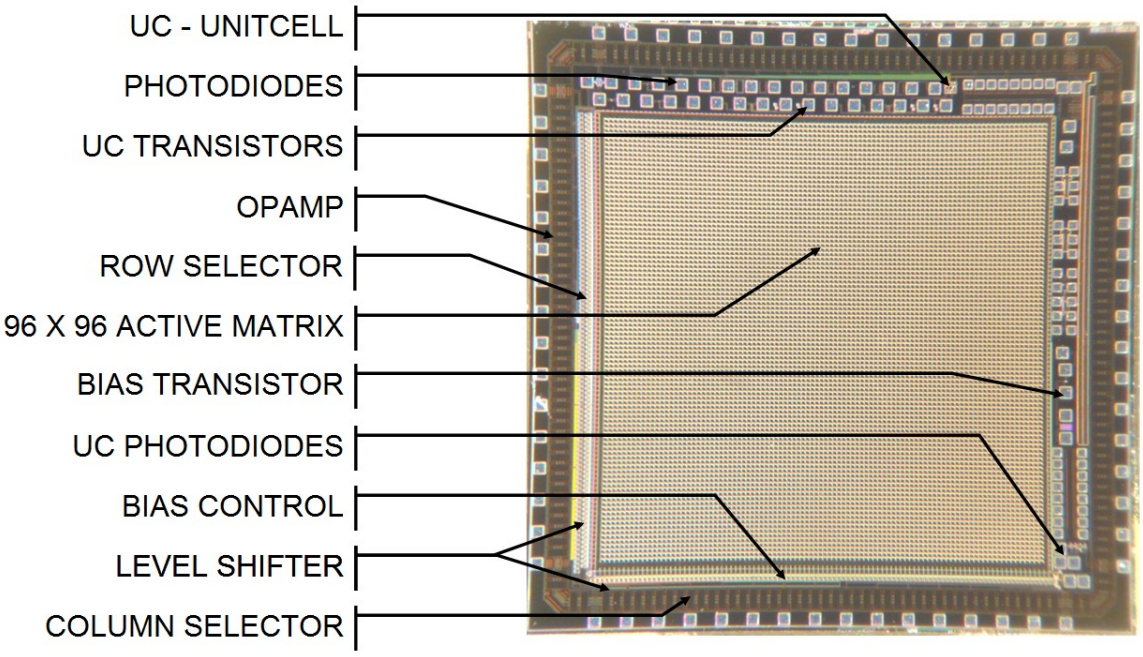
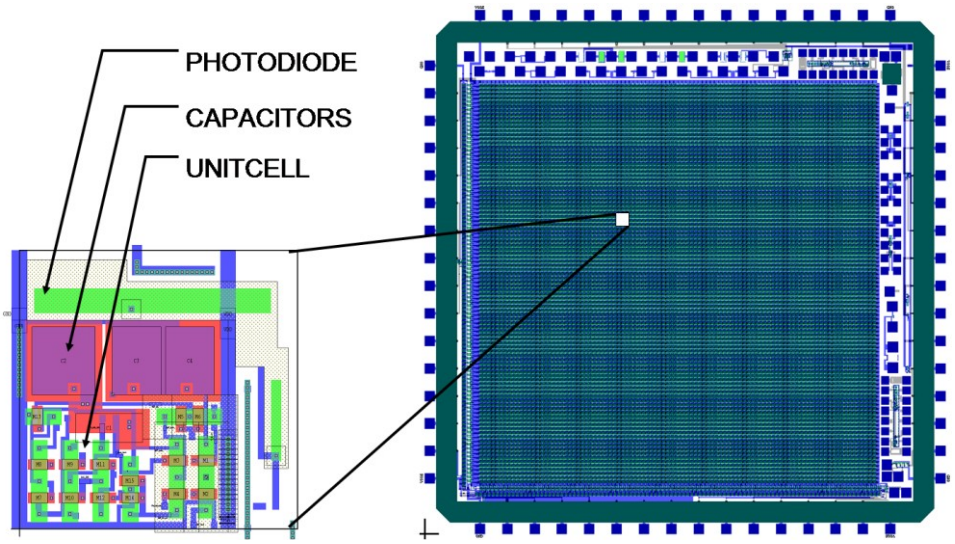


Figure 6.1. Microphotograph of test chip.

The layout of the unit cell and chip are shown in Figure 6.2. The pixel has 15 transistors and four capacitors designed in a 30 x 30 μm^2 area at a pitch of 40 x 40 μm^2 to fit the photodiodes. Considering 320 μm^2 of area not covered by metal layers, the fill factor is 20%.

Technology		TSMC 0.35 μm CMOS 2P4M
Power supply	Low voltage section	3.3 V
	High voltage section	15 V
Die size (including pads)		5.14 x 5.14 mm^2
Total pixels array size		98 x98
Active pixels array size		96 x 96
Pixel pitch		40 x 40 μm^2
Pixel size		30 x 30 μm^2
Phtotodiode type		n+/n-well/p-sub
Fill factor		20%
Unit cell transistors		15
Unit cell capacitors		4
C-INT		74fF
C-Bias		55 fF
C-Hold		57 fF
Integration time		0.85 to 245 ms
Input voltage swing		10 V
Output voltage swing		7.8 V

Table 6.1. ITP-ROIC design main parameters.

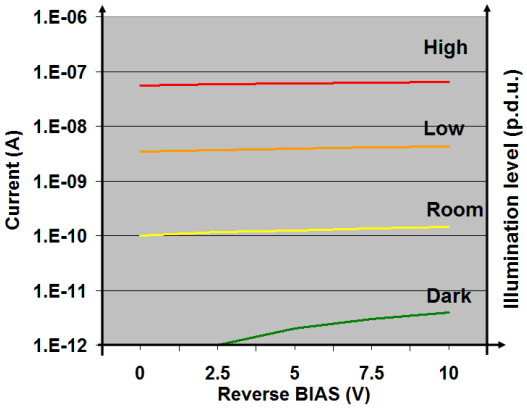


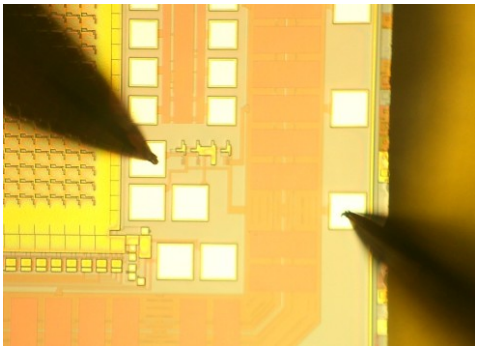
(a) (b)

Figure 6.2. The 30 x 30 µm^2 pixel layout and the test photodiode on pitch of 40 x 40 µm^2 (a), from the layout of the chip (b).

6.1. Photodiode

Figure 6.3 (a) shows the response of the adopted unit cell photodiode (PD) structure to procedure-defined units (pdu) of illumination, where one can note not only the photocurrent response to the illumination level but the desired variation of photocurrent related with the applied bias.





(a) (b)

Figure 6.3. n+/n-well/p-sub photodiode response (a), and probing for the guard-ring type (b).

Initial comparative measurements of the four types of photodiode test structures are shown in Table 6.2. As expected, the covered photodiode shows the smaller response. But, and unexpected, the value of the current was nearly as high as that of the reference structure. As expected, the photodiode with a guard-ring showed a lower response versus the Unit Cell photodiode, due to the grounding effect. Comparing these values with the more detailed characterization of Figure 6.3, one could conclude that the very high illumination level makes the covered photodiode respond to the high level of scattering. The photodiode connected to the PAD showed an extremely high abnormal current value. Suspecting pad leakage or light response, the separated pad was tested and did not present related significant values for these effects. Reviewing the design, a problem was found in the photodiode connection, triggering an unintended short circuit to ground. This problem was not detected by the highlight tool because the substrate connection was disabled. On the other hand, it was possible to measure the ground resistance of the substrate, which was near 800 ohms.

Type	Covered	Guard-ring	Unit cell	To pad
Photocurrent (μA) @ 5 V	3.0	3.2	3.6	6,350

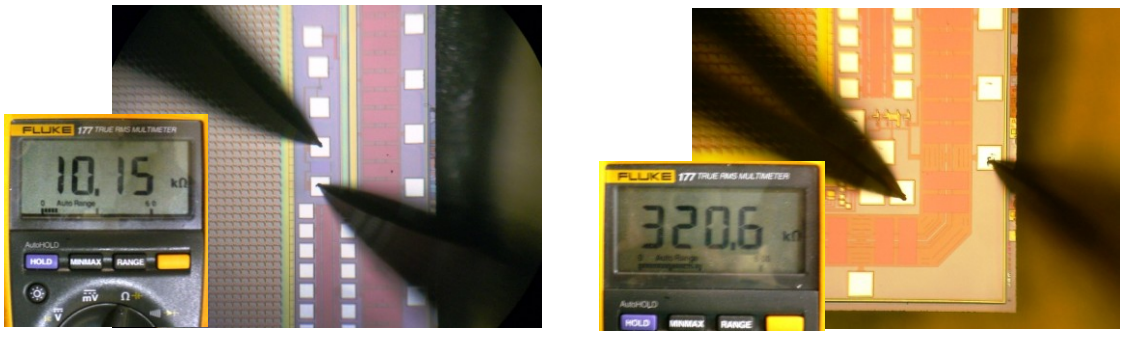
Table 6.2. Response comparison of different photodiode structures.

6.2. Poly resistors

The designed poly resistors showed good precision of value definition, i.e., 1.5% for the 10 kΩ test structure and 0.18% for the 320 kΩ resistor, as shown in Figure 6.4. This was necessary once an internal digital-to-analog conversion using an R-2R ladder was planned to assure a better settling time for the output voltage.

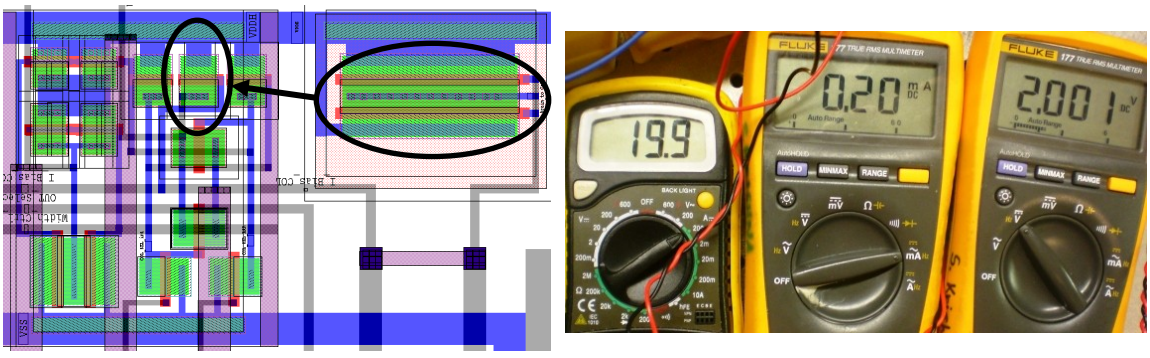
6.3. Mirror transistors

As described in Section 3.4, the FF 99 on column selector does not drive current to any internal column but has its column-bias transistor and multiplexer switch driven to an external pad. Originated from the 10 x 1 sizing of these transistors (Figure 6.5 a), the column-bias current-mirror transistor supplies a current of 1/10 of the input-adjusted bias current without the requirement of a clock to the column selector. Figure 6.5 (b) shows the externally adjusted bias current of 200 μA (middle multimeter) to reflect 19.9 μA (left multimeter) on a 10 kΩ current-limiter resistor. The multimeter (right) shows the measured source-to-gate voltage.



(a) (b)

Figure 6.4. Poly resistor test structure of 10 kΩ (a) and of 320 kΩ (b).



(a) (b)

Figure 6.5. Current-mirror transistor sizing relationship (a), and measurement (b).

6.4. Column selector

The group of multiplexer switches, column selector and output buffer proved to work correctly, as shown in Figure 6.6. One can observe the cross-talk of the full-swing width-control signal on the output video signal, due to parallel wires on design (Figure 3.20) and the input floating node of the output buffer amplifier. This issue was addressed on the new design by shielding these signals with a ground wire between them and by a VDD shielding layer on top [46], the last of which also shields the circuit against undesired light effects.

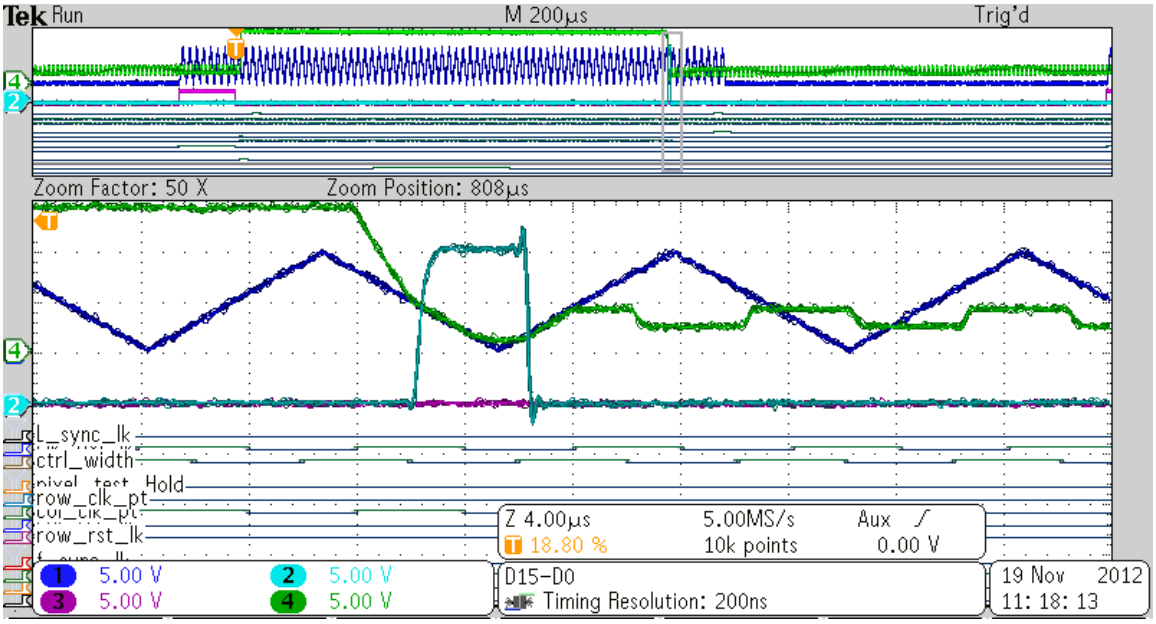


Figure 6.6. Column selector output 99 and video output in hold with cross-talk.

6.5. Unit cell

The unit cell in the separated design has proven its functionality as shown on biasing, integration and holding waveforms of the Figure 6.7.

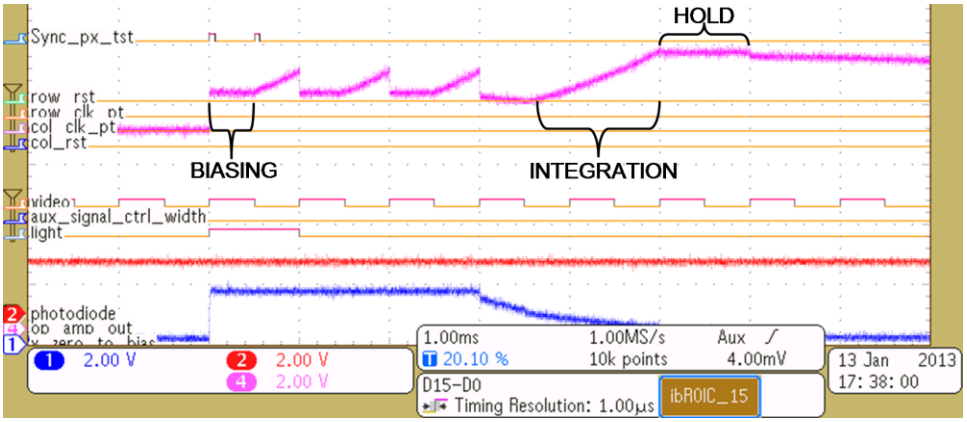


Figure 6.7. Biasing, integration and hold signals on unit cell.

The separated unit cell also demonstrates the wide voltage range in its BIAS input, from 0.04 V to 10.4 V (+-5 V related to 5.04 V on detector common node), in the same Figure 6.8 that shows the correspondent output range from 5.0 V to 12.8 V (related to VSS).

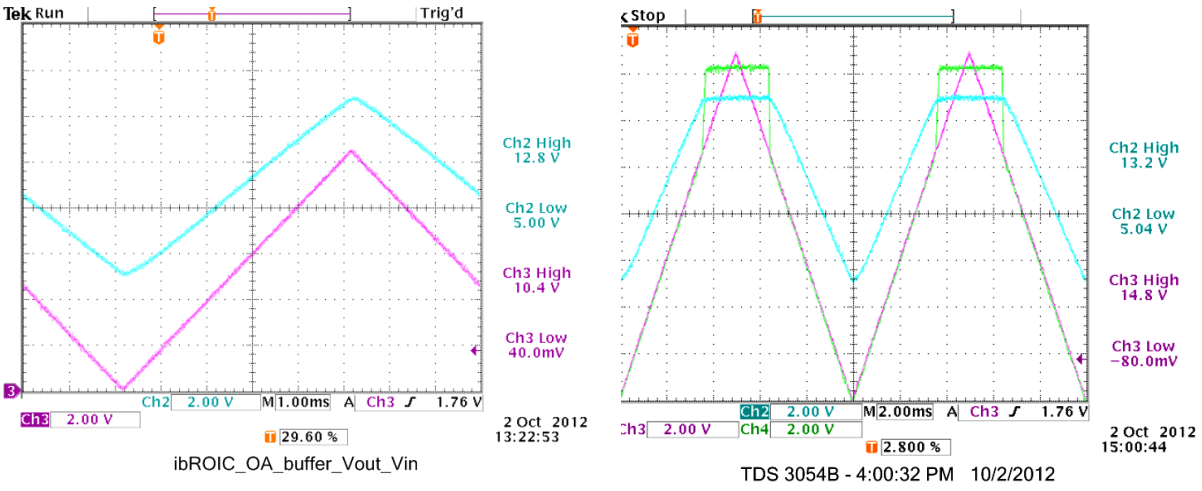


Figure 6.8. Input (a - bottom) voltage range and output swing (a - top) of unit cell.

Saturated output waveform (b) similar to simulation.

Increasing the input values, one can observe that the output waveform turns similar to that one simulated in Section 3.7.

6.6. ITP-ROIC

Two biases with correlated different integration rate are shown in Figure 6.9 for the FPA reading.

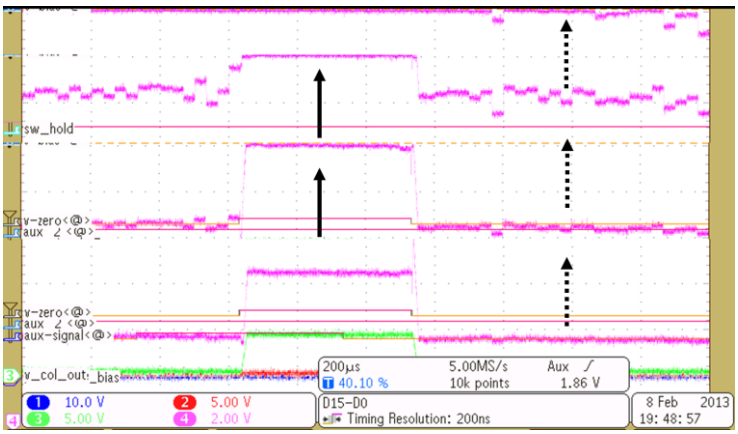


Figure 6.9. Integration with 2 biases during sweeping in one row (4 combined images).

Following adequate signals generation, connection, and synchronization, the ITP-ROIC was able to reset, bias, integrate, reference, hold, and transfer the acquired image to the frame grabber. Figure 6.10 shows the main digital signals, detaching the analog signals BIAS (top), the ITP-ROIC output (middle), and the video signal (bottom).

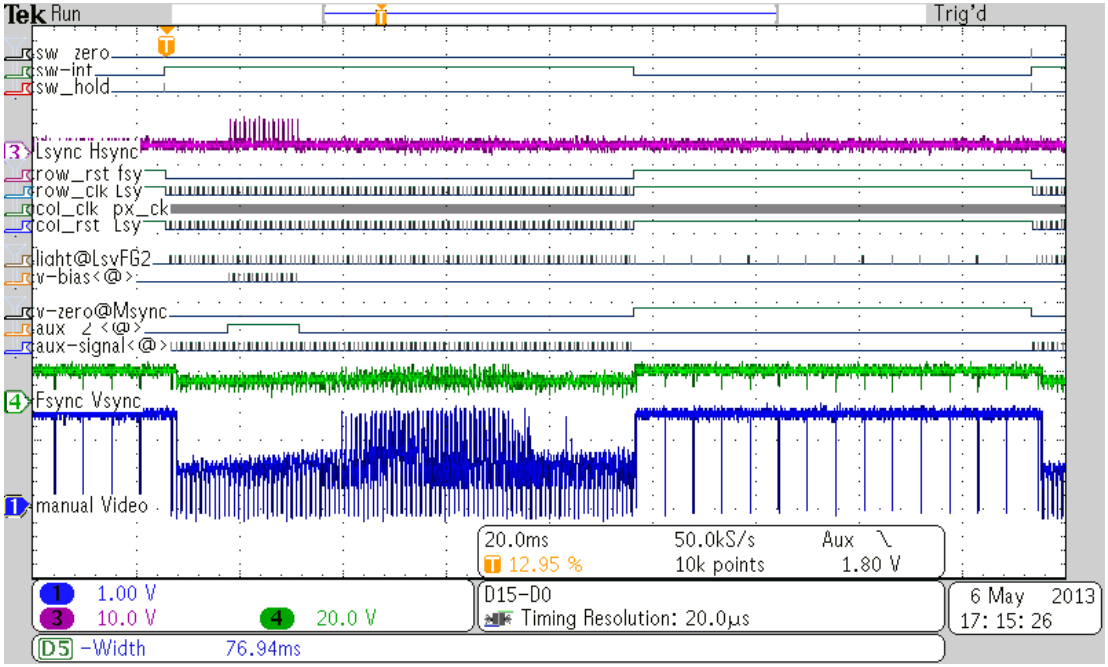


Figure 6.10. Waveforms of generated digital signals and analog measurements.

The main individual pixel biasing feature of the ITP-ROIC, controlled by the FPGA-based test system, is presented in Figure 6.11 (a) to (f).

A test image pattern was elaborated and printed, presenting several numbers and background bands at different gray levels. The acquired image, at 250 kHz of pixel clock, 10 FPS and 57.04 ms of integration time, demonstrates a region of interest defined as a rectangle. As it is moved over the white area, the enhanced image presents the numbers that were hidden on that respective location. Another example of object localization by enhancement of a region of interest using the ITP-ROIC is shown in Figure 6.11 (g) to (k). The ideal illumination for image acquisition of (g) contrasts with (h), where the lightbar barely appears. On (i), the square formed by the (j) and (k) bars reveals the object with a better contrast. Finally, an external environment image displayed in a computer monitor was acquired by the ITP-ROIC with a bottom BIAS pattern applied, as shown in Figure 6.11 (l).

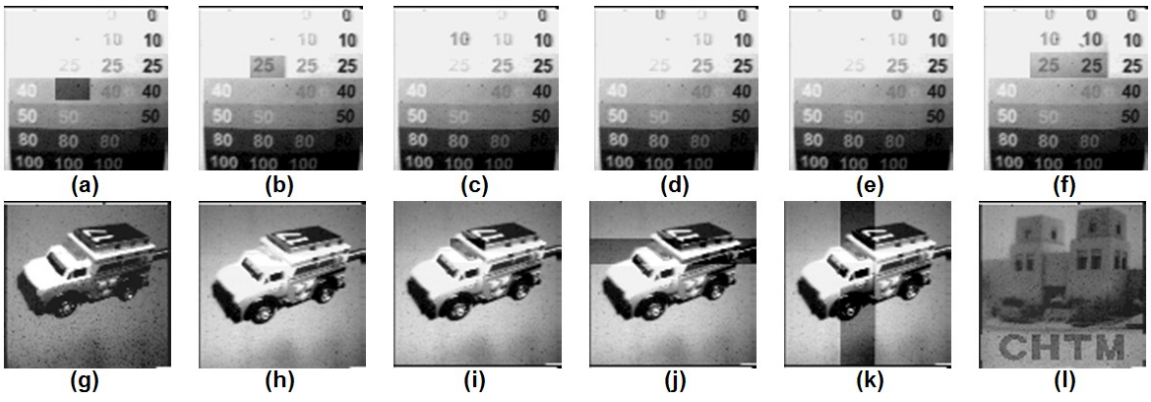


Figure 6.11. Test image pattern (a) to (f) and region of interest enhancement (g) to (k).

More detailed, Figure 6.12 presents two more examples of a region of interest hiding, due to its saturation on white level (bottom), specific features on top of the truck. A rectangular area–the resolution of which can be defined at pixel level–with a different bias is moved to the area of interest, reducing the gain and exposing new details of the object.

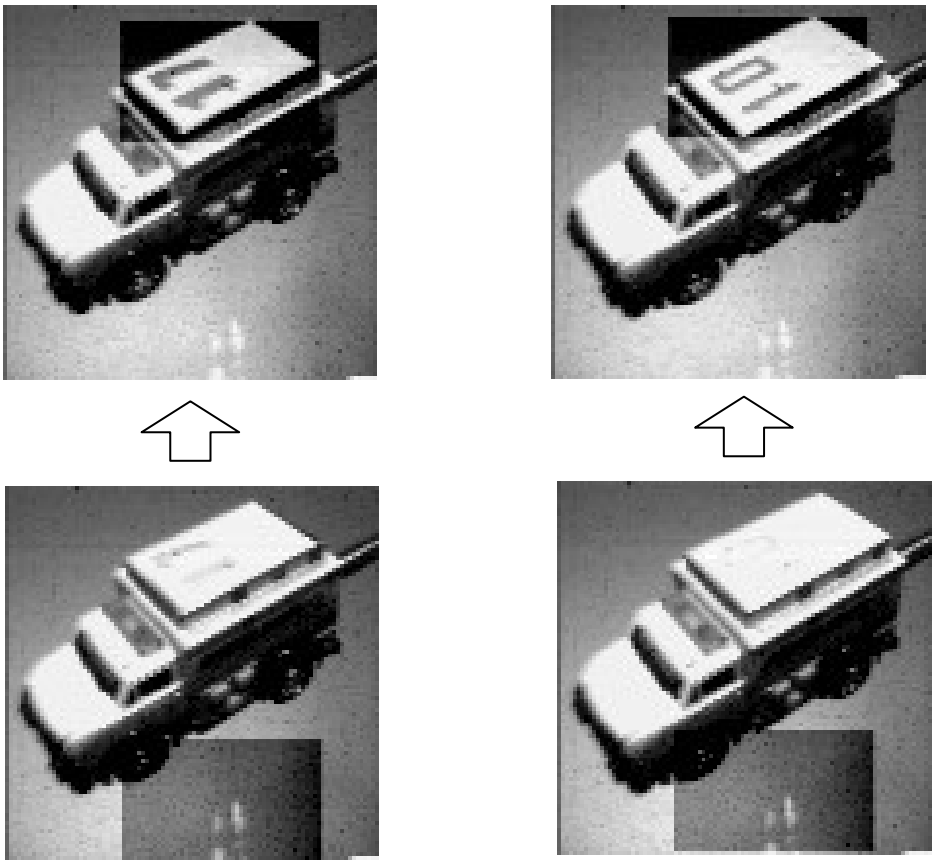


Figure 6.12. ROI enhancement examples.

6.7. FPGA test system

The FPGA-based infrastructure has been utilized as a functional and versatile tool for signal generation and FPA testing and characterization. It presents characteristics that facilitate the operation, offer flexibility on connection and measurement of all signals, and improve the visual analysis of waveforms. Its main features are:

• The online, autonomous, individual adjustment (via software) of signal parameters (Figure 6.13)

• Phase and size-adjustable pulse generation for testing of specific blocks with multiple digital and analog inputs.

• Synchronized ramp-signal generation for analog response and clock feedthrough analysis.

• Repetitive pulse train for access to a specific pixel of the matrix for characterization and testing of related analog circuitries.

• Differentiated frame-sync, line-sync, pixel clock, and clamp signals for synchronization of an external frame grabber.

• Generation of a 2D image pattern of individual-biased pixels (Figure 6.14); defined on code compilation.

• Generation of a biased region of interest based on vertical, horizontal, and square shapes, with adjustable size and position at pixel-size resolution (Figure 5.25).

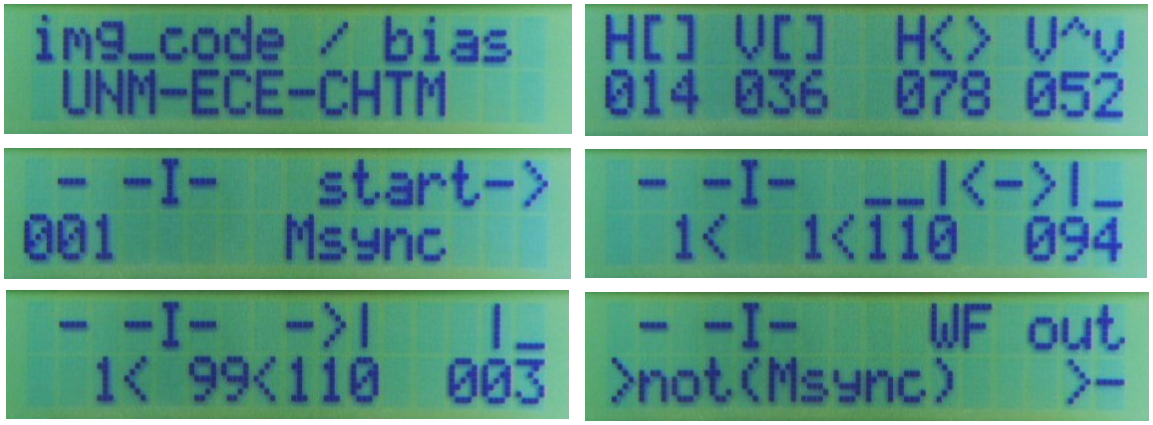


Figure 6.13. Online individual adjustment of signal parameters.

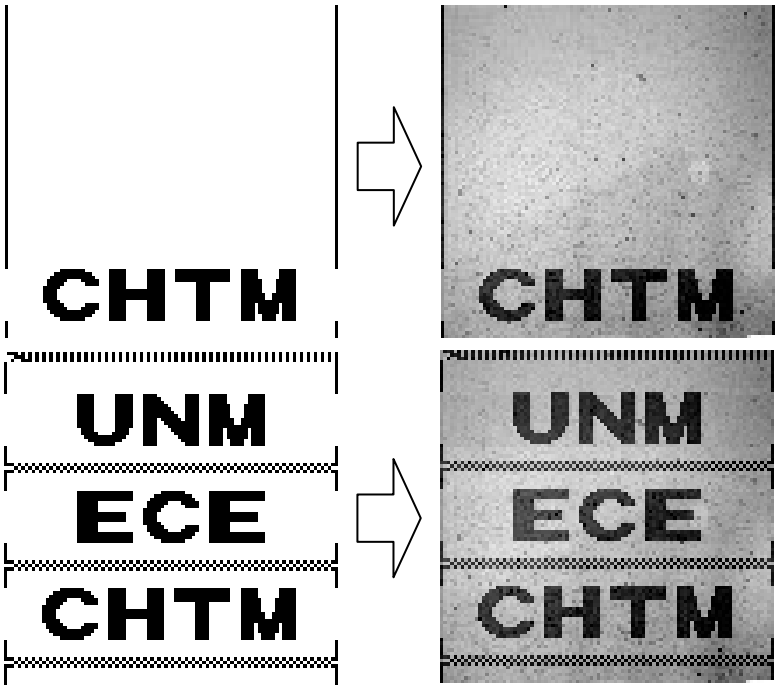


Figure 6.14. 2D image pattern applied to BIAS and acquired from ITP-ROIC.

6.8. PCB and interconnections

The adopted procedure for wire bonding the dies on an open cavity LCC carrier, together with the ZIF socket and specificly designed PCB, allowed a flexible, quick, safe, practical way to access any test structures inside the chip, increasing the number of test structures by chip.

6.9. DAC bias and ramp generator

The DAC software block was successfully able to create one important feature of the test system: the bias voltage generation for each pixel on its related selection and writing-time window. In addition, a triggered pulse with controlled parameters (minimum voltage, maximum voltage, and step size/clock division) was generated, the features of which permit the clock feedthrough characterization, via a gate-voltage slew-rate control (Figure 6.15).

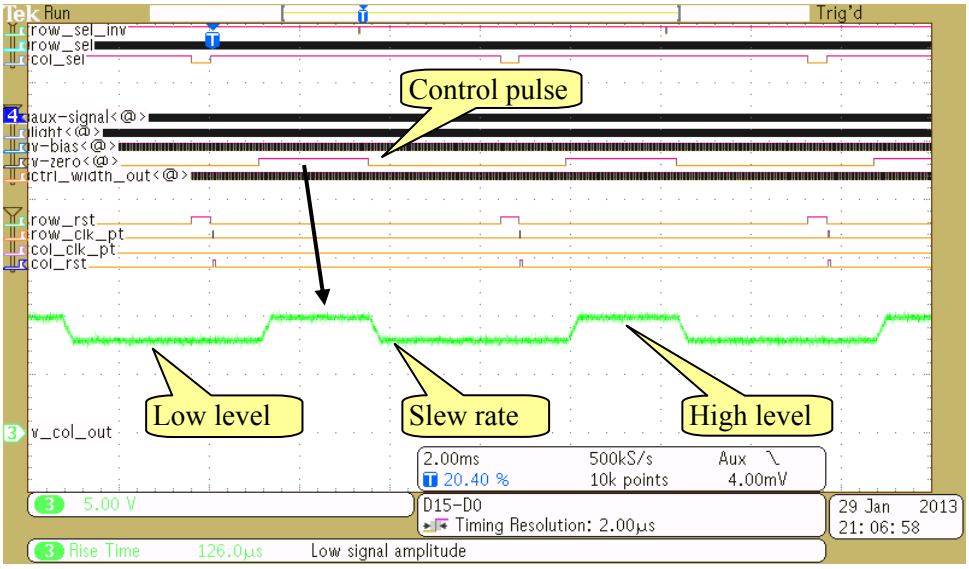


Figure 6.15. Integration switch gate-voltage waveform with controlled parameters.

The programming time of the 4-output DAC initially was established on a minimum of 2 µs, but unfortunately, the settling time of the DAC reached a minimum of 3 µs on measurements, although it could reach as high as 10 µs by the datasheet. This settling time defines the minimum period for the pixel clock in the actual system, if using the onboard DAC for biasing, and ideally it should be 0 µs.

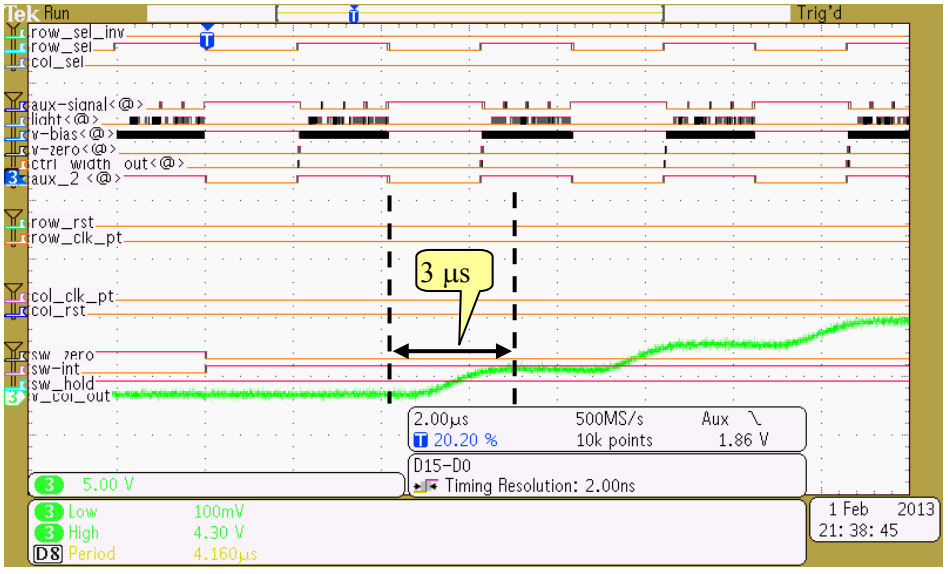
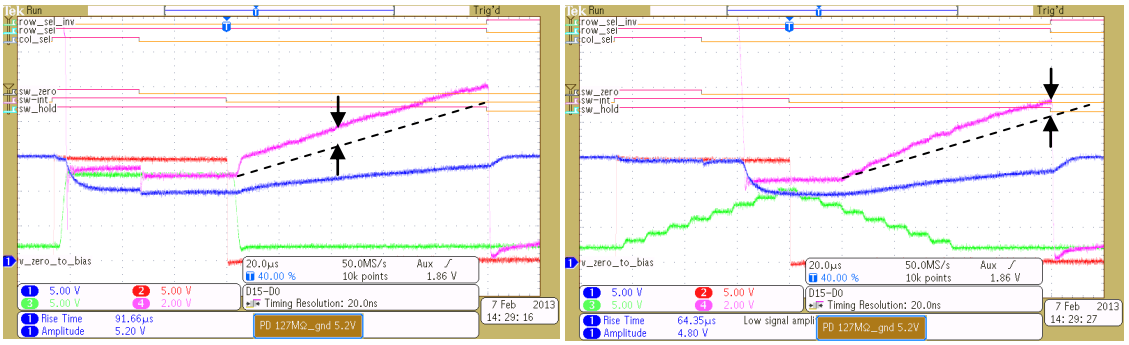


Figure 6.16. Settling time of DAC output voltage @ 4.16 µs pixel clock.

This means a maximum clock frequency of 333 kHz and 30 ms necessary to define the bias on all 10,000 pixels. Adding 245 ms of maximum adopted integration time, the frame time will be 275 ms, resulting in a minimum of 3.63 FPS. This value is not so different from the planned 3.78 FPS (@ pixel clock of 2 μs), showing that the integration time is the main factor that defines the FPS rate. Again, this is a limitation only for the onboard DAC in defining the individual bias with the high resolution of 5 mV.

6.10. Clock feedthrough

When testing the separated unit cell, an offset was observed in the integration signal (Figure 6.17 a), likely due to the charge injection via the gate-source capacitance, which resulted from the high-voltage variation that occurs in a short time (clock feedthrough). Controlling the slew rate of the gate voltage reduced the initial voltage differential, but as shown in Figure 6.17 (b), an integration of this charge still occurs over time. More tests are planned with the adoption of a DAC with better features, with the characterization of one cell inside the FPA matrix and with an improved design for the integration switch.



(a) (b)

Figure 6.17. Clock feedthrough effect (a) and slew-rate control compensation (b).

An offset compensation on the output signal would be an option, but for the actual system, it seems that this effect occurs on all pixels and that it is compensated on the final

image due to the frame grabber voltage-range adjustment.

6.11. VGA controller

Initial tests were made with a VGA controller block [47] for a 640 x 480-pixel resolution image on an external monitor, proving that autonomous monitor controlling could be achieved (Figure 6.18). Unfortunately, it would be necessary to implement an analog-to-digital (ADC) conversion block, a dual-port RAM memory, and a synchronization block, to transfer the image from the FPA to the memory and to read the RAM to the VGA control block, with independent clock frequencies. Due to time limitations, this phase of the project was left for later development.

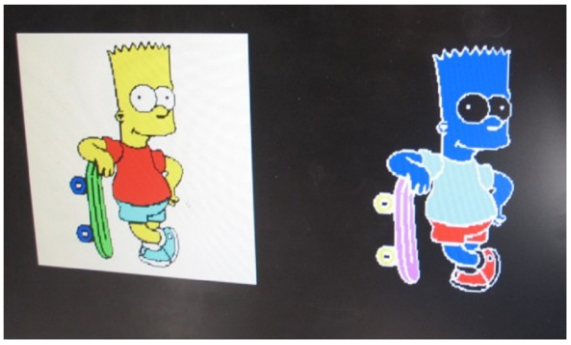


Figure 6.18. Images from FPGA ROM memory (a) and processing (b) [47].

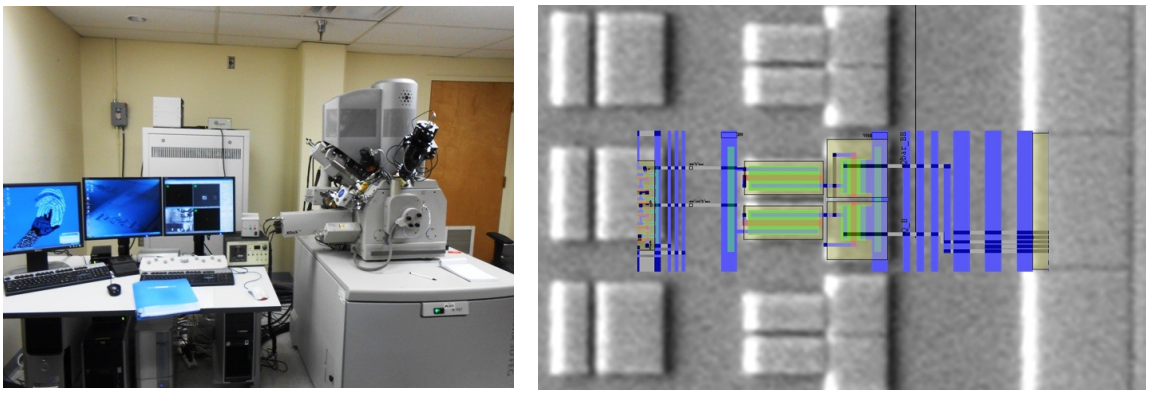
6.12. Chip recovery

During initial testing of the FPA, it was noted that the SW-BIAS on each pixel was not being activated by the internal AND-gate. This problem was detected with the injection of a triangular waveform in the V-ZERO pin, with the SW-ZERO enabled. Independent of SW-INT and SW-Hold, after each pixel is selected by the column and row selectors, the respective voltage should appear on V-BIAS, which did not occur. Furthermore, keeping SW-INT and SW-Hold on, each unit cell should work as a buffer, transferring

the V-ZERO voltage to the output, which did not happen. Because the column selector was working–and the row selector is an exact copy of it–it was suspected that the row colum level shifter was defective. The level shifter for the column selector is different from the row selector, increasing the probability of a defect in that circuit. In addition, if no row is selected, the backup plan of Row0_UNM would not work.

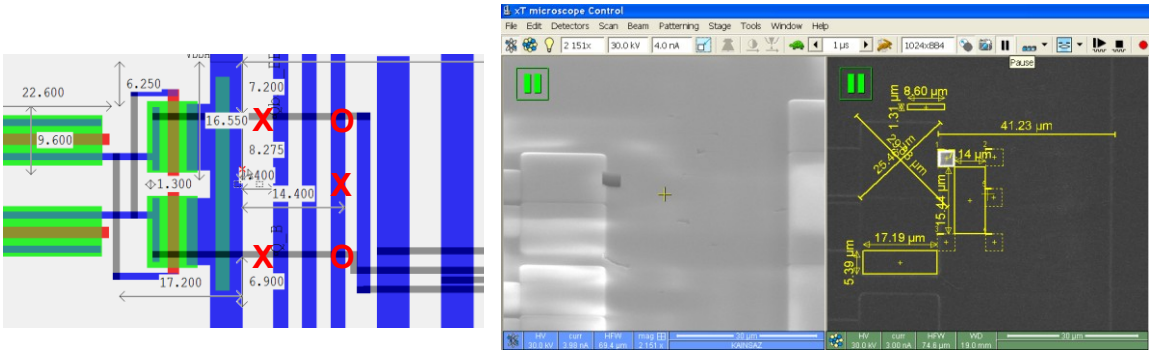
In an attempt to recover chip functionality, at least for one row selection, the use of the focused ion beam (FIB) was planned (Figure 6.19). The chip has available two floating internal pads that could be connected to row_select and row_select_bar of Row 97, after cutting the metal connection between the level shifter and unit cells of that row.

To locate the points to be cut (etched), filled, and connected, the design's layout was measured in the same way the SEM image (Figure 6.20). Unfortunately, the FIB process, although able to execute the cutting, filling, and metal depositing, destroyed the silicon structure near the processed points, which short-circuited the access points to the ground. Figure 6.21 shows the etched and filled holes, the deposited metal tracks, and the collateral destructive effects.



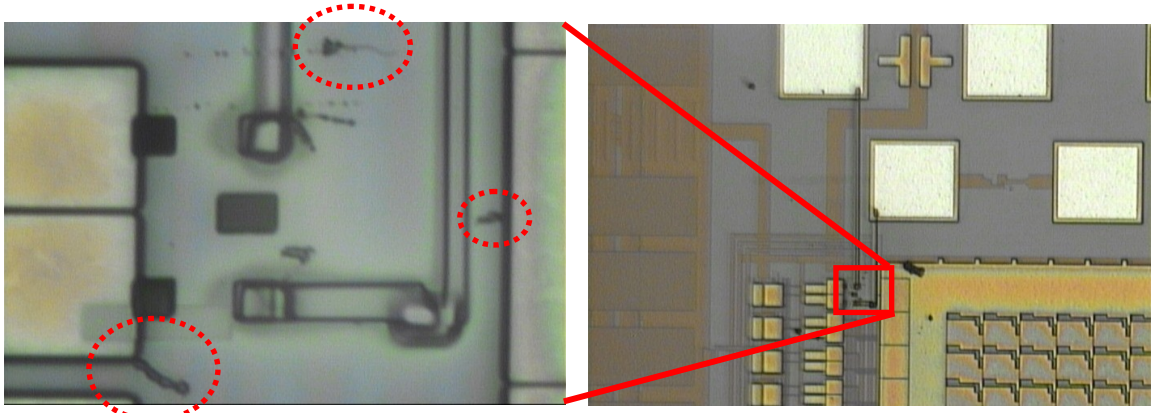
(a) (b)

Figure 6.19. Focused ion beam (FIB) equipment (a) and layout over SEM image (b).



(a) (b)

Figure 6.20. Planned cutting/filling locations on design layout (a) and on SEM image (b).



(a) (b)

Figure 6.21. Details of final work with the collateral effects (a) and overall view of processed area (b).

6.13.2 x 2 matrix

With chip recovery using FIB not successfull and with the designed chip unable to demonstrate the spatial feature–with different biases on pixels in different positions–a backup plan to build a small matrix using separated unit cells was undertaken.

The 84-pin carrier could accommodate four dies in a 2 x 2 matrix in the same way that the necessary pins for the unit cell operation, including the output current mirror, could be wire bonded to one side. Figure 6.22 shows a wire-bonding and carrier interconnection diagram with several biases, and the connected control pins of each unit cell. A matrix of two columns and two row selection lines has to be provided by the FPGA system.

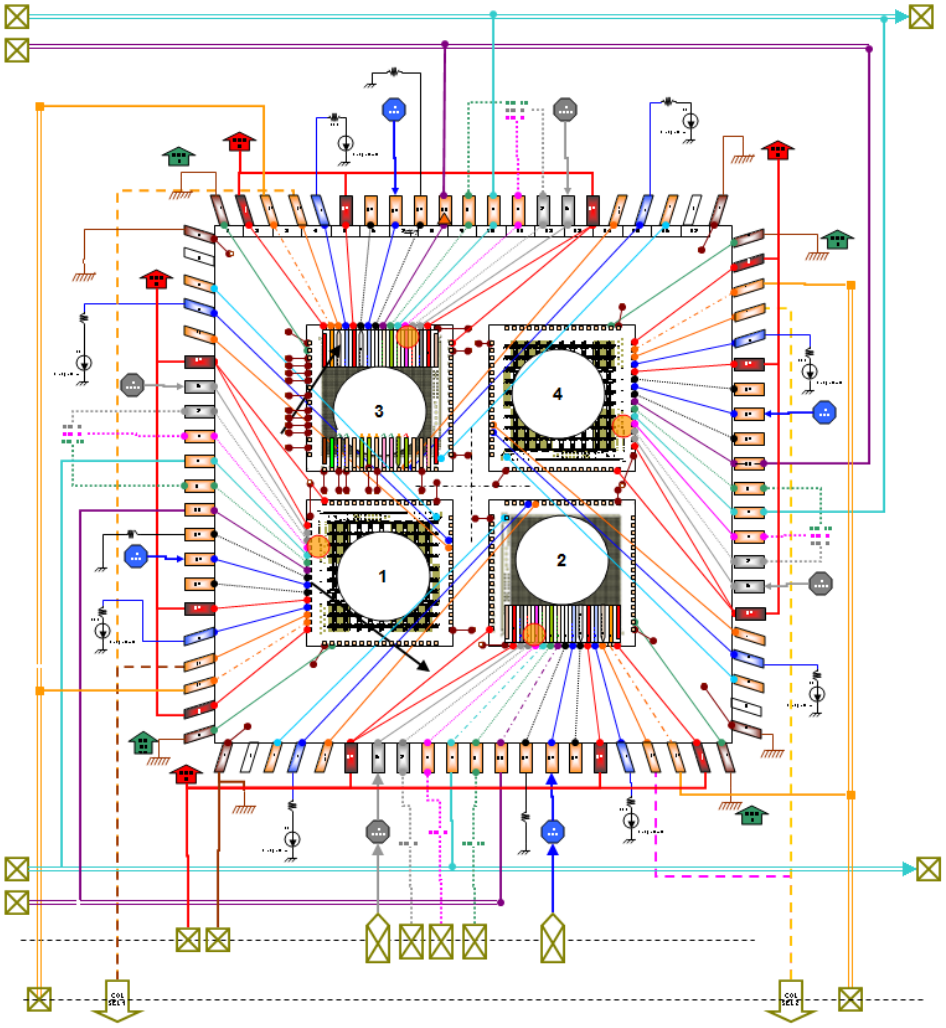


Figure 6.22. A 2 x 2 matrix of individual unit cells with external column/row selectors.

After the wire bonding on the carrier and the elaboration of the interconnection diagram, a solution was found for the level-shifter problem, and the chip responded, discontinuing this phase before the VHDL code could be elaborated.

Nevertheless, the 2 x 2 matrix remains useful, as intended, with each side of the carrier having one unit cell for individual characterization or use. Furthermore, access to the interconnections of columns and rows offers conditions for specific voltage measurements and analysis, which does not happen with the full FPA.

6.14. Problema solucionado

Concentrating analysis efforts on the suspect circuit design–the column-selector level shifter–a discrepancy was observed on the sizes of transistors on the input of the level shifter and on the output of the column selector (Figure 6.23). These transistors present 20 µm and 0.9 µm, respectively, which represents a ratio (of fan-out) of 22.2 of size and of capacitance. In addition, the smaller transistor works at low voltage (3.3 V) and the larger transistor operates at 15 V, presenting a gate-source threshold voltage of up to 2 V.

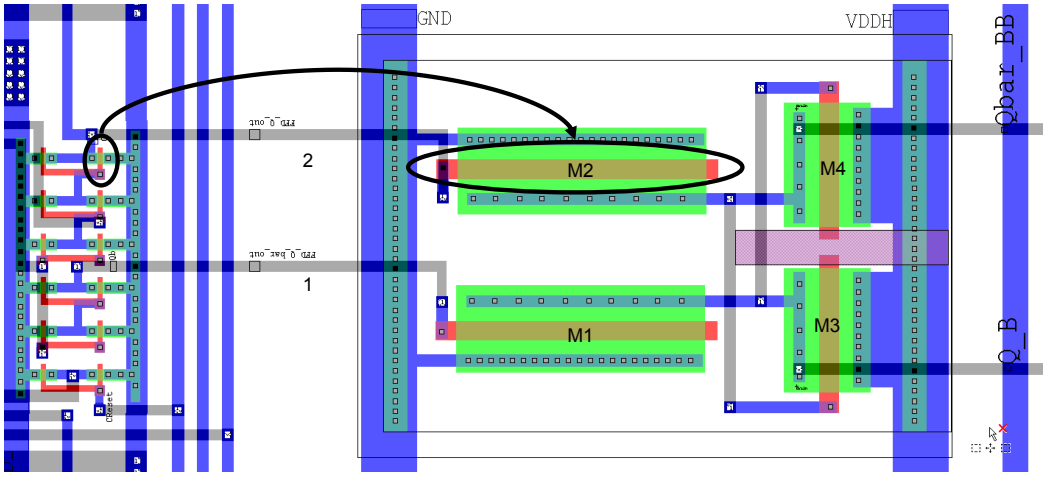


Figure 6.23. Fan-out of the low voltage FF output to the high voltage level shifter input.

For minimum delay, it is recommended [48] that the design ratio between chain transistors should be four. The operational column-select level shifter has a total ratio of 32.09, much bigger than the row-selector chain, but it consists of two inverters at ratios of 5.56 and 5.8. To reduce the difference of operational points of the low-voltage and high-voltage transistors, the low-voltage power supply was increased from 3.3 V to 3.5 V and the high-voltage power supply was reduced. Monitoring the waveforms, it was noticed that the SW-BIAS begin to work when the high-voltage power supply was reduced from 15 V to 9.75 V. And consequently, the ITP-ROIC proved its functionality.

Chapter 7

Conclusions and future work

7.1. Conclusions

A new wide dynamic range, high voltage, dual polarity, individually tunable bias ROIC test chip was successfully designed, fabricated, and tested. The test chip contains a 96 x 96 array of unit cells and controlling logic circuits for readout functionality. Based on the TSMC's 0.35 μm CMOS process technology, the layout of the unit cell was designed to meet the 30 μm pitch requirement for the DWELL-FPA. A flexible test and characterization system with online, autonomous individual adjustments (via software) of signal parameters was developed, permitting its use on upcoming similar projects. The successful design of the proposed ITP-ROIC lays a solid foundation for future applications of infrared FPAs such as the infrared retina, classification cameras, and remote sensing imagers.

7.2. Future work

The knowledge and experience acquired during the development of this project permits improvements related to the design, software, and hardware of a continuing work, described as follows.

7.2.1. Design

- The design of a new ITP-ROIC version that has improved operational characteristics, in the manufacturing process at MOSIS. The SW-BIAS will assume the function of SW-REF as a result of an implemented feature on the row

and column selectors. This also liberated an area on unit cell layout to improve the voltage swing on output.

- The level shifter on the row selector layout was redesigned and now is similar to the one on the column selector to solve the main problem found on ITP-ROIC Version 1.
- Individual transistors must be designed to reduce the metal 1 layer area that covers most of the actual cell.
- Make two individual transistors, one uncovered and one covered with metal 4, for comparison of the light effect.
- Cover the entire chip with metal layers to avoid scattering and collateral light effects, as had happened on this version with its exposed areas. For this we need to work on metal 3 and metal 4 layers, because the DRC requires a dilatation margin on metal.

7.2.2. Hardware

- Testing and characterization of the ITP-ROIC at lower temperatures are planned, with a gradual reduction of its values, to identify the operational range of the CMOS devices and structures at low temperature, using the temperature controller on SE-IR system, which will need to receive a new adapter for the LCC socket to fit on it. This is necessary once: “It should be mentioned however, that silicon-based MOSFETs show a number of operational difficulties conditioned by the very low temperatures required for the readout circuits for these detectors. They are related to freeze-out of thermally generated charge carriers, making the

circuits unstable, increasing noise, and causing signal hysteresis. They are described in details by Glidden et al."[50].

- Power supplies with a shutdown control pin [49] to turn off its output are presented as a better option to manual mechanical switches, in which current passing through could generate heat, losses, noise, or oscillations of voltage of the test system.

- Implementation of a DAC with high-speed conversion output for fixed pattern noise (FPN) correction via BIAS compensation is necessary.

- An external DAC block with better settling time (less than 0.1 μs) could be defined to offer a higher pixel clock rate, to offer a faster individual pixel biasing for the test system and consequently a better FPS rate.

- An specific PCB containing the electronic circuits—analog and digital level shifters, input/output analog buffers, power supplies, and current bias generation—, for interface between the FPGA board and the carrier PCB can offer more stable and reliable interconnections, reducing the noise, facilitating interconnections for new testing setups.

7.2.3. Software

Not all initial desired features could be implemented due the limited time and to the actual limit of program memory on the adopted FPGA board.

Needed now:

- Optimization of the software, reducing the number of counter/muxes to the

minimum possible, liberating space on hardware of the FPGA for other block's implementation, and keeping its operational specifications.

- Design, tests, and implementation of the following software blocks: FLASH memory, to store variables and setup values, reducing the number of counters/memory; ADC for image acquisition; and DDR SDRAM for acquired, processed, and stored images.
- As described in Sections 4.11 and 5.5, a VGA controller can be implemented to display not only a graphical user interface to adjust the signals parameter but also to display an individual pixel biasing screen and the aquired image from the ITP-ROIC, in this way substituting the external frame grabber and making the FPGA system autonomous. In a like manner, another FPGA board could be programmed to be used as a frame grabber, receiveing only video and synchronization signals, liberating hardware resources for the test and characterization's main system.
- USB or RS-232 interface for transferring of stored images in a standard image files format.

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