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Fabrication of Oxide-Based Memristors for Neural Networks

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Fabrication of Oxide-Based Memristors for Neural Networks

by

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B.S. Electrical Engineering, University of New Mexico, 2018

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Dedication

To all the LGBTQIA+ scientists who came before me and the ones who will also follow in the future.

My special thanks to Dr. Alan Turing and Dr. Lynn Ann Conway, notable contributors to computer design and semiconductor foundry processes, whose seminal work I benefited from.

"My silences had not protected me. Your silence will not protect you."
– Audre Lorde

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Abstract

This thesis discusses what a memristor is, how it is hypothesized to work and the fabrication work undertaken with hafnia and titania-based ultrathin oxide films. In addition, the electrical tests utilized to characterize the physical performance of the memristors including but not limited to, their IV hysteresis responses, yield rates and overall reliability. The results and discussion of this work are aimed at better understanding how fabrication of memristive devices can be further improved for future work.

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Chapter 1

Introduction

Definition: What are memristors or resistive random-access memory (RRAM)?

Memristor is a portmanteau of memory plus resistor which describes the unique electrical characteristics of this device. Memristors were first hypothesized as a possible fourth class of passive circuit element, extending beyond resistors, inductors and capacitors in the 1970s [Chua 1971]. Unlike ordinary static resistors where there is a fixed value of resistance that does not change based on voltage or current (unless the resistor experiences dielectric breakdown and ceases to function as such), a memristor's resistance state is dependent on the voltage bias applied to it.

Per Chua, the voltage across a memristor is shown in Figure 1.1:

$$v = M\big(q(t)\big)i(t) \text{ where, } M(q) = \frac{d\psi(q)}{dq}$$

Figure 1.1: Equation for modeling for a memristor's behavior.

Ergo, the resistance state of the memristor changes in time based on the time-varying voltage applied to the circuit element, etc. So while the resistance appears fixed at a given moment, this is highly dependent on the flux of the charge across the memristor [Chua 1971].

When a forward (positive) voltage is applied at a sufficiently high level, the resistance of the memristor drops to a low enough level that it behaves as a short circuit. When a reverse (negative) voltage bias is applied, the memristor returns to a high resistance state. The circuit element can then be made to cycle between the high and low resistance states by biasing the element with forward or reverse voltage. The critical point for a functional memristor is that it holds the high or low resistance state when a low level of voltage is applied to read the existing state, much like other forms of random-access memory. However, unlike SRAM or DRAM, the high or low resistance state holds true without an active voltage source, making it a non-volatile form of memory. However, it is possible to rapidly cycle states in a fashion similar to conventional random access memory. Hence, memristors have also been colloquially referred to as resistive random access memory (RRAM) devices. RRAMs' potential capabilities have value in several different applications **[**Jeatrakul 2009].

Why Memristors?

Memristors will have applications in both neuromorphic computing and radiation hardened electronics used in space and systems designed to survive exposure to higher than average levels of gamma, beta, and alpha radiation that may exist either in an environment exposed to radiological nuclides from their presence in a post-nuclear release event of a significant scale or in exo-atmospheric conditions, i.e. deep space or orbital platforms.

In the first case delineated, the RRAM can have varying levels of high or low resistance that are not restricted to a binary state of 0 or 1 (off/on). The varying resistance states can represent the weighted probabilistic values of a statistical model used to train a neural network

much more efficiently than the ordinary SRAM/DRAM that is currently used to hold the weighted values; an individual RRAM can hold one weighted value, whereas binary memory requires multiple instances of capacitors or bistable latch circuits to hold a single instance of a probabilistic weight as a binary string [Radwan 2015]. This would enable the implementation of neural network algorithms in a much more energy and computationally efficient fashion than ordinary SRAM/DRAM implementation, allowing them to be scaled down into applications like radiation detection, search functions for independent data analysis in autonomous drone platforms, etc.

In the second case of radiation hardened electronics, unlike ordinary SRAM/DRAM devices, the RRAM would have the potential capability of retaining its ON or OFF state regardless of ionizing radiation incident on the platform.

Currently, space-based electronic systems require that either a significant portion of the mass of any launched satellite be either consumed by radiation shielding to ensure the safety of internal electronic hardware, or that the electronics all be hardened against radiation, or that the performance of the system not be degraded within a reasonable time frame before adequate data is gathered by the satellite and software corrections can be uploaded by ground control systems on the planet Earth [Ma 1989].

The reason this problem exists is because satellite systems in orbit about the planet are exterior from the Van Allen radiation belt which normally blocks the grand majority of the ionizing radiation incident on the planet as well as most cosmic rays, which has the inadvertent effect of acting as an electromagnetic interference (EMI) shield, which most semiconductor electronic systems benefit from. Both ionizing radiation and cosmic rays possess the ability to short out ordinary binary-valued semiconductor devices. Alpha radiation incident parallel to a RAM array can change the entire row of memory states (flipping from 0 to 1 or an unreadable state), rendering the information returned from the memory completely invalid and a beta particle can force a change from 0 to 1 in a MOSFET, etc. [Ma 1989].

Because memristors are a more strongly non-volatile system than ordinary SRAM or DRAM devices, they can be exposed to ionizing radiation without suffering as many adverse changes in the logic states being held in memory. This reduces the amount of EMI or ionizing radiation shielding needed onboard the orbital platform for preserving the functionality of the logic circuits, enabling improved computational capabilities without dramatically increasing payload lift demands to bring a satellite system into the required orbit.

The remainder of this Thesis is organized as follows. Chapter 2 presents hypothesized models describing memristor physics. Chapter 3 presents a description of the memristor fabrication process, geometry, and material stack. Chapter 4 describes the fabrication and characterization of the generations of memristors studied in this work. The conclusions from this work are presented in Chapter 5. Appendix A presents the hafnia memristor fabrication process sheet.

Chapter 2

Hypothesized Models of Memristor Physics

As memristors are a relatively new development in semiconductor devices, the physics driving the material state change from low to high resistance is not completely understood. It has been hypothesized that the forward bias voltage from the V_{CC} to GND induces a weak dielectric breakdown in the oxide layer, creating a filamentary pathway which acts as a conductive channel [Larcher 2012], as shown in Figure 2.1.

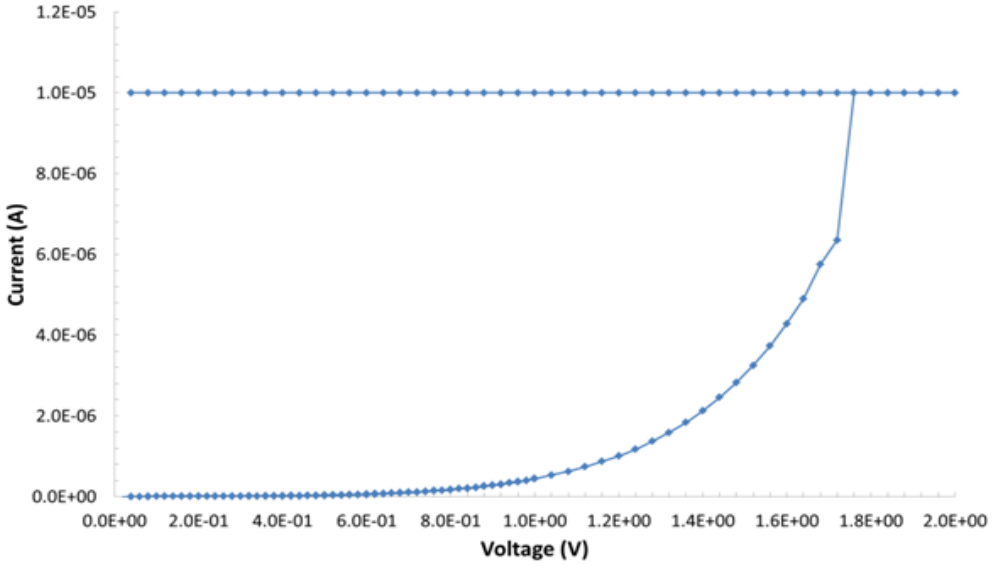

Figure 2.1: Current-voltage formation curve of an RRAM device being set ON [Source: Prior work at Sandia on TaOx memristors].

Reverse bias applied to the device from GND to V_{CC} in turn breaks the filament pathway, forcing a high resistance state which can be seen in Figure 2.2.

By shifting the voltage +/-, the RRAM can be cycled between the high and low states. This in turn generates a hysteresis curve as the resistance changes states between high and low (or ON and OFF) as the filament forms and breaks repetitively as can be seen in Figure 2.3.

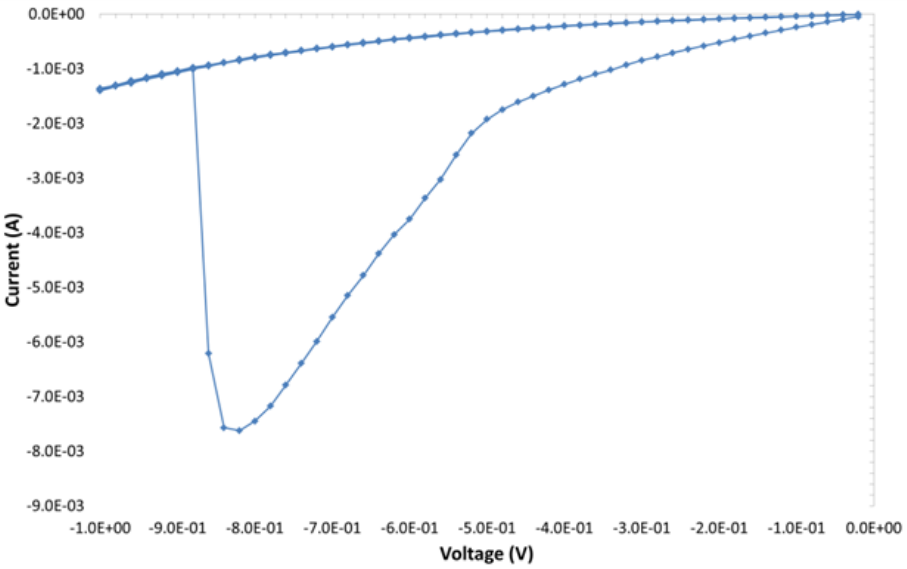

Figure 2.2: Current-voltage breakdown curve of an RRAM device being set to OFF [Source: Prior work at Sandia on TaOx memristors].

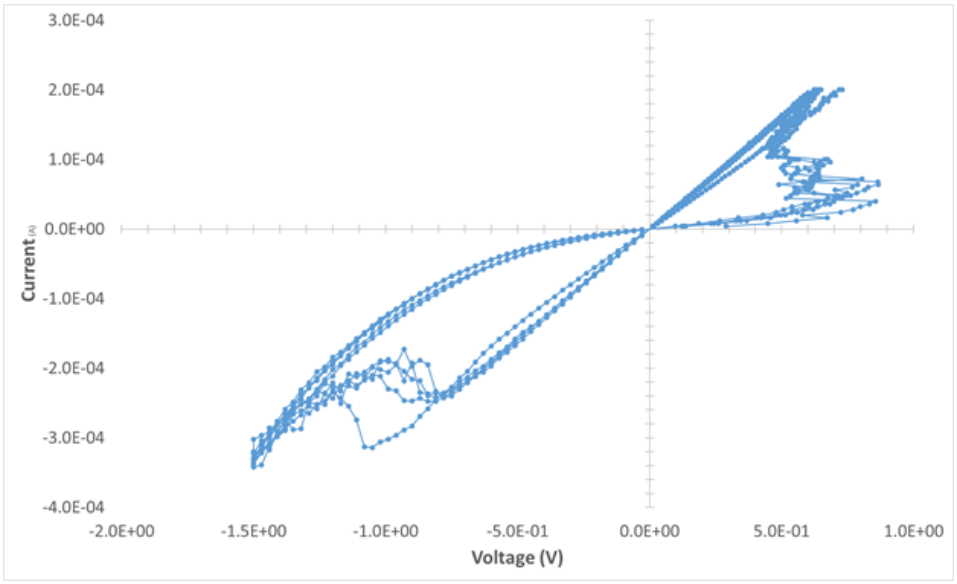

Figure 2.3: Current-voltage hysteresis curve of a memristor device being cycled ON/OFF repeatedly [Source: Prior work at Sandia on TaOx memristors].

While this hypothesis is widely accepted as a possible explanation, Schmitt, et al. take a different view of the material physics and hypothesize that the conductance changes are due to the movement of oxygen ionic charge carriers to oxygen vacancies in the high electric field [Schmitt 2017]. However, the precise mechanism that would enable such changes remains unexplained and proving this hypothesis empirically is problematic at best.

At the time of this writing, I favor the conductive filamentary model due to it being directly testable and a more precise description of the process of how the RRAM undergoes the state changes. However, it is worth noting that the filamentary model suggests a technically significant challenge in RRAM design as it is likely that filamentary breakdown can occur only so many times before the cell burns out, undergoing irreversible dielectric breakdown and shorting to an ON state on a permanent basis. The unanswered question then becomes how to engineer the RRAM to have a lengthy duration of functionality so the failure rate vs. time does not become an impediment to broad scale implementation.

Chapter 3

Overview of Memristor Geometry, Material Stack, Fabrication Process, and Characterization

3.1 Device Geometry Description

The RRAM is fabricated in a crossbar pattern array, allowing for rapid production of pseudo-neurons holding multiple states. The initial proposed crossbar array is shown in Figure 3.1.

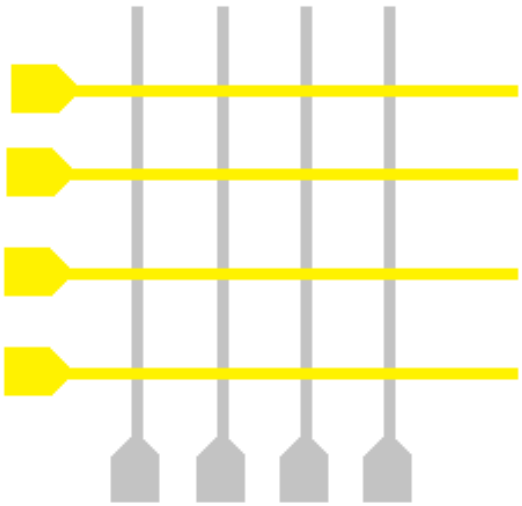

Figure 3.1: Crossbar pattern draft.

The proposed mask file in AutoCAD for the memristors can be seen in Figure 3.2. Initially it was planned that the AutoCAD mask would be utilized, but after discussion with CINT scientists and examination of pre-existing masks there, an existing hard mask was selected for use in the early fabrication of the prototypes to expedite device fabrication.

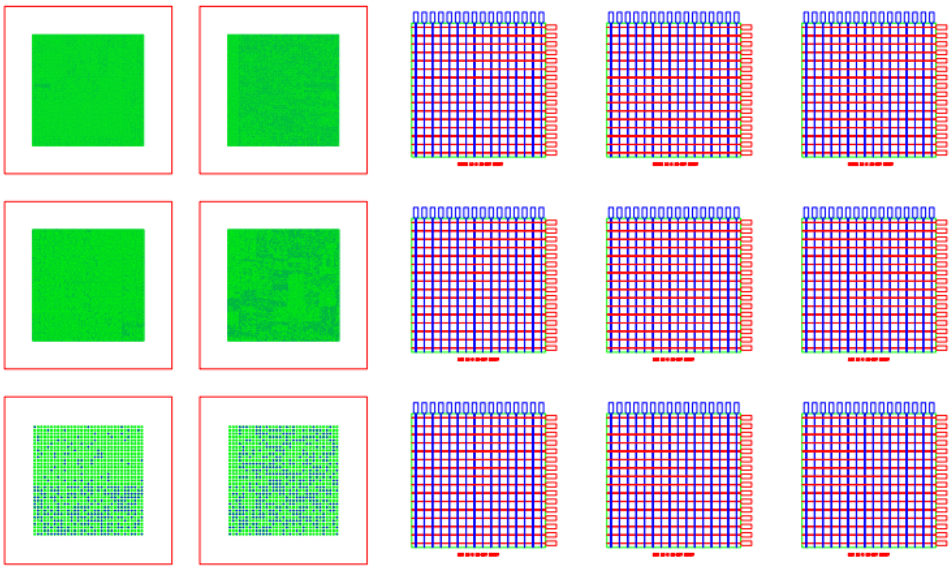

Figure 3.2: AutoCAD mask draft design file.

3.2 Memristor Material Stack

The electrodes and contact pads are patterned via optical lithography or electron beam lithography. The 10 to 1 micron range of devices can be fabricated using optical lithography. However, the sub-micron range from 500 nm to 50 nm requires the use of electron beam lithography to reach the smaller dimensions. After the bottom electrode pattern is deposited via metal evaporation, the ultra-thin oxide layer is deposited using stoichiometric processes in an atomic layer deposition reactor. The top electrode is then patterned via lithography perpendicular to the bottom pattern and deposited again using metal evaporation. The generalized material stack for the memristors is shown in Figure 3.3.

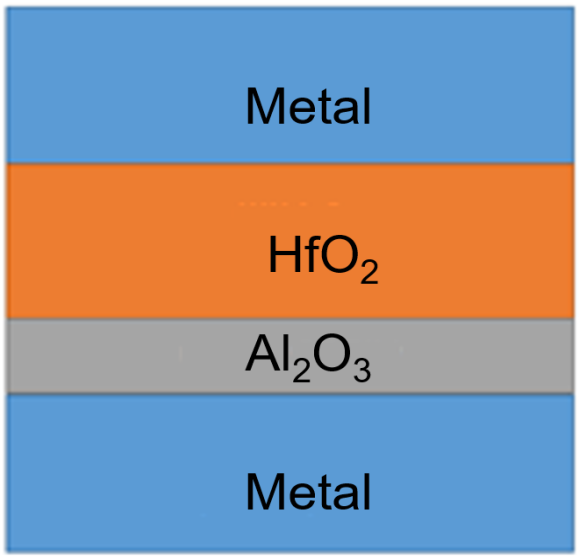

Figure 3.3: Metal-Insulator-Metal (MIM) memristor stack.

The metal-insulator-metal configuration is preferable for production purposes, in that it enables the memory chips to be wire bonded and packaged with minimal extemporaneous effort. Once packaged into an industry-standard device packed, the RRAM can then be incorporated into printed circuit board design and then utilized as you would any other RAM chip. The precise methodology for the initial fabrication run is as follows. First, the bare substrate will be prepared

using hexamethyldisilazane to promote adhesion bonding between the silicon dioxide and the NLOF 2035 photoresist [Microchem 2018]. Figure 3.4 shows the basic stack height for the raw SiO_2 wafer used as the substrate for the devices.

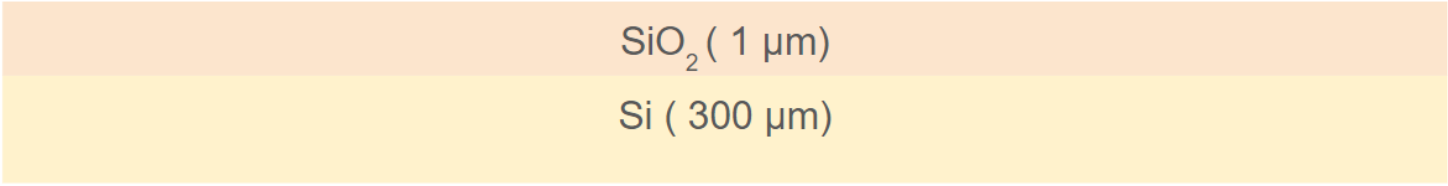

Figure 3.4: SiO_2/Si bare substrate.

The coated sample is then exposed to ultraviolet light and patterned using an optical lithography mask. The sample is then immersed in MIF 300 developer, rinsed, dried and evaluated for proper alignment and good resolution of the pattern. Figure 3.5 shows the substrate prepared for developer.

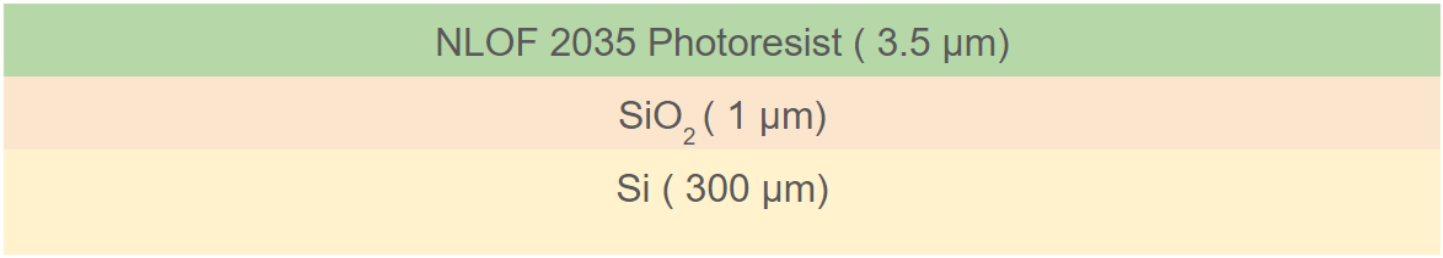

Figure 3.5: Substrate coated with photoresist.

The sample is then coated with titanium via metal evaporation to promote metal to silicon adhesion and then the process is repeated with platinum as show in Figure 3.6.

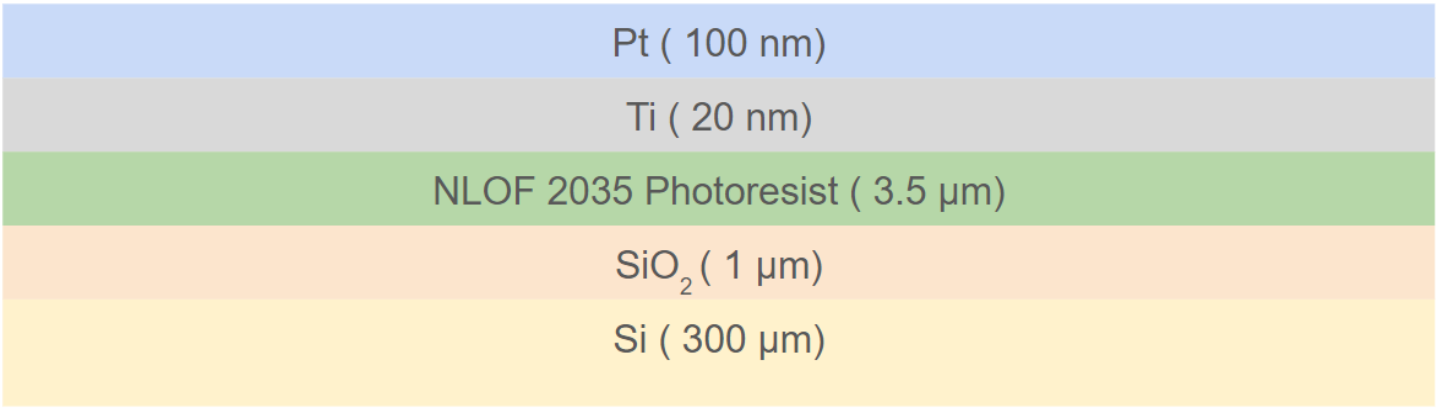

Figure 3.6: Sample pre-lift off.

Once complete, the sample is then immersed in Remover PG, a chemical solution that breaks down the unexposed photoresist and removes the excess metal as seen in Figure 3.7.

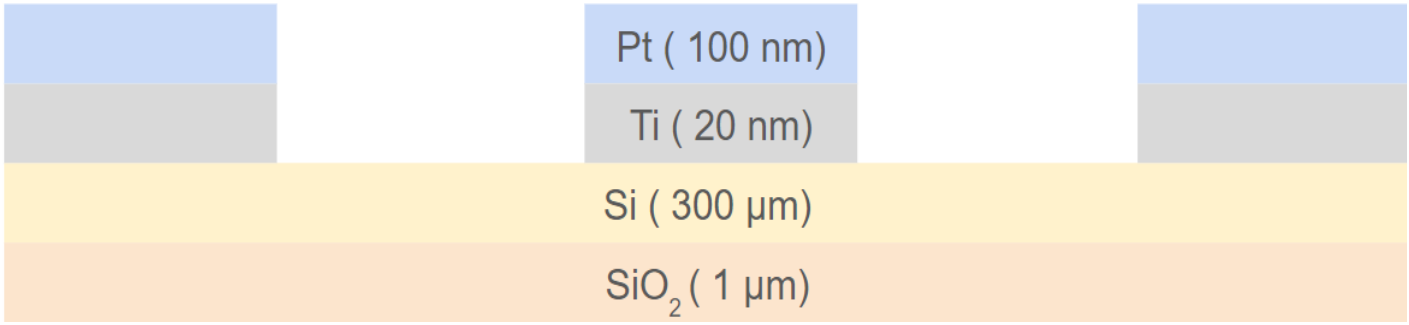

Figure 3.7: Sample post-lift off.

The sample is then inserted into the Picosun atomic layer deposition reactor and coated with alumina and hafnium oxide. The process is highly conformal so the oxide coats both the electrode pattern as well as the bare substrate as demonstrated in Figure 3.8. Fortunately, the oxide covering the contact pads does not disturb the basic functionality of the devices.

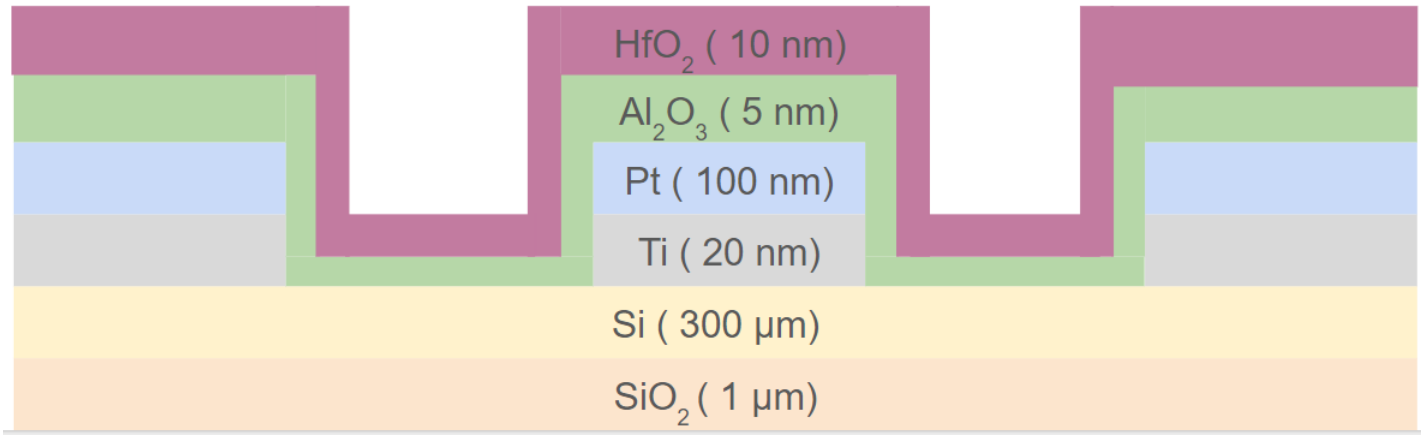

Figure 3.8: Sample stack post-atomic layer deposition.

The sample is then recoated with HMDS and NLOF 2035 in preparation for the final electrode pattern. Care must be taken with alignment at this stage to ensure the pattern is both orthogonal to the bottom electrode pattern and has maximal coverage of the bottom array. Figure 3.9 shows the sample prepared for final metal deposition.

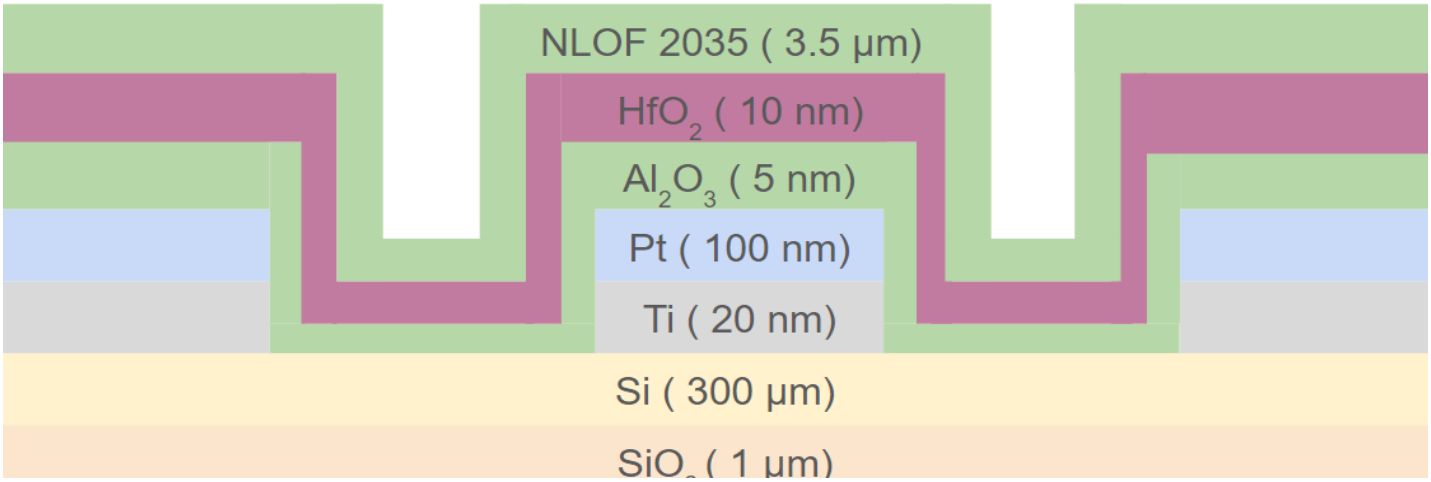

Figure 3.9: Sample coated for the final pattern.

After the sample is developed, optical inspection must confirm the orthogonality of the lithography pattern, then the sample is coated with titanium and gold using a metal evaporator.

The thickness of the top electrode layer should be at least twice that of the bottom electrode to ensure that the pattern does not break during lift off as illustrated in Figure 3.10.

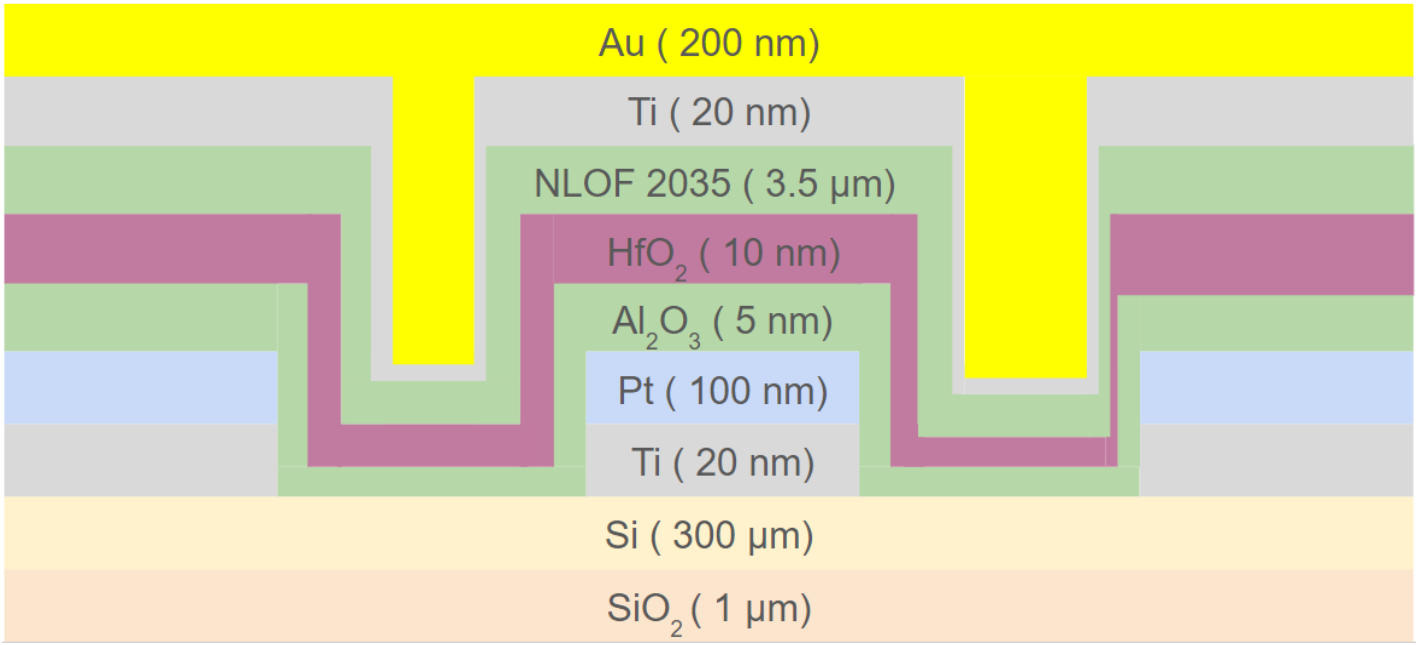

Figure 3.10: Sample post metal deposition and pre-lift off.

Once the deposition has been completed, the samples are placed in the remover compound for a final lift off step and the excess metal and photoresist is dissolved one last time as can be seen in Figure 3.11. The samples are then inspected under a microscope to verify that the pattern adhered properly and the RRAM is ready to be characterized electrically.

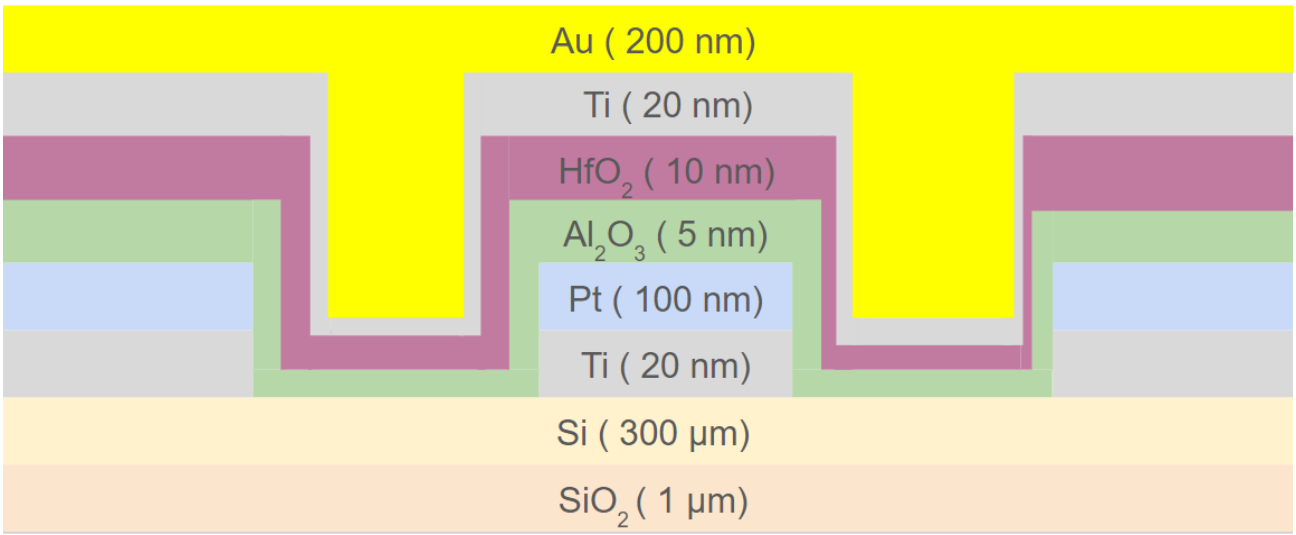

Figure 3.11: Sample cross section post final lift off.

3.3 Electrical Characterization of Memristors

The devices were placed on a plate below a probe station and held in place via vacuum or carbon tape. Once secured, the electrical probes were aligned with respect to the electrode pads and then lowered into place. The B1500A Semiconductor Parameter Analyzer is capable of spot, pulse, and sweep measurements ranging from the microvolt range up to two hundred volts. Current can be controlled to range from the femtoampere range to one ampere as well [Keysight 2019]. This enables greater flexibility in testing as devices can be subjected incrementally increasing values of voltage and current to gauge both stress tolerances and stable functionality.

The samples will be subjected to both positive and negative sweeps to verify the ability to set and reset, then cycles to ensure that they are capable of switching states. Data will be recorded for each sweep for analysis in an .xml file format and then converted either using Excel or Matlab for a more detailed look at how the RRAM behaves when subjected to time-varying positive and negative bias voltage sweeps. Figure 3.12 shows the basic information flow diagram for the electrical characterization sweeps conducted to validate the memristor functionality.

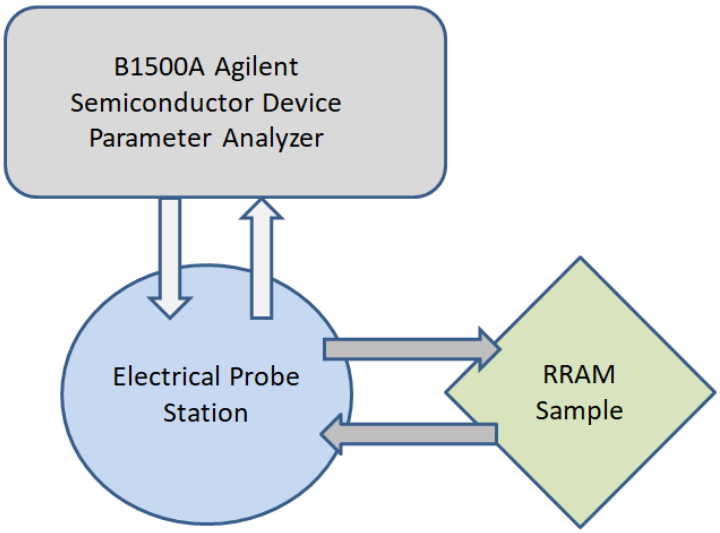

Figure 3.12: Data flow diagram for experiments.

3.4 Summary of Protocol and Potential Challenges

Oxide-based RRAM offers a potential line of inquiry and development as a form of non-volatile memory that has applications in both neural network optimization and ionizing radiation-resistant electronics. Therefore it will be investigated further by:

1) Development of the fabrication process in such a manner that the RRAM can be fabricated with a minimal possible number of defects or anomalies in the devices.

2) Electrical characterization experiments to be executed on multiple devices to develop a statistically robust data set on RRAM performance.

The major challenges are ensuring good resolution of the smaller feature sizes for the photolithography, ensuring proper adhesion of the metal and that the oxide layer is sufficiently thick for good switching and minimal shorting of devices from irreversible dielectric breakdown, but not so thick that it acts as a strong dielectric and prevents filamentary formation from occurring.

Chapter 4

Fabrication and Characterization of Memristors

This chapter discusses the multiple iterated fabrication runs, the characterization of the prototype memristors, the failures and troubleshooting efforts and finally successes of the process development.

4.1 Initial Fabrication, First Generation Memristors

4.1.1 - Fabrication Process, Optical Lithography

Bare substrate samples formed of silicon and silicon dioxide (one micron thick atop silicon) that were diced to one by one inch dimensions were first cleaned with acetone and isopropyl alcohol at the solvent bench, then dried with a nitrogen gas gun set to forty psi. The samples were then placed on a hot plate set to 180 °C and dehydration baked for five minutes. When complete, the samples were then placed on a cooling tray for roughly thirty seconds.

The samples were then coated with hexamethyldisilazane (HMDS), an organosilicon compound that promotes adhesion bonding between the silicon substrate and the photoresist [Microchem 2018]. After HMDS was applied, the samples were then spun on a spinner plate at three thousand RPM for thirty seconds, the HMDS was then soft baked to the substrate by placing the samples on a hot plate set to 90 °C for thirty seconds.

After the HMDS had cooled, the samples were then placed back on a spinner chuck set to three thousand RPM and coated with NLOF 2035, a negative photoresist that is ideally suited to patterning samples with photolithography [Microchem 2005].

The samples were then spun for thirty seconds and then soft baked at 112 °C for one minute. The optical lithography mask was then removed from the storage case, inspected for any visible contamination and washed with acetone, rinsed with isopropyl alcohol and dried with the nitrogen gas gun. The mask was then placed in the vacuum holder and loaded into the optical lithography system. Figure 16 shows the photolithography mask post cleaning under the microscope.

The samples were then aligned on the vacuum plate of the Heidelberg Instruments DWL 66fs Optical Lithography System with respect to the mask and then exposed for six seconds at sixty nanojoules at with the wavelength at four hundred nanometers.

Post exposure, the samples were then soft baked at 112 °C for four minutes and then cooled. This is necessary to ensure that the pattern does not wash away during the develop step and the

pattern becomes clearly visible during the bake. The samples were then soaked in MIF 300 developer solution for ninety seconds and rinsed in deionized water for approximately five minutes. The samples were then dried with a nitrogen gas gun and inspected under the optical microscope to verify the pattern had good resolution on the substrate.

As can be seen in Figure 4.1, a successfully developed pattern is clearly visible and ready for the next steps.

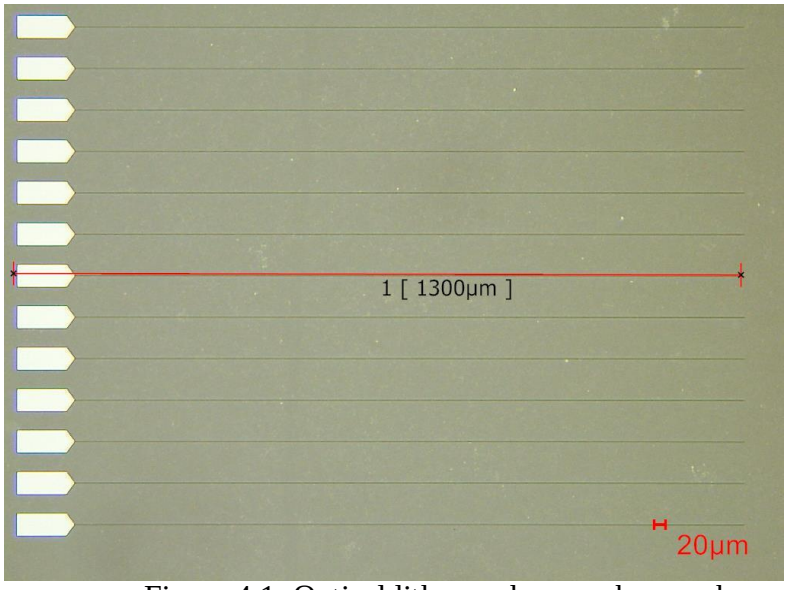

Figure 4.1: Optical lithography crossbar mask.

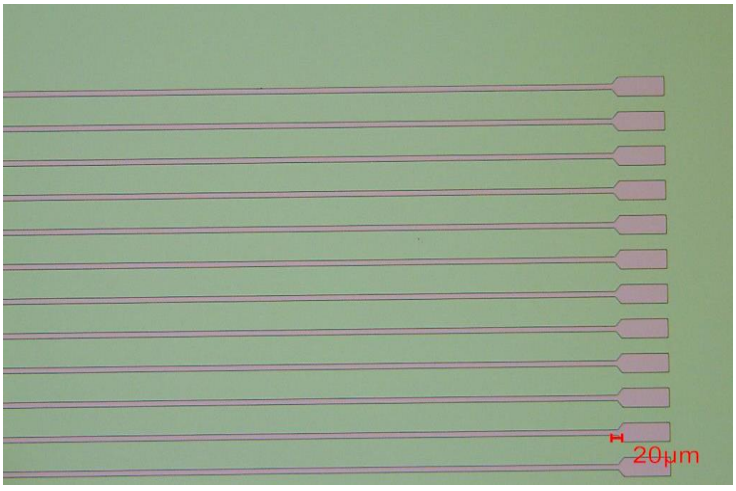

Figure 4.2: Memristor sample, post development step.

The samples were then loaded into the Anatech Inductively Coupled Plasma system and run through a one hundred watt, thirty second descum cycle. This ensured no organic contamination of the surface to promote good adhesion of the metal to the substrate.

The samples were then loaded into the Temescal FC-2000 Metal Evaporation system and coated with fifty nanometers of titanium and two hundred nanometers of gold. After the process was completed, the samples were placed in Remover PG for ten hours to dissolve the photoresist layer. The samples were then rinsed with acetone and isopropyl alcohol to remove any loose

metal film and dried with a nitrogen gas gun. The samples were then inspected under the Keyence optical microscope to validate the success of the lift off process as seen in Figure 4.3.

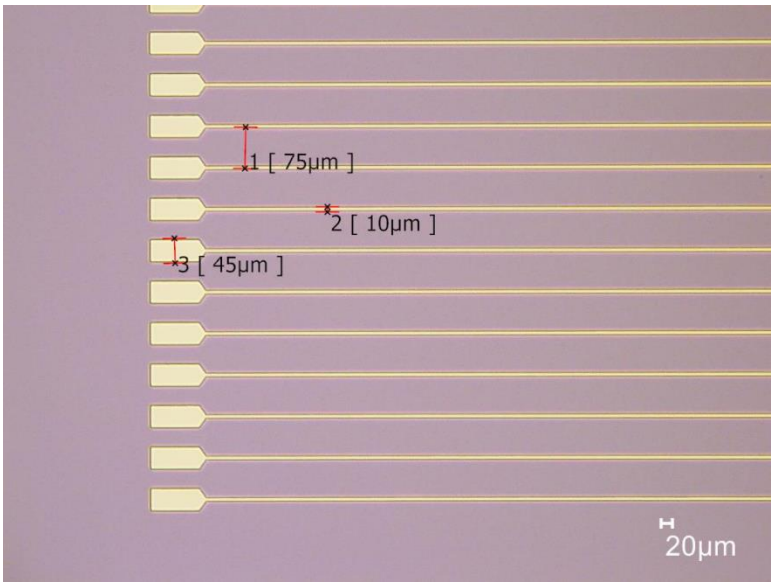

Figure 4.3: Memristor sample, post lift off.

The samples were then loaded into the Picosun Sunale R150 Atomic Layer Deposition Reactor and were then treated with the chemical precursors trimethylaluminum and water at 250 °C to form the aluminum oxide film via stoichiometric process. After the alumina forms to a thickness of five nanometers, the hafnium dioxide layer is then formed using tetrakis (dimethylamido) hafnium (IV) and hafnium dioxide at 250 °C. When the HfOx film reached a thickness of ten nanometers, the process was completed and the samples removed. The visual change from the HfOx deposition can be seen in Figure 4.4.

The samples were then cleaned and prepared for the top electrode layer to be deposited via metal evaporation a second time. The cleaning and coating processes were unchanged, however the samples must be aligned in such a manner that the bottom electrodes are orthogonal to the mask. This requires careful adjustment of the sample positioning and verification of the sample alignment via the microscope attached to the optical lithography system. Once aligned, the samples were then exposed for six seconds, etc.

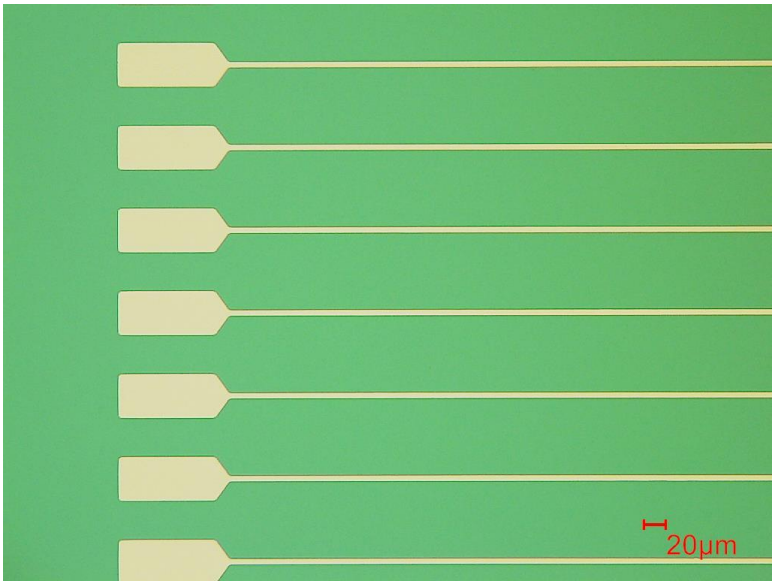

Figure 4.4: Hafnia memristor sample, post atomic layer deposition process.

Post exposure bake and development followed the same procedure, samples were then inspected under the microscope to verify the pattern in the photoresist. The samples were then descummed and loaded into the metal evaporation system, coated with fifty nanometers titanium and four hundred nanometers platinum. The samples were again soaked in Remover PG, rinsed with acetone, isopropyl alcohol and dried with the nitrogen gas gun. The samples were then inspected to validate the crossbar pattern. As seen in Figure 4.5, the crossbar pattern is clear across the whole array when successful and devices can be tested from top to bottom.

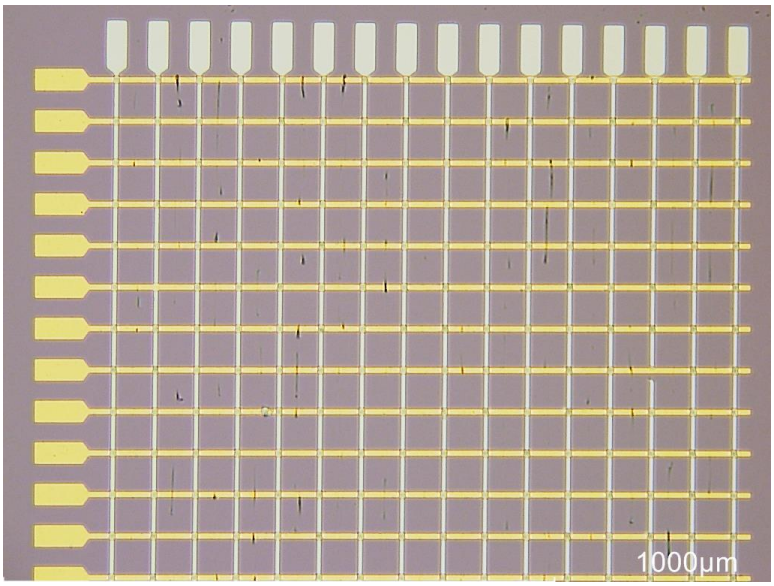

Figure 4.5: Memristor array, post final lift off.

The completed samples were then stored in a nitrogen dry box until the probe station was available for use conducting electrical characterization studies.

4.1.2 – Fabrication Process, Electron Beam Lithography

The samples were cleaned with acetone and isopropyl alcohol at the solvent bench, then dried with a nitrogen gas gun set to forty psi. The samples were then placed on a hot plate set to 180 °C and dehydration baked for five minutes. When complete, the samples were then placed on a cooling tray for roughly thirty seconds.

After the samples cooled, they were place on a spinner chuck set to run at three thousand RPM for thirty seconds. The samples were coated with PMMA 495 A4 electroresist and then spun. After the spin was complete, they were then placed on a hot plate set to 180 °C for two minutes and then cooled. The samples were then placed back on the spinner chuck and coated with PMMA 950 A4 electroresist and spun for a second time. When the spin was complete, they were placed on the hot plate set to 180 °C for another soft bake for another two minutes.

A sample was then placed in the 2F position in the cassette for loading into the JEOL JBX-6300fs electron lithography system. The JEOL system was then calibrated for a beam condition of a thousand micro-Coulombs per square centimeter with a beam diameter of twenty four nanometers with a shot pitch of fifteen nanoamperes to write crossbars with a width of five hundred nanometers.

As each sample's exposure to the electron beam was completed, it was removed from the EBL system and then placed in a solution of MIKB:IPA 1:3 developer for seventy five seconds and then rinsed with isopropyl alcohol and dried with a nitrogen gas gun. The samples were then checked under a microscope to verify the pattern was well developed as can be seen in Figure 4.6.

The samples were then loaded into the Anatech Inductively Coupled Plasma system and run through a one hundred watt, thirty second descum cycle. This ensured no organic contamination of the surface to promote good adhesion of the metal to the substrate.

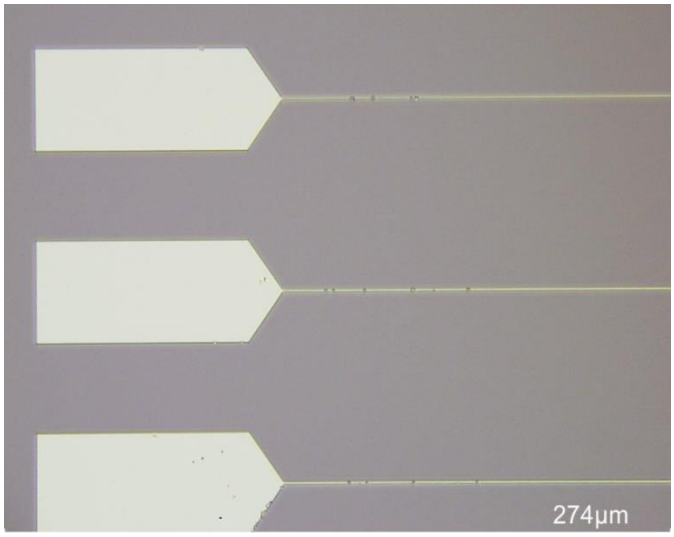

Figure 4.6: EBL sample, post lift off.

The samples were then loaded into the Temescal FC-2000 Metal Evaporation system and coated with twenty nanometers titanium and one hundred nanometers platinum. After the process was completed, the samples were placed in Remover PG for ten hours to dissolve the electroresist layer. The samples were then rinsed with acetone and isopropyl alcohol to remove any loose metal film and dried with a nitrogen gas gun. The samples were then inspected under the Keyence optical microscope to validate the success of the lift off process. As seen in Figures. 4.6 and 4.7, the patterns are still visible using the optical microscope but making out particular details of the electrode bar (as opposed to the pad) is a bit more challenging due to how thin it is at fifty nanometers thickness as seen in Figure 4.7.

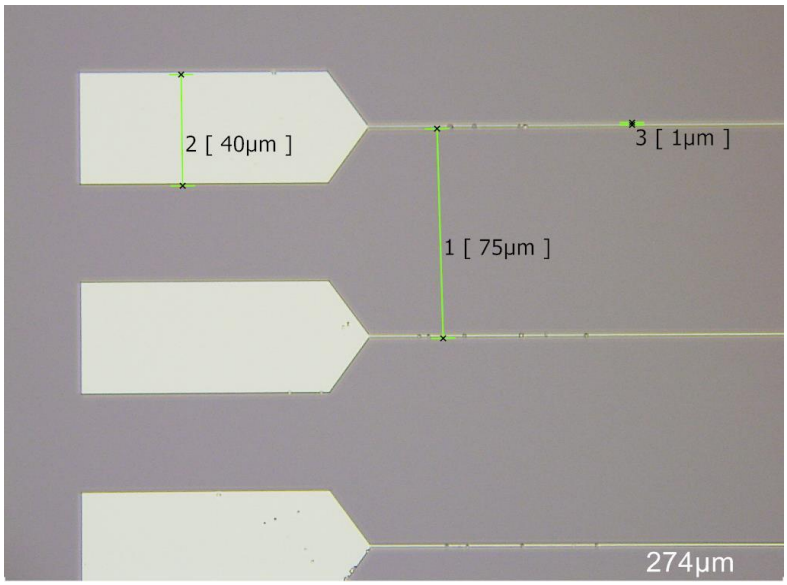

Figure 4.7: Electron beam lithography sample, post lift off with measurements.

The samples were then loaded into the Picosun Sunale R150 Atomic Layer Deposition Reactor, the samples were then treated with the chemical precursors trimethylaluminum and water at 250 °C to form the aluminum oxide film via stoichiometric process. After the alumina forms to a thickness of five nanometers, the hafnium dioxide layer is then formed using Tetrakis (dimethylamido) hafnium (IV) and hafnium oxide at 250 °C. When the HfOx film reached a thickness of ten nanometers, the process was completed and the samples removed.

The samples were then coated again with PMMA 495 A4 and PMMA 950 A4 as outlined for the bottom electrode and again loaded into the JEOL system. The beam condition calibration remained unchanged, but aligning the beam to correctly write the top electrode pattern orthogonally with respect to the bottom pattern requires a few additional steps in order to do a direct write.

First, the global alignment marks must be found using the scanning electron microscope function on the JEOL system. Once located, the offset must be calculated and input into the job deck file that controls the electron beam write process and then compiled. After the global marks are found, the smaller chip alignment marks must also be located and then used to calibrate a drift program that adjusts for any misalignment of the sample relative to the stage. Once these

steps were completed on a sample, the top electrode pattern is written. Owing to some difficulties in calibrating the drift function on the first attempted run, this step was omitted on the write. This did lead to some visible drift in the pattern and it was imperfectly aligned relative to the bottom electrode as seen in Figure 4.8.

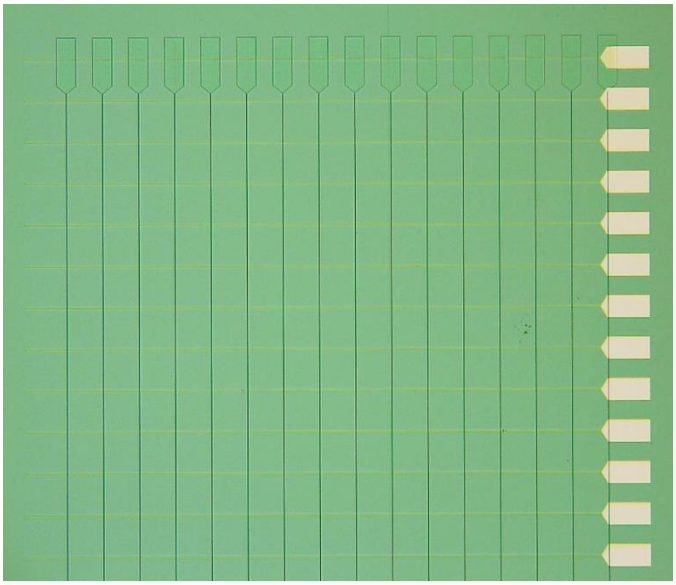

Figure 4.8: Electron beam lithography memristor sample, post top electrode pattern lithography development.

However, the alignment was still adequate for a first time EBL run to validate the fabrication process. Once the alignment and exposure were completed, they were again placed in MIKB:IPA 1:3 developer for seventy five seconds, rinsed with isopropyl alcohol and dried with the nitrogen gas gun. The samples were again inspected and this is where it became visibly obvious that the alignment was not ideal, but was deemed acceptable for the time being.

The samples were then loaded into the Anatech Inductively Coupled Plasma system and run through a one hundred watt, thirty second descum cycle. Afterwards, the samples were loaded into the Temescal FC-2000 Metal Evaporation system and coated with forty nanometers of titanium and two hundred nanometers of platinum. After the process was completed, the samples were placed in Remover PG for ten hours to dissolve the electroresist layer. The samples were then rinsed with acetone and isopropyl alcohol to remove any loose metal film and dried with a nitrogen gas gun.

The samples were inspected under the Keyence optical microscope to validate the success of the lift off process as seen in Figures 4.9 and 4.10. The completed samples were then stored in a nitrogen dry box until the probe station was available for use conducting electrical characterization studies.

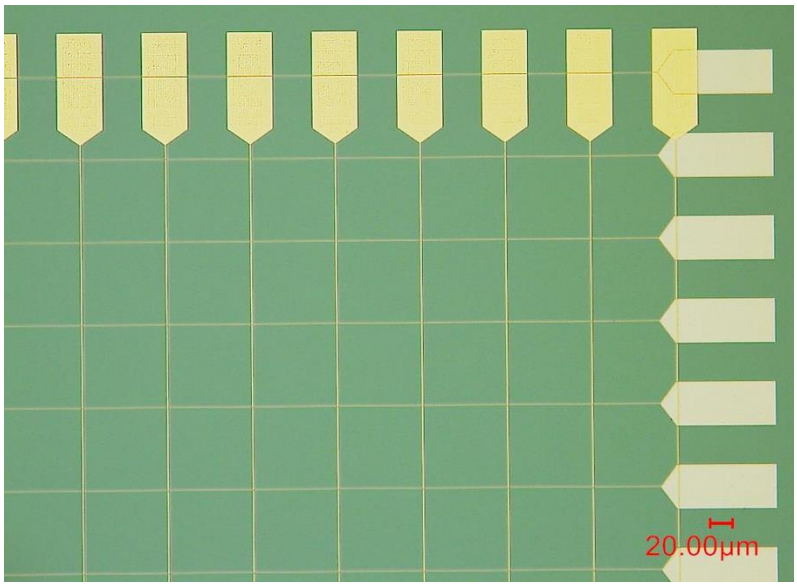

Figure 4.9: Electron beam lithography sample, post final metal lift off.

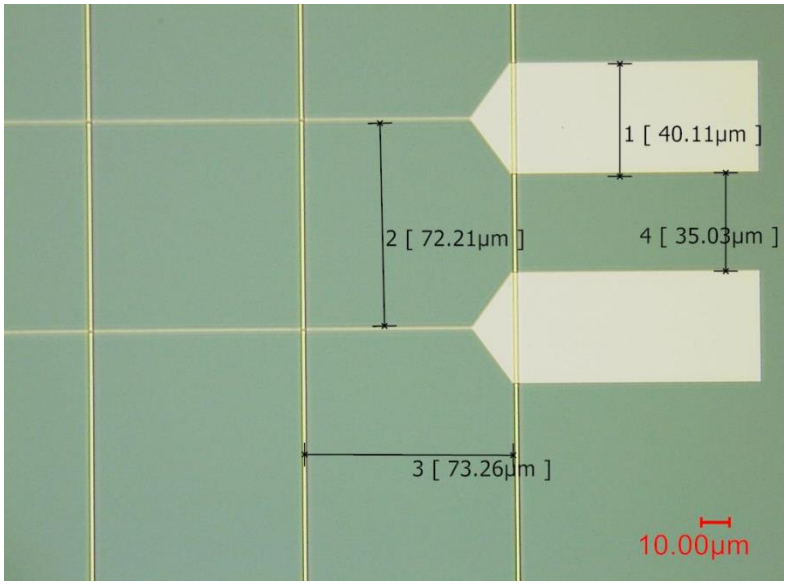

Figure 4.10: Electron beam lithography memristor, post final lift with measurements.

4.1.3 Electrical Characterization of Memristors

For electrical characterization, a B15000A Agilent Semiconductor Parameter system was utilized with a vacuum plate to hold the samples in place and whisker probes were attached to the system via coaxial cables. The samples were aligned on the vacuum plate, probe tips were then aligned and lowered to make electrical contact with the electrodes. Probing began with the innermost corner array of devices and worked across the first line.

The process was then repeated with additional devices in an iterative fashion. The compliance current was set low to avoid possible dielectric breakdown of the devices, from one to ten microamperes. The steps to characterize the RRAM are as follows:

- **Form Step**

  Voltage incremented in 0.25 to 0.5 steps until device forms, low resistance demonstrated by hitting compliance current at a steady state. If the device fails to hit

compliance even when voltage is increased up to ten volts, it likely is an open circuit and unable to form.

- **Reset Step**
  Voltage bias reversed and decremented in -0.5 steps until high resistance state appears and remains stable. Compliance current is disabled for this step, as the current will be throttled when the device goes to a high resistance state. However, there is some risk of dielectric breakdown if the device state fails to change.
- **Cycle Step**
  The On/Off voltage and compliance current set to values the device switched at and then the device is run in both directions to verify stable functionality. The devices will sometimes fail, however.

The optical lithography samples were tested iteratively until a device was found that would cycle reliably with no failure. Earlier tested devices shorted either during the formation step, did not reset or shorted when cycling was attempted.

As seen in Figure 4.11, a successful formation step entails the device hitting compliance current. Having compliance current low enough to ensure formation, but not so high that an irreversible dielectric breakdown occurs and ruins the device is of particularly crucial importance. Sometimes even when the compliance current is set to the microampere range, formation will fail and irreversible dielectric breakdown will occur as seen in Figure 4.12.

Figure 4.13 shows what a successful reset looks like, however it is important to note that current is not regulated on this step. Rather, the engineer operating the parameter analyzer has to rely on the intrinsic material physics and wait for the current to become throttled when the device switched to a high resistance state. This is not without its' risks however and shorting can occur during the reset as seen in Figure 4.14.

The first cycling attempt as seen in Figure 4.15 was extremely noisy for reasons unknown; however, by the second cycle as seen in Figure 4.16, the noise was gone and the hysteresis cycle was ideal as both lobes were well defined with clear state changes visible on the plot.

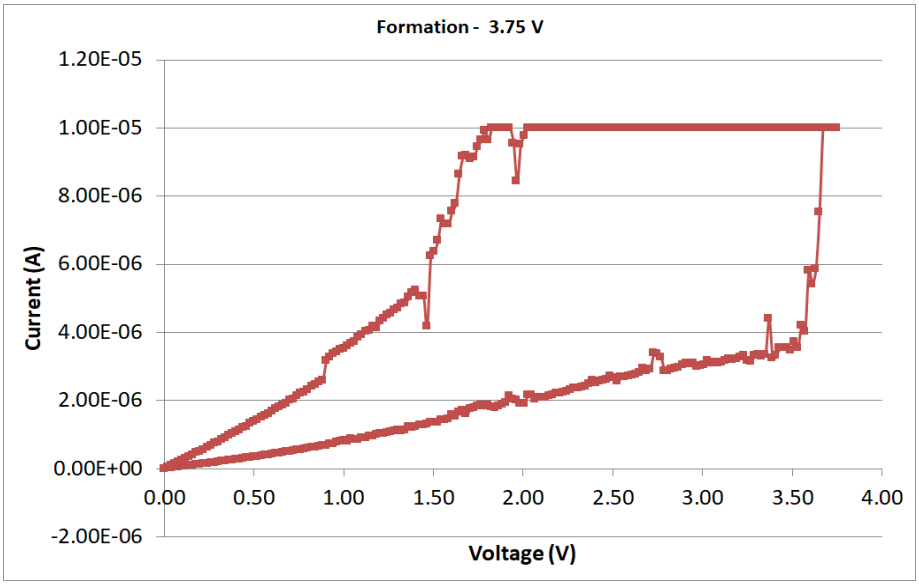

Figure 4.11: Optical lithography sample characterization, form step.

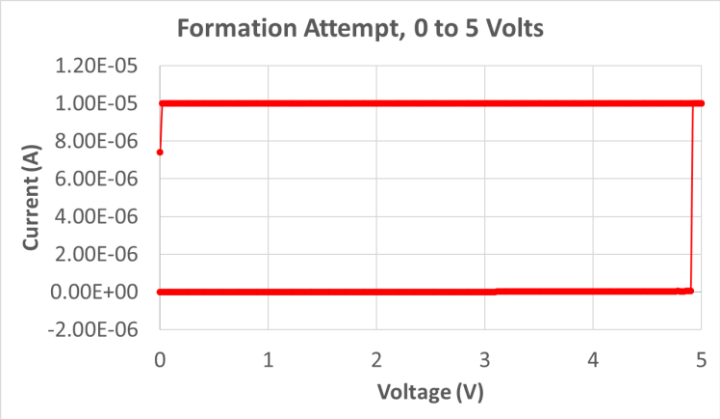

Figure 4.12: Formation failure, device shorts in the ON state.

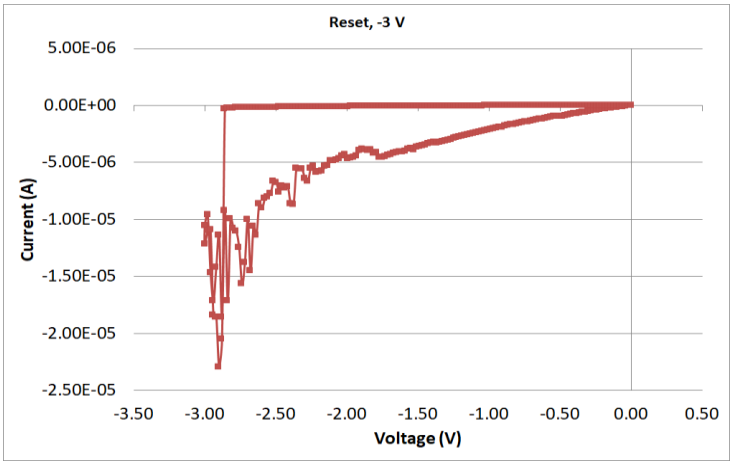

Figure 4.13: Optical lithography sample characterization, reset step.

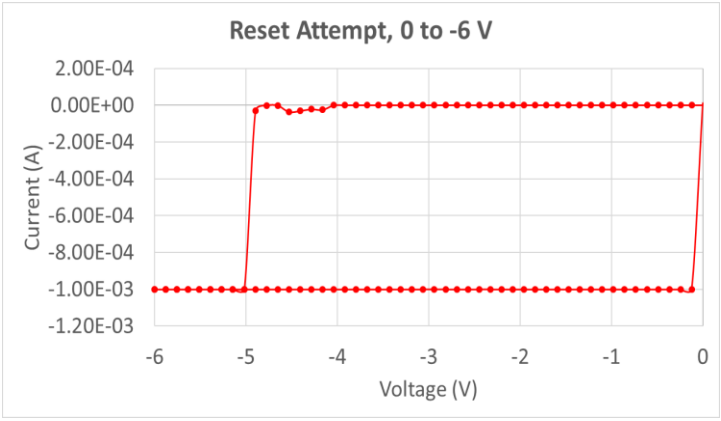

Figure 4.14: Reset failure, device shorts in the ON state.

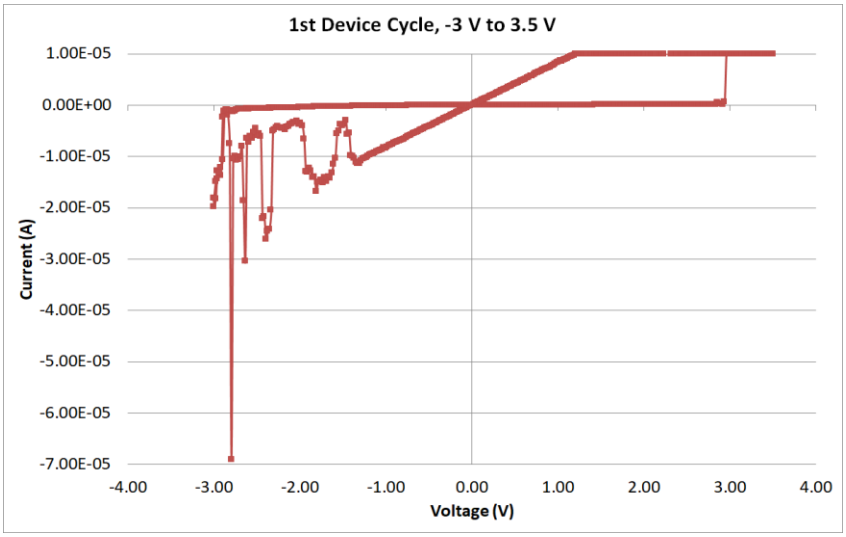

Figure 4.15: Optical lithography sample characterization, first cycle.

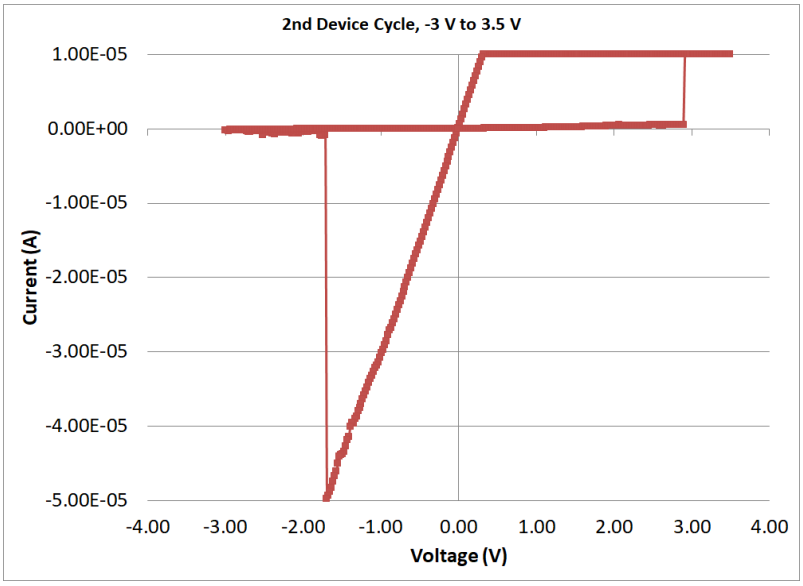

Figure 4.16: Optical lithography sample characterization, second cycle.

4.1.4: Troubleshooting and Technical Problems:

Major problems that occurred in the course of developing a working prototype:

1) Adhesion problems with the metal. The first run failed on the metal evap deposition for the top electrode, this was either due to the metal layer being too thin or organic contamination under the photoresist. This can be seen in Figures 4.17, 4.18 and 4.19 where the metal lift off failed on the optical lithography samples.

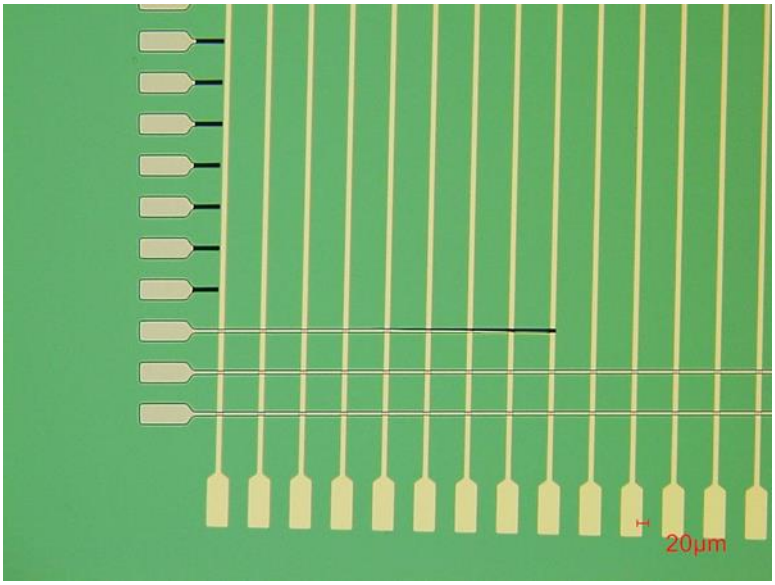

Figure 4.17: Optical lithography sample characterization, top electrode failure.

Solution: An oxygen plasma descum has been incorporated into the cleaning step, the post dehydration bake and the metal thickness of the top electrode has been doubled to that of the bottom electrode for a 2:1 aspect ratio. There have also been problems with adhesion of the bottom electrode with optical lithography however, possibly due to problems with the resolution of optical lithography breaking down in the five to one micron range.

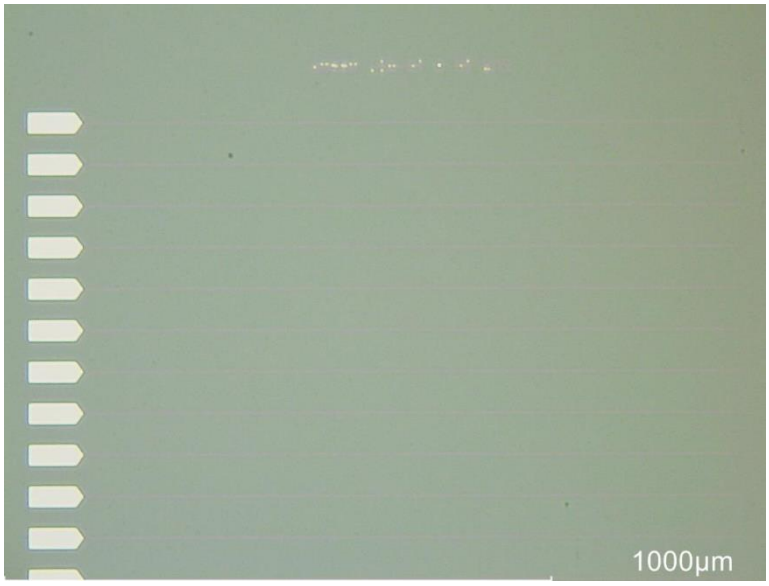

Figure 4.18: Optical lithography sample characterization, bottom electrode failure.

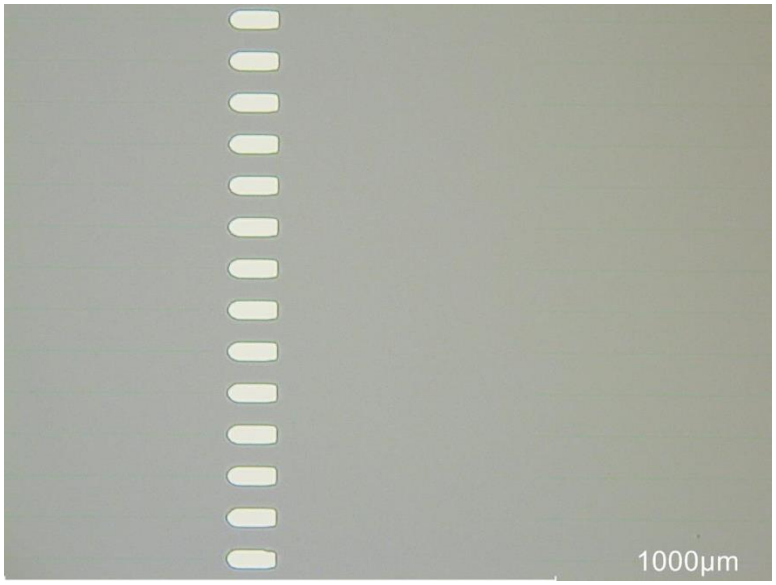

Figure 4.19: Optical lithography sample, bottom electrode lift off failure. Peeling can be seen about the edges, indicating poor adhesion of the metal due to resolution issues.

Since the electron beam lithography samples had no adhesion problems with the exact same deposition thickness further investigation revealed flaws in the lithography process that were then resolved in later generations.

Devices not forming even when voltage increased to the five to ten volt range as seen in Figure 4.20. This may be a problem with the oxide layer being too thick at fifteen nanometers and thus acting as a strong dielectric barrier. An example of this can be seen in Figure 4.20 where the current clearly never exceeds the pico-ampere range and a filament pathway does not form.

Solution: Per Molina, et al., they were able to fabricate function RRAM with the oxide layer as thin as four nanometers [Molina 2016]; the ALD recipe was altered to two nanometers alumina, five nanometers hafnium oxide to reduce the probability of an open circuit. The results of the changes were then documented to observe if this led to a higher rate of successful device development.

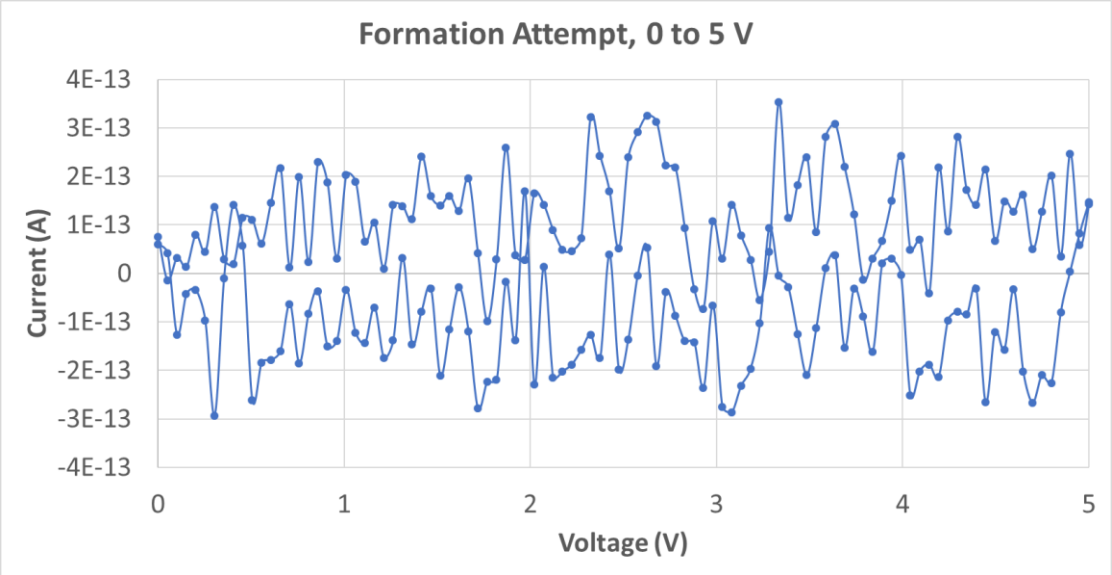

Figure 4.20: Failed formation attempt, memristor registers as an open circuit.

4.2 Revised AutoCAD File and Fabrication using Maskless Alignment System

4.2.1 – AutoCAD Mask Redesign for Optical Fabrication:

Previously, the mask used for fabrication was a simple crossbar design as seen in Figure 4.21.

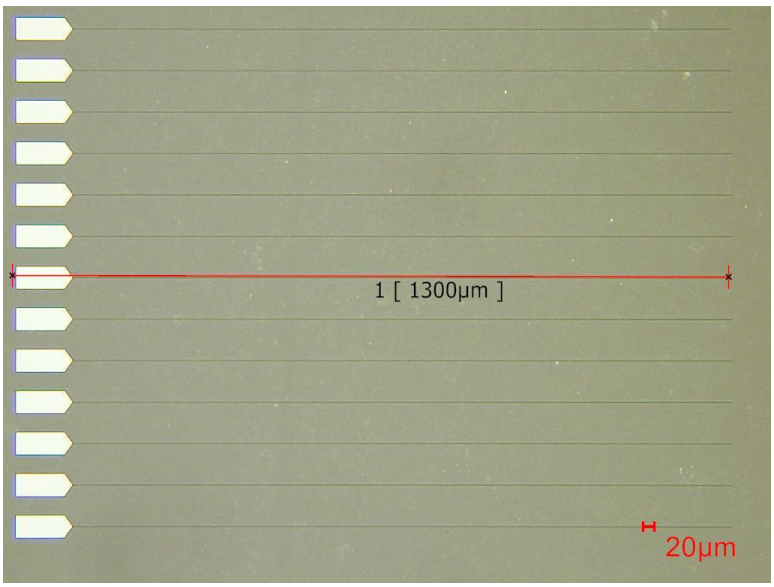

Figure 4.21: Optical lithography crossbar mask.

As seen on the left side, the contact pads were positioned on one end while the crossbars maintained the same width across the length of the array. However, this does pose several drawbacks:

1) The integrity of the metal is lower on average because a thin line of metal is prone to breakage from lateral motion or vibration.
2) If a single line breaks earlier in the liftoff process this then reduces the number of usable memristors.
3) Thin lines of metal are not wholly reliable in bonding to the silicon substrate which can lead to failure modes occurring in the liftoff process.

With the addition of the Heidelberg maskless alignment system to CINT's tool list a shift was made to using purpose-built AutoCAD mask files for several reasons when considering the hard mask:

1) The integrity of the metal is lower on average because a thin line of metal is prone to breakage from lateral motion or vibration.
2) If a single line breaks earlier in the liftoff process this then reduces the number of usable memristors.
3) Thin lines of metal are not wholly reliable in bonding to the silicon substrate which can lead to failure modes occurring in the liftoff process.

Considering the above problems and the availability of the Heidelberg 150 Maskless Aligner system, this enabled the opportunity to redesign the mask using AutoCAD in order to overcome the outlined issues, as well as move towards larger quantities of memristors being fabricated on a per-sample basis. Discussion of the mask changes follows starting with Figure 4.22.

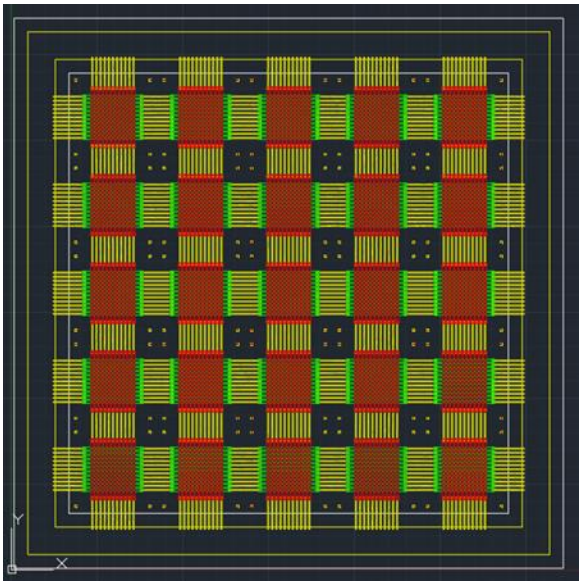

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Figure 4.22: AutoCAD mask file, all layers.

The new mask is a five by five array of memristors with eleven by eleven possible devices per neuron for a total of 3025 memristors per sample which is a substantial increase over the older physical mask design that was being used. In addition, there are significant changes to the crossbars which can be seen in Figures 4.23 and 4.24 when an individual eleven by eleven array is inspected more closely.

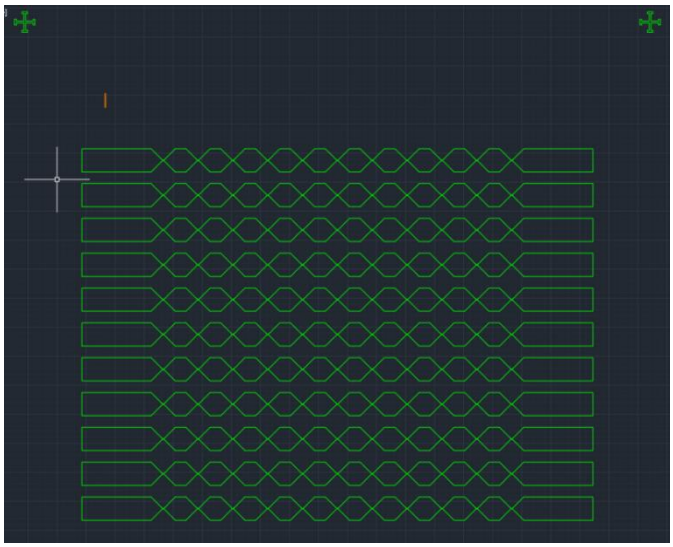

Figure 4.23: Array of single neuron, bottom contact.

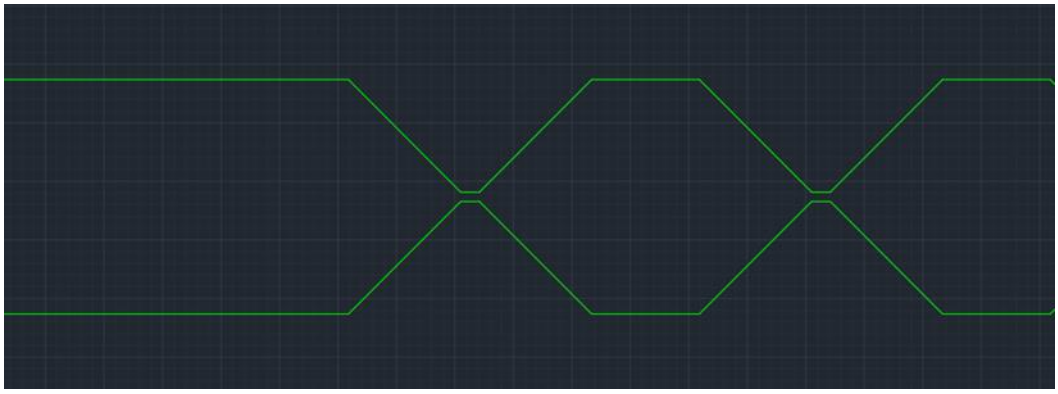

Figure 4.24: Bottom contact, crossbar and bowtie.

As can be seen, the array is no longer a simple line, but a crossbar pattern. This will make for a more structurally sound metal layer as the width broadens out where the devices will not be formed. This allows for greater surface area where the metal is deposited, ensuring more uniformly consistent adhesion of the Ti/Au metal, post-deposition during liftoff.

After the first metal deposition, the oxide layer is deposited conformally using atomic layer deposition. Then a positive photolithography pattern is placed with the oxide exposed on the electrical contacts for an etch using buffered hydrofluoric acid to remove the oxide from the electrical pads to ensure a reliable conduction pathway can be made for characterization of the devices as can be seen in Figure 4.25.

Once the excess oxide is removed, photolithography is then conducted for the final metal deposition step and the top electrode pattern is placed orthogonally to the bottom contact as seen in Figure 4.26.

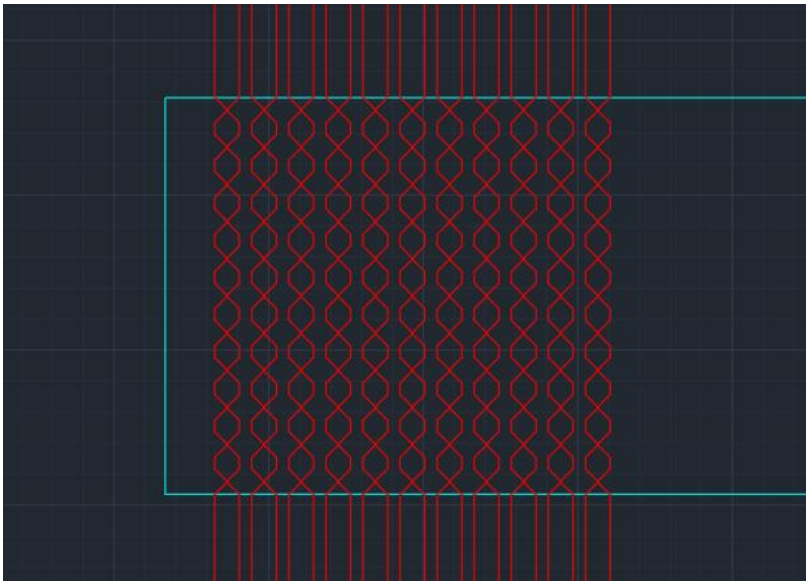

Figure 4.25: Oxide protection photoresist mask.

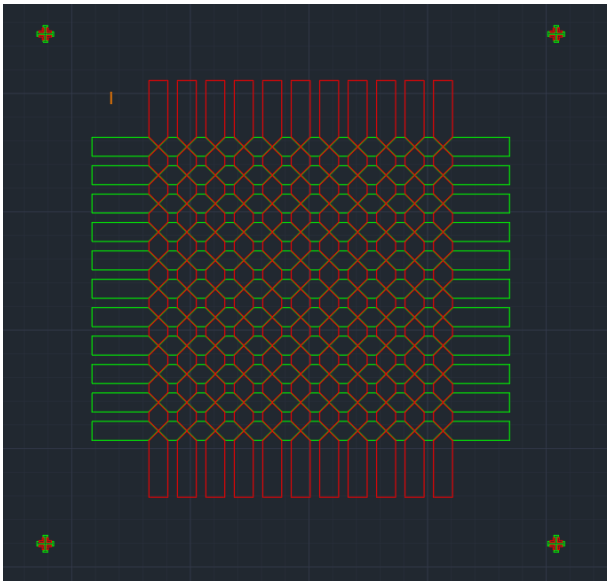

Figure 4.26: Top and bottom contact patterns.

Post final metal liftoff, the sample is then coated with a thick photoresist and lithography is conducted in preparation for electoplating, as shown in Figures 4.27 and 4.28.

Then, the entire sample is placed in a gold electroplating bath, with the top and bottom contacts connected to the electroplating terminals. A voltage is then run across the contacts to attract the gold ions to the metal surfaces, thickening the total surface of the metal contacts to a thickness suitable for the wirebonding procedure. Once electroplated, the samples are then diced out for wirebonding and then being packaged.

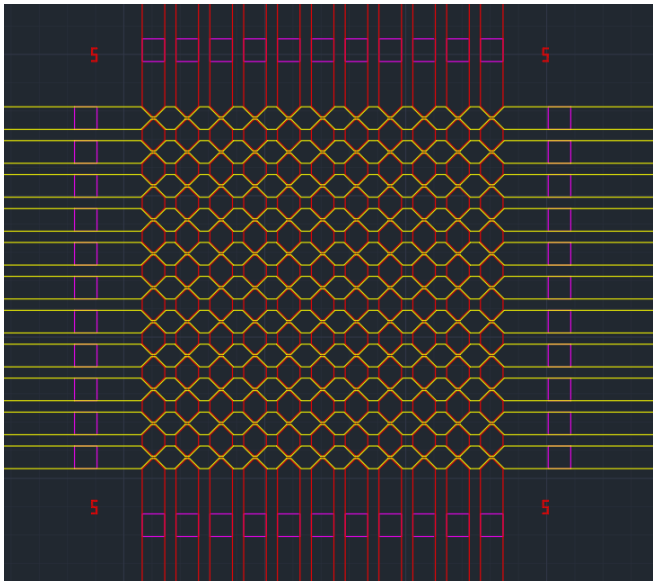

Figure 4.27: Electroplated squares on traces.

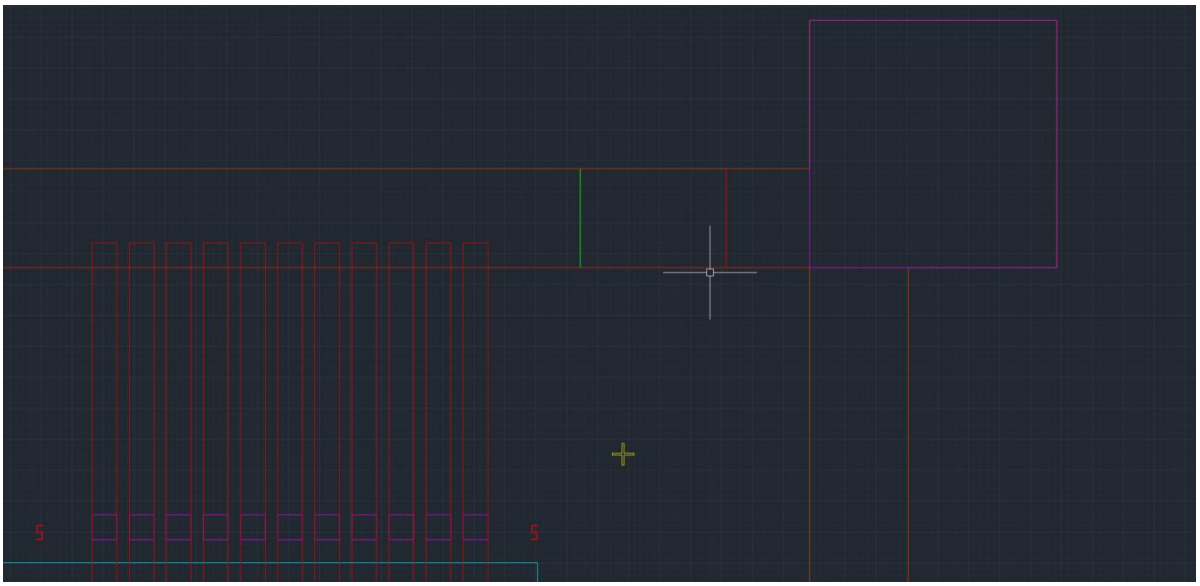

Figure 4.28: Electroplating pad and ring, overlaps with traces to ensure the gold grows across all metal surfaces.

4.2.2 The MLA150 Maskless Aligner:

The MLA 150 system offers unprecedented flexibility in the lithography process as rather than the exposure simply being a UV source that floods a target which in turn is pattered via a traditional mask, the system uses a 2-dimensional spatial light modulator to specifically write the pattern onto the sample, much like the JEOL Electron Beam Lithography system as can be seen in Figure 4.29.

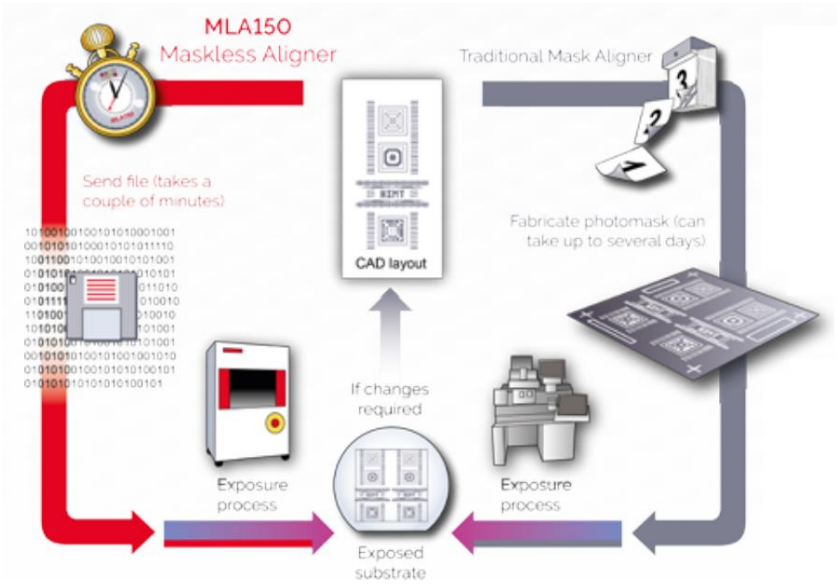

Figure 4.29: MLA150 Maskless System vs Traditional Lithography
Source: Heidelberg Fact Sheet [Heidelberg 2016].

This enormously expedites the process of changing the mask for the RRAM as rather than having to submit a request to CINT for the fabrication of a hard mask template, the changes can be made to the initial AutoCAD file and then directly exported to the tool and implemented immediately, allowing me to fabricate a prototype RRAM generation, observe what changes need to be made to the AutoCAD file and then reconfigure the mask file as needed. Training was finished rapidly on this system and the new RRAM mask was then imported into the system. However, this quickly revealed there are some subtle but crucial differences between AutoCAD *.dwg files and the file format accepted by the tool, *.dxf files. While the AutoCAD file appeared sound and in working order, the initial import failed with the program on the MLA150 hanging in execution for upwards of 15 minutes. Investigation revealed that the program would error out if layer names were longer than 16 characters and the layer named “Memristor Oxide Protection Layer” exceeded this character length. The layer name was then truncated to “Oxide Layer” which resolved this issue. Visual inspection of the mask in the file import viewer revealed the images were not converting correctly and were blank.

Further investigation and consultation with the postdoc revealed that per a guide written for this topic “Design Rules for Drawing Masks Using AutoCAD” [Artwork 2020], this problem would occur when the polygons were not fully closed and the metadata was not scrubbed from the AutoCAD file before saving it in *.dxf format. Further research yielded the discovery of a free program that could be utilized to inspect mask files before attempting to import them at CINT, KLayout.

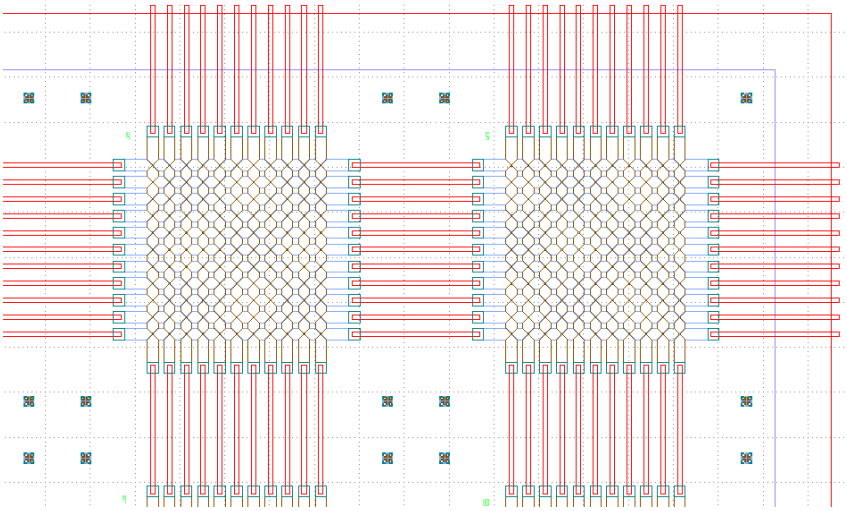

Figure 4.30: Broken mask file in Klayout.

KLayout was then installed and used to inspect the mask file, revealing that none of the polygons in the mask file were closed, as can be seen in Figure 4.30 where none of the shapes have diagonal hatching which would then indicate that the file was sound. The mask was then rigorously debugged until the polygons were clearly closed as shown in Figure 4.31.

After further discussion with the tool owner, the mask was also altered to eliminate the excess alignment marks between RRAM arrays with 4 major alignment marks placed at the outer corners of the overall arrays as the MLA system aligns more efficiently with simpler markings than it did with the more elaborate system that was placed initially. The mask was further modified at this time to increase the diagonal gap spacing as shown in Figures 4.32 and 4.33, due to concerns that the initial gap of 2.5 um was too small and there would be overlap between the top and bottom traces, leading to shorts. The corrected mask file was then taken to CINT and successfully imported, enabling the resumption of RRAM fabrication with the new mask design being deployed in future generations of fabricated devices.

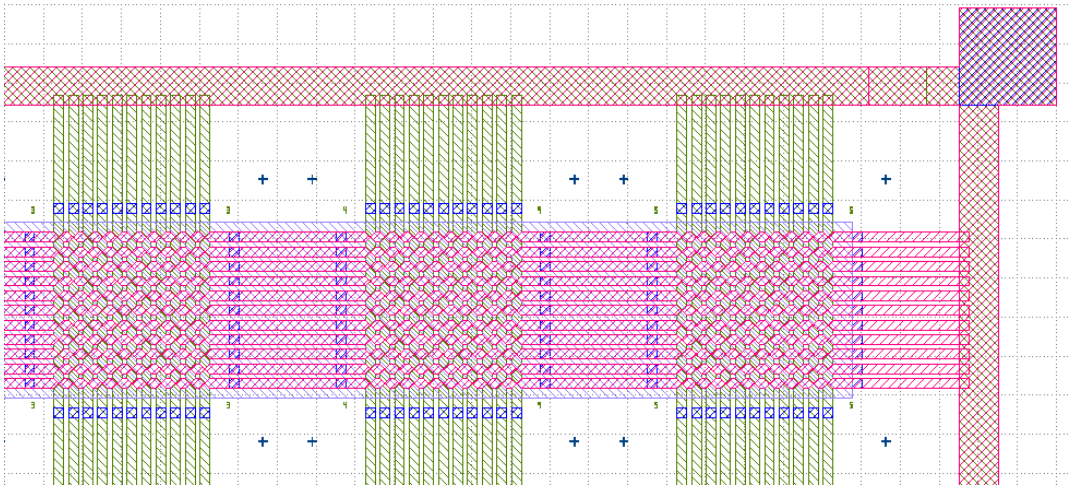

Figure 4.31: Corrected mask file in KLayout.

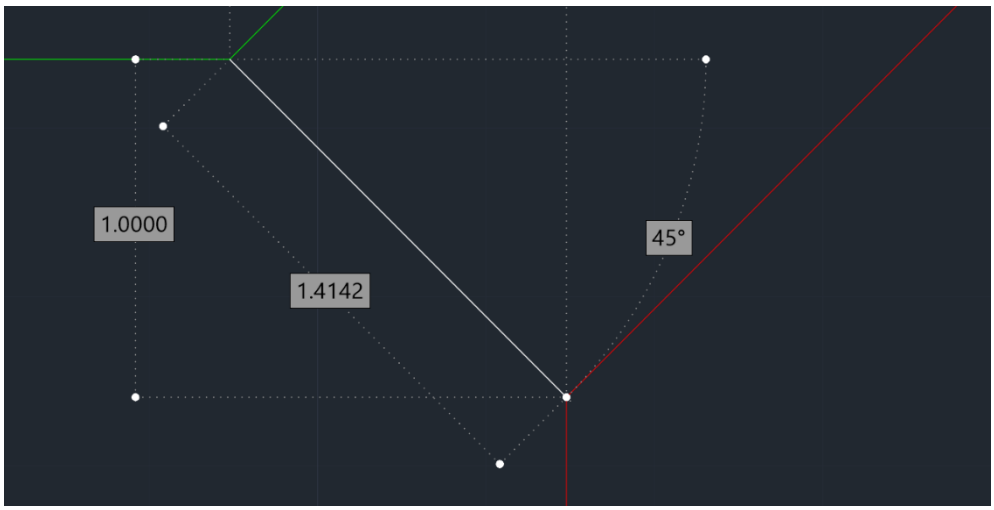

Figure 4.32: Initial gap on the diagonal measured 1.4 um, too close to MLA design tolerance of 1 um.

Figure 4.33: Revised gap on the diagonal is now 2.8 um, more in line with the design tolerance of the MLA system.

4.2.3 - Electron Beam Fabrication, Discontinued:

Due to the JEOL Electron Beam Lithography system being down extensively for overhaul and maintenance for months at a time and lead time for fabricating sub-micron memristors on the EBL being a minimum of two weeks or more, the decision was made to prioritize memristor fabrication on the MLA system as total production time using the MLA lithography system was a week at most. Moreover, there was no compelling reason per literature or prior data collected to continue on with nanoscale memristor production at this time as it was more efficient to refine the fabrication process using optical lithography.

4.3 Second Generation Memristors

With CINT re-opened from the multi-month shutdown due to the COVID-19 pandemic, fabrication work resumed on the hafnia memristors using the MLA Maskless Lithography system. It was initially assumed that NLOF 2035 would continue to be utilized for the lithography process, however after consulting with CINT scientists, it was determined that AZ5214E photoresist would be simultaneously more flexible for both the positive and negative lithography needed, as well as not requiring dose testing or calibration for use in the fabrication process.

Therefore the samples were first spin coated with HMDS, soft baked at 90 °C for one minute, then spin coated at 5000 rpm for thirty seconds with AZ 5214E resist and soft baked at 110 °C for one minute. The samples were then loaded into the MLA150 Maskless Aligner and exposed at 120 nJ with the wavelength set to 405 nm. The samples were then developed using MIF 300 developer with an exposure of 45 seconds, rinsed with DI water and inspected optically. As can be seen in Figure 4.34, the resolution of the MLA150 system is outstanding, with good features down to the 1 micron thickness for the crossbar pattern.

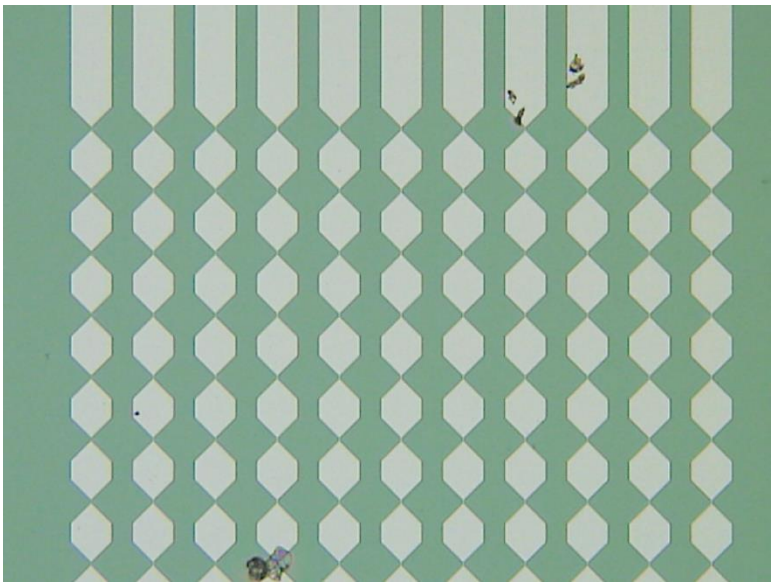

Figure 4.33: Optical lithography crossbar mask, 1 um pattern.

The samples were then loaded into the Anatech Inductively Coupled Plasma system and run through a one hundred watt descum cycle for three minutes. This ensures no organic contamination of the surface to promote good adhesion of the metal to the substrate.

The samples were then loaded into the Temescal FC-2000 Metal Evaporation system and coated with twenty five nanometers titanium and one hundred nanometers gold. Previously, thicker metal layers were used due to uncertainty about the adhesion with thin crossbar patter, but this was determined to be less of a concern with the modified bowtie pattern.

After the process was completed, the samples were placed in Remover PG for twelve hours to dissolve the photoresist layer. The samples were then placed in an ultrasonic bath to

break down the excess material as it was found empirically that using an acetone nitrogen spray gun would not remove the metal completely on by itself. The samples were then rinsed with acetone nitrogen spray gun, then rinsed methanol and isopropyl alcohol and dried with the nitrogen gas gun. The samples were then inspected under the Keyence optical microscope to validate the success of the lift off process as seen in Figure 4.34.

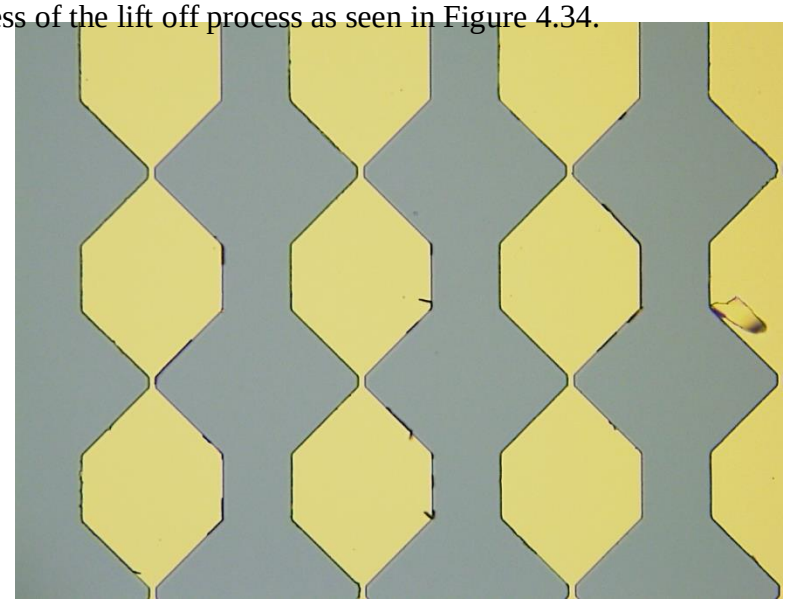

Figure 4.34: Bottom electrode pattern, post liftoff process.

The samples were then loaded into the Picosun Sunale R150 Atomic Layer Deposition Reactor, the samples were then treated with the chemical precursors trimethylaluminum and water at 250 °C to form the aluminum oxide film via stoichiometric process. After the alumina formed to a thickness of approximately five nanometers, the hafnium dioxide layer is then formed using tetrakis(dimethylamido)hafnium(IV) and hafnium oxide at 250 °C. When the HfOx film reached a thickness of approximately ten nanometers, the process was completed and the samples removed.

The samples were then spin coated with AZ 5214E at 5000 rpm for thirty seconds with a one minute soft bake at 110 °C in preparation for the oxide protection lithography before being soaked in buffered oxide etch (BOE) solution to remove the oxide from the contact pads.

As this step calls for an inversion of the mask image to protect the crossbar patterns coated in hafnia while exposing the remainder of the substrate to the buffered oxide etch (BOE), the samples were exposed in the MLA150 system at 60 nJ at the 405 nm wavelength. A post exposure bake is then conducted on the samples at 120 °C for one minute. The samples are then placed in the mask aligner lithography system with no mask and a flood exposure is conducted for one minute.

The samples are then developed using MIF 300 for 45 seconds and rinsed with DI water. As can be seen in Figure 4.35, the oxide area is protected while the rest of the sample is exposed for the BOE soak. The samples are then hard baked for twenty minutes at 130 °C on a hot plate.

As the oxide film is an ultrathin film of approximately 15 nm, the samples are soaked in BOE for one minute at the acid wet bench and no longer to ensure there is no breakdown of the

hafnia given how reactive BOE is. The samples are then rinsed with DI water and placed in a Remover PG solution to soak for a minimum of twelve hours to ensure the hard baked resist is fully removed before the top electrode pattern is written.

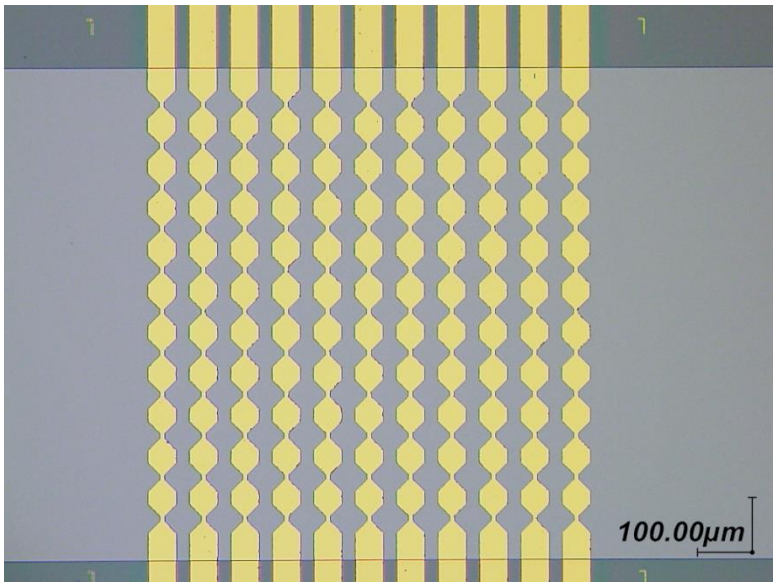

Figure 4.35: Oxide protection lithography, photoresist over bowties and rest of the substrate exposed.

The samples are then cleaned with acetone, methanol and isopropyl alcohol to ensure the surface is clean. The samples are then placed on a hot plate at 180 °C to completely dehydrate the surface in preparation for the top electrode lithography. The samples are then spin coated with HMDS, soft baked at 90 °C for thirty seconds, spin coated with AZ 5214E at 5000 rpm for thirty seconds and soft baked at 110 °C for one minute. The samples were then loaded into the MLA150 Maskless Aligner, manually aligned and exposed at 120 nJ with the wavelength set to 405 nm. The samples were then developed using MIF 300 developer with an exposure of 45 seconds, rinsed with DI water and inspected optically. Figure 4.36 shows that the alignment and exposure were successful, with good resolution and aligned with respect to the bottom electrode pattern.

The samples were then loaded into the Anatech Inductively Coupled Plasma system and run through a one hundred watt descum cycle for three minutes. This ensures no organic contamination of the surface to promote good adhesion of the metal to the substrate.

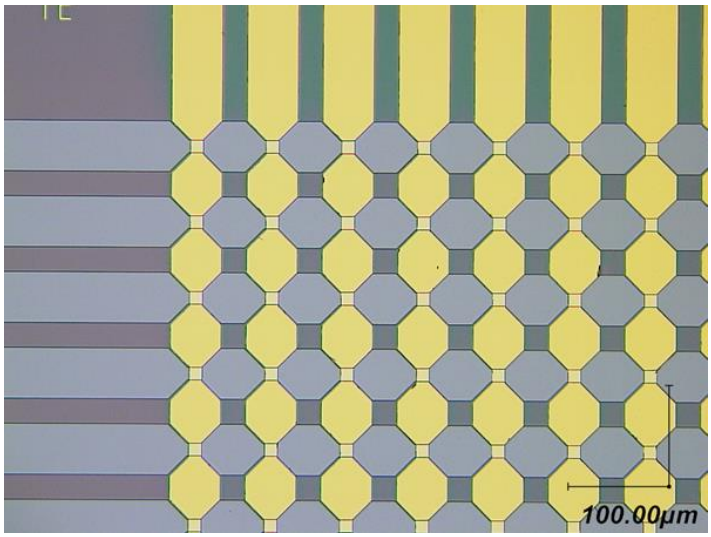

Figure 4.36: Top contact lithography, crossbar and bowtie aligned.

The samples were then loaded into the Temescal FC-2000 Metal Evaporation system and coated with fifty nanometers titanium and two hundred nanometers gold. Previously, thicker metal layers were used due to uncertainty about the adhesion with thin crossbar pattern but this was determined to be less of a concern with the modified bowtie pattern.

After the process was completed, the samples were placed in Remover PG for twelve hours to dissolve the photoresist layer. The samples were then placed in an ultrasonic bath to break down the excess material, the samples were then rinsed with acetone nitrogen spray gun, then rinsed methanol and isopropyl alcohol and dried with the nitrogen gas gun. The samples were then inspected under the Keyence optical microscope to validate the success of the lift off process as seen in Figure 4.37.

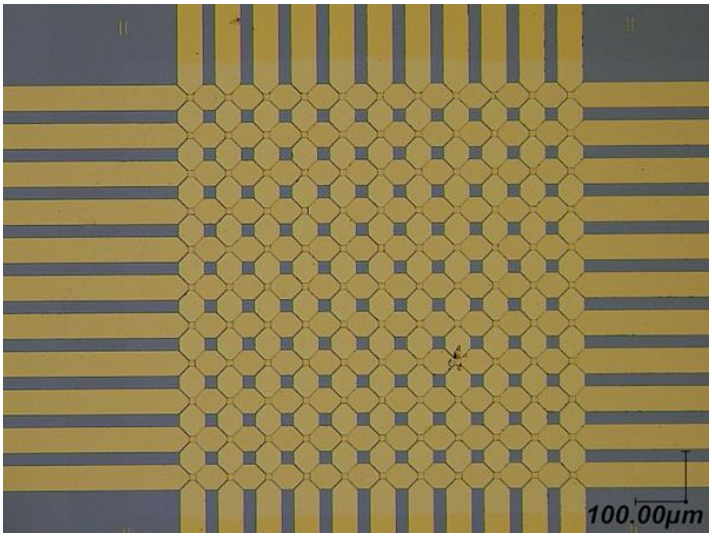

Figure 4.37: Second generation, final liftoff.

Upon inspection with higher magnification, it became clear that there was some overlap on the bowtie diagonals which raised concerns about the viability of the devices as can be seen in Figure 4.38.

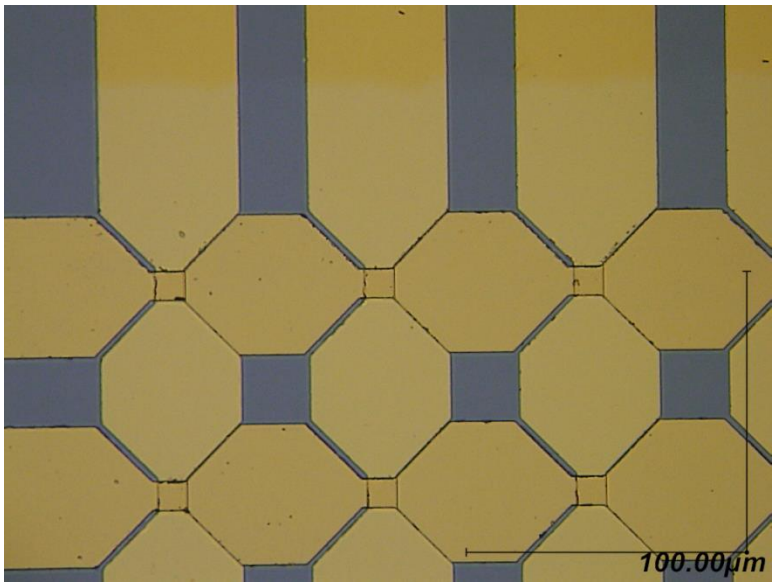

Figure 4.38: Slight overlap on the diagonal on the right side.

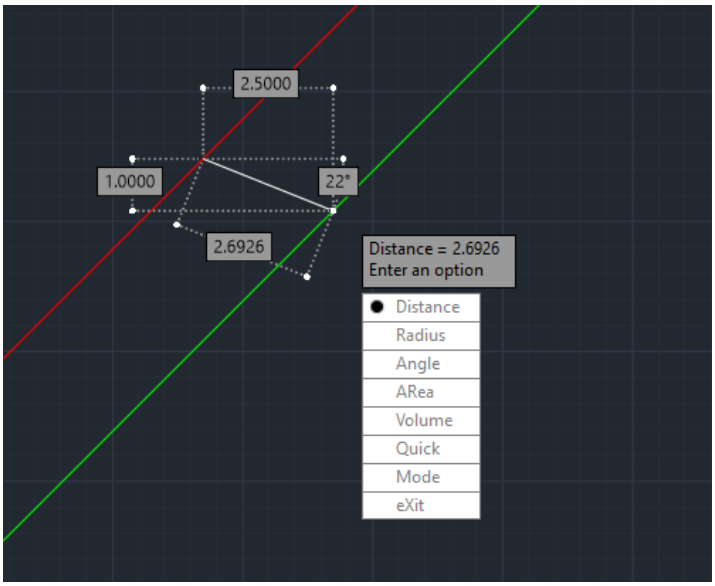

Figure 4.39: Measured diagonal gap in mask file.

When I inspected the distance of the diagonal in the mask design file, I determined that the spacing gap was approximately 2.5 microns which exceeded the alignment error margin on the MLA150, leading to the overlap as can be seen in Figure 4.39. The mask was then edited to increase the diagonal gap to 5 microns to match the tolerances on the MLA150 Aligner and the changes incorporated into the next generation of RRAM.

4.4 Third Generation Memristors

The fabrication process was then repeated as outline for the second generation, the only change being the revisions made to the mask as discussed in the last paragraph. After the liftoff was performed for the top electrode, the samples were then inspected using optical microscopy to verify that there was adequate clearance along the bowtie diagonals. As can be seen in Figure 4.40, even with slight deviation from the margins of error in the MLA150, there is sufficient spacing to ensure proper clearance between the electrodes.

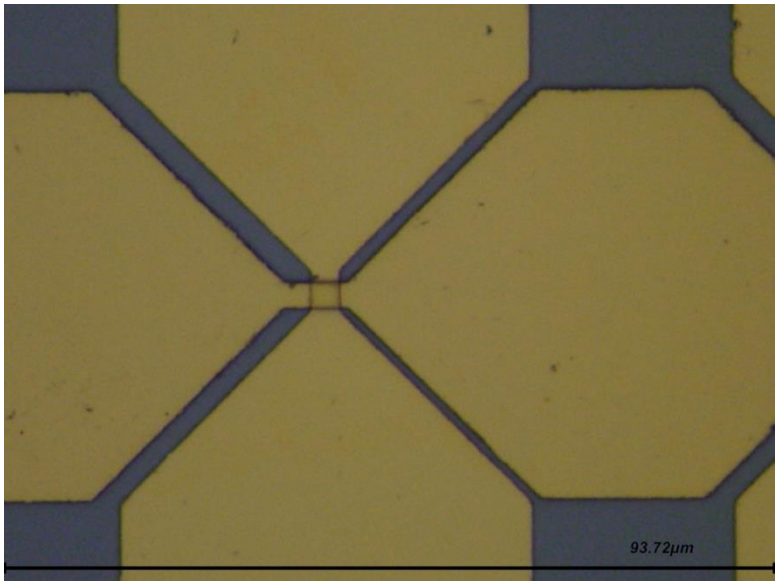

Figure 4.40: Diagonal gap spacing improved, no overlap.

The samples were then prepared for electroplating by spin coating with AZ 9260 at 2000 rpm and soft baked for five minutes. The samples were then loaded into the MLA150 Maskless Aligner, manually aligned and exposed at 120 nJ with the wavelength set to 405 nm. The samples were then developed using MIF 300 developer with an exposure of two minutes, rinsed with DI water and inspected optically. The electroplating sites are clearly defined as seen in Figure 4.40. The samples were then transported to CHTM and placed in the electroplating system there, with a targeted thickness of 10 microns being the desired height for the electroplated sites.

The samples were then spin coated with photoresist to protect the completed devices, diced and the samples placed in Remover PG for twelve hours to remove the photoresist layer. The samples were then cleaned with acetone, methanol and isopropyl alcohol and dried with a nitrogen spray gun and inspected using optical microscopy. As can be seen in Figure 4.42, it was clear the electroplating was successful with the only question being, how thick the electroplated gold on the arrays was. The thickness was then checked using profilometry as can be seen in Figure 4.43.

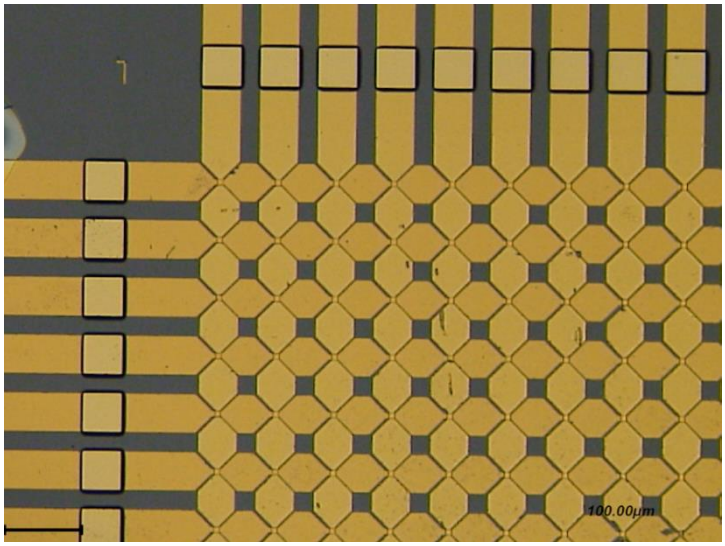

Figure 4.41: Sample with electroplating lithography.

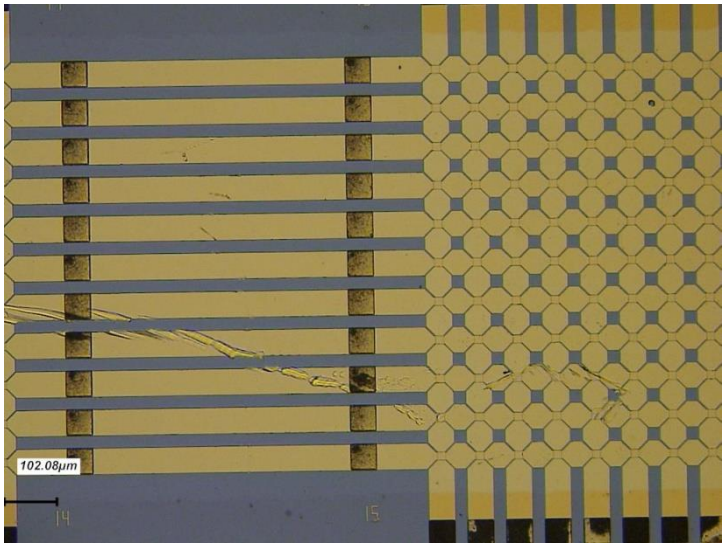

Figure 4.42: Memristor array with electroplating completed.

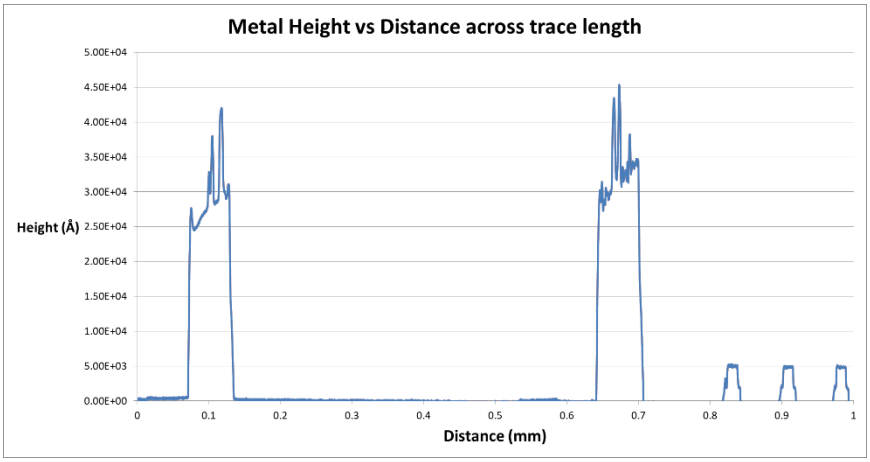

Figure 4.43: Profilometry of RRAM electroplated sites.

As can be seen from the profilometry plot, electroplated sites on the samples reached approximately 3 microns which fell short of the desired height of 10 microns. Analysis of the electroplating setup indicates that the target site for making electrical connection to the samples for the electroplating was too small for good conduction pathways. Furthermore, dicing the samples and attempting to wire bond the RRAM revealed that the traces were too tightly spaced for consistent connections as the width fell below the design tolerances for the wire bonding tool as can be seen in Figure 4.44. I also did manage to make electrical contact with some of the samples and it was quickly determined that the oxide layer was electrically shorted as can be seen in Figures 4.45 and 4.46.

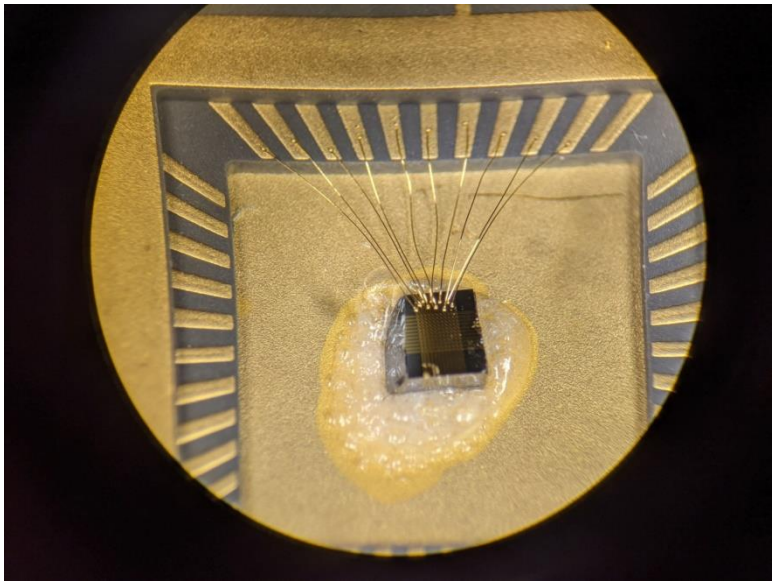

Figure 4.44: Attempted wire bond of memristor array to package.

A wire bond test was then conducted on a sample consisting solely of bare metal traces of identical thickness with no oxide layer to determine if the metal traces would peel or break during the wire bonding process. It was determined that electroplating was an unnecessary step and the geometric limitations of the wire bonding station, as well as the need for quick electrical characterization before packaging necessitated changes made to the mask file to accommodate these needs in the fabrication process. On consultation with the postdoc, the mask was then changed to give the memristor arrays a radially outward series of pads large enough to match the tolerances of the wire bonding station while simultaneously enabling electrical characterization at a probe station prior to dicing and packaging. These changes to the mask were then implemented in the next generation of memristors.

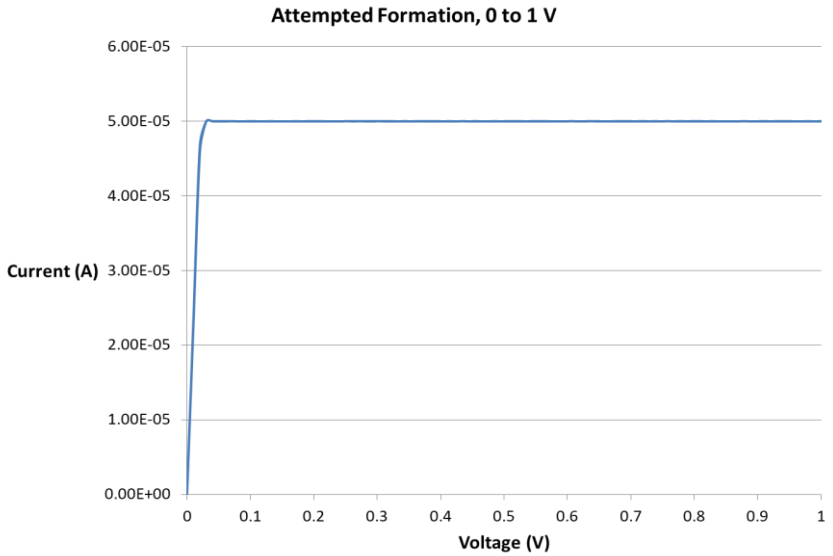

Figure 4.45: Attempted formation, devices hit compliance current at 50 microamps.

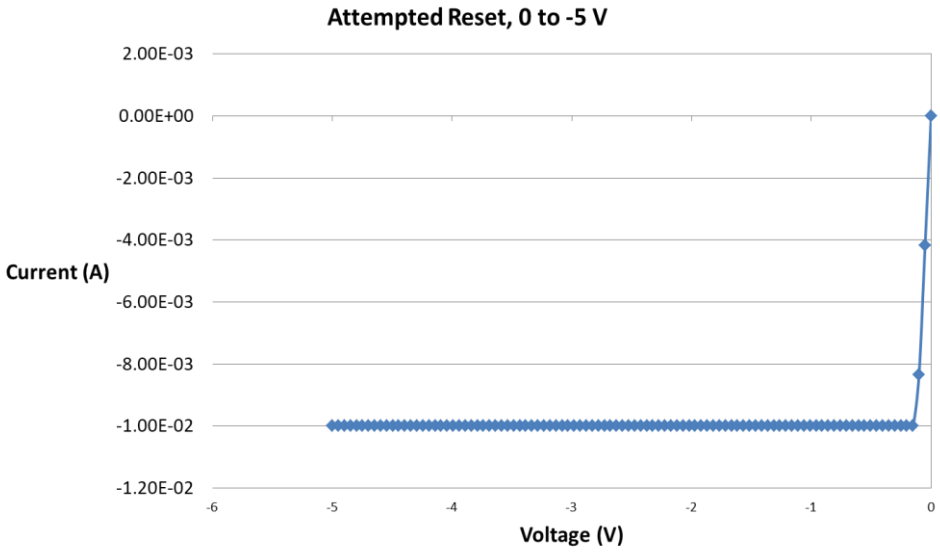

Figure 4.46: Attempted reset, devices did not change state at -5 volts.

4.5 Fourth Generation Memristors

The mask file was redesigned to cover a 2 x 2 cm area per array with contact pads that are 100 x 100 microns in size with 50 micron spacing between pads as shown in Figure 4.47.

The next generation of RRAM was then fabricated following the process previously outline with the mask revision, as four samples were prepared they were then split into two groups at the oxide layer step to evaluate if changing the oxide film thickness would yield results that were not shorted electrically as seen in the second and third generations.

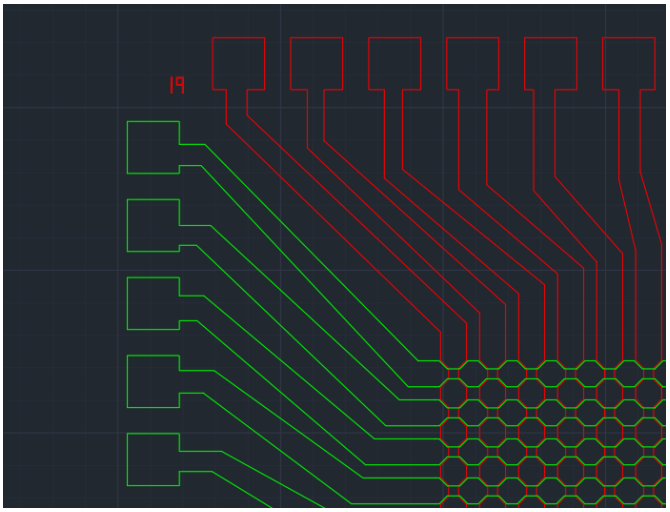

Figure 4.47: Revised memristor mask file with contact pads.

Group A was given a 2/5 nm AlOx/HfOx layer while Group B was given a 2/5/2/5 laminate structure based on a paper by Ding, Zhang, et al. [Ding 2007]. The fabrication was successful with the contact pads well defined as can be seen in Figure 4.48 and 4.49, enabling rapid electrical characterization to gauge the results of the changes made to the oxide layer.

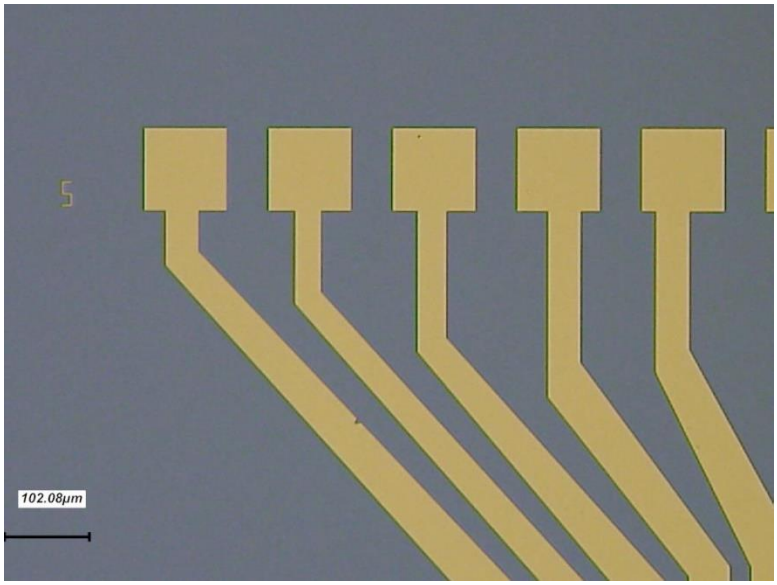

Figure 4.48: Bottom contact pad array, post liftoff.

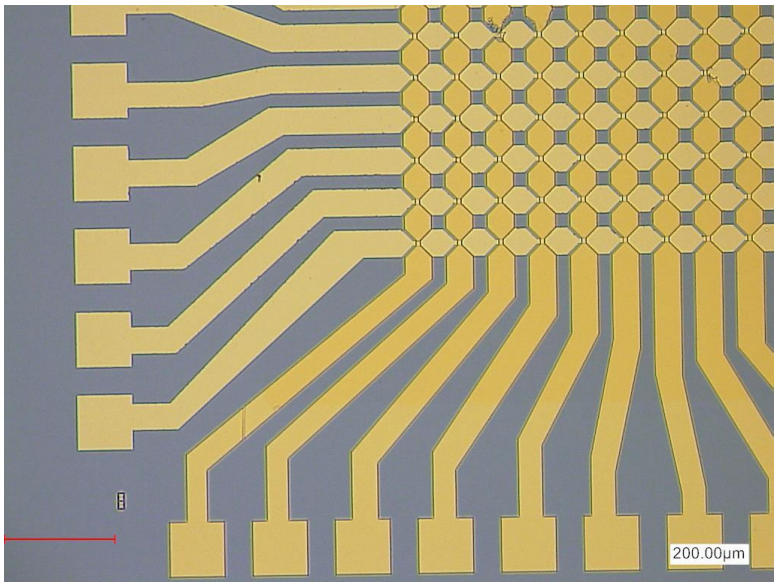

Figure 4.49: Full memristor array, post final liftoff.

The fabricated samples were then characterized using the B1500A Agilent Semiconductor Parameter Analyzer at CINT, with several devices of varying trace thickness checked at random to obtain a statistically significant result that could be extrapolated to estimate the functionality of devices on the samples. As can be seen from Figures 4.50 through 4.53, the 5 nm oxide thickness memristor devices in Group A demonstrated weak electrical switching, but the 10 nm bilayer laminate memristors in Group B did not change states.

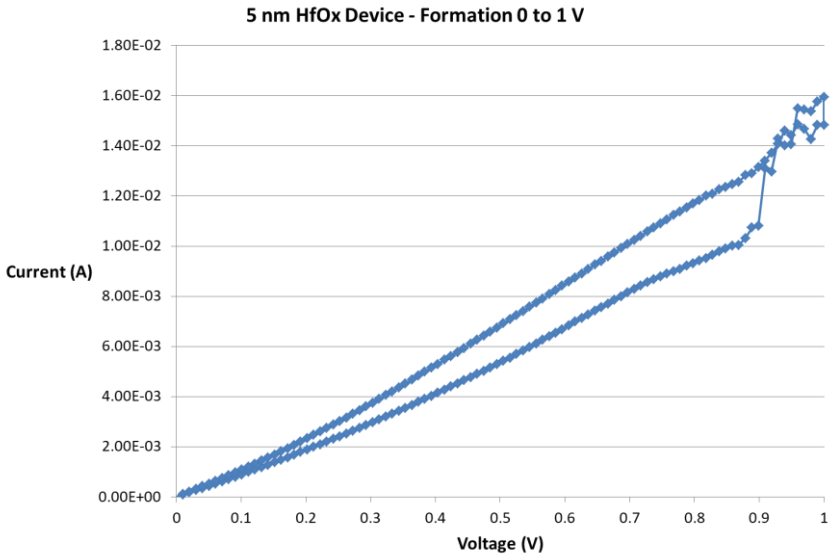

Figure 4.50: Group A memristor formation, 5 nm.

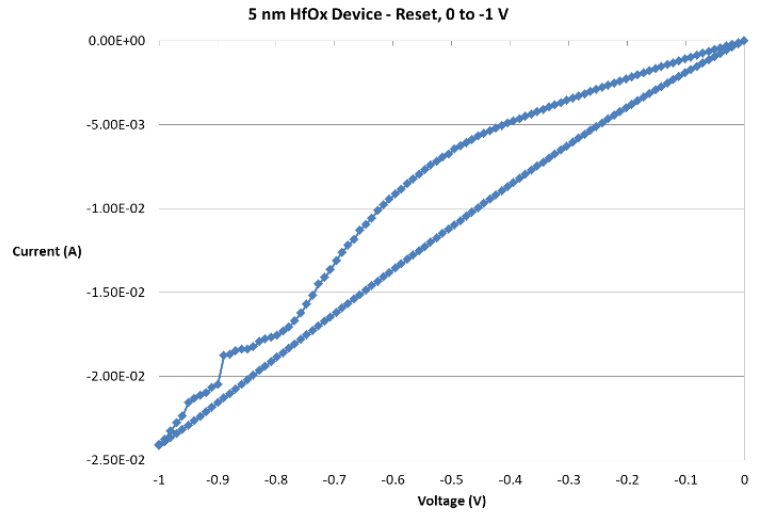

Figure 4.51: Group A reset attempt, 5 nm. Weak reset switching observed.

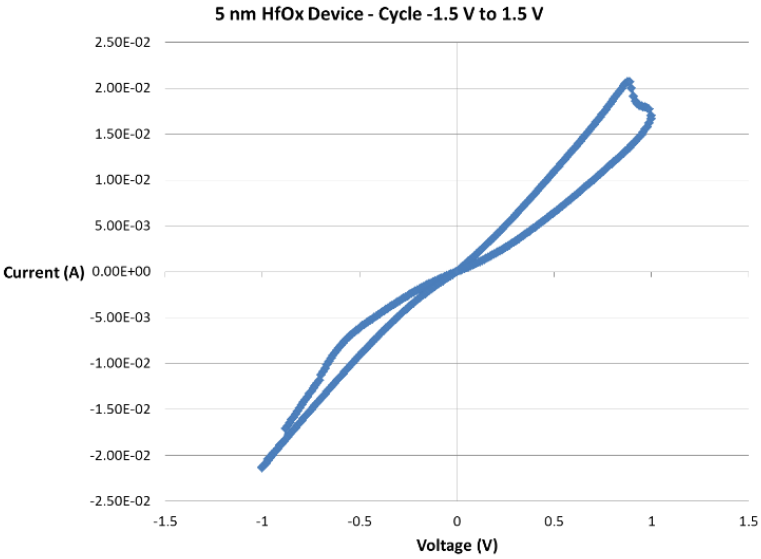

Figure 4.52: Group A full hysteresis cycle, 5 nm. Memristor did change states, but difference is too small for viability.

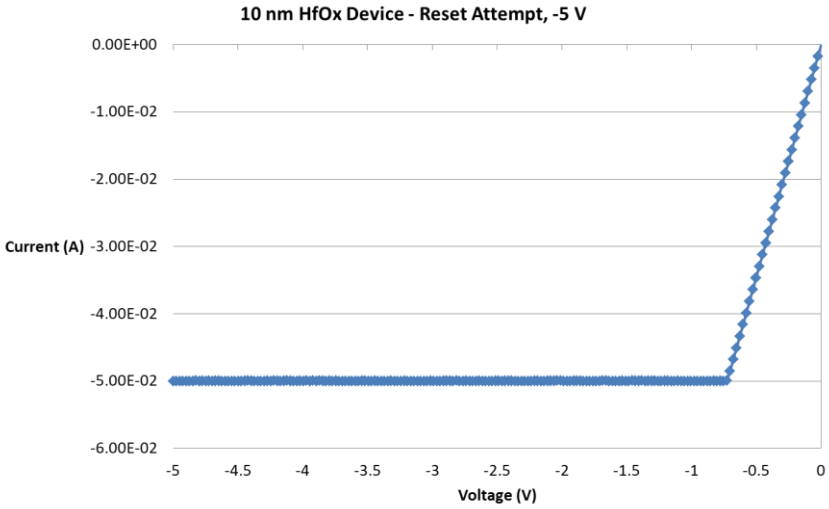

Figure 4.53: Group B bilayer formation attempt, 10 nm. Shorted device.

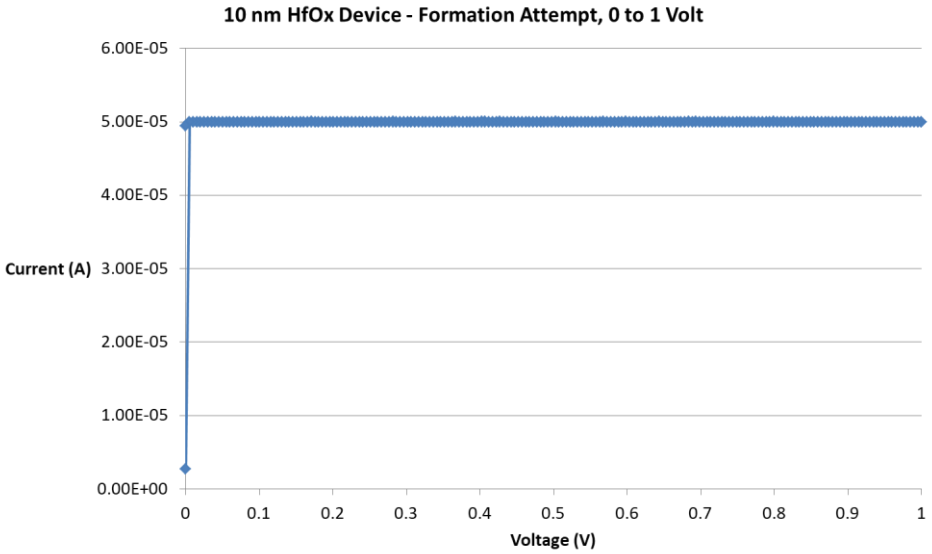

Figure 4.54: Group B reset attempt, 10 nm. Device did not reset at -5 volts.

The working hypothesis at this time is there was an unknown change in the oxide properties at higher thickness levels which led to the devices exhibiting shorted electrical characteristics. The next generation of RRAM fabricated was based on the 2/5 nm AlOx/HfOx RRAM that demonstrated the desired electrical characteristics to validate it as a replicable process for device fabrication. Wire bonding tests were also conducted on memristors from this generation and as shown in Figure 4.54, this was far more consistent than the prior generations were in terms of wire bonds with no shorts and eliminated possible failure modes in this processing step.

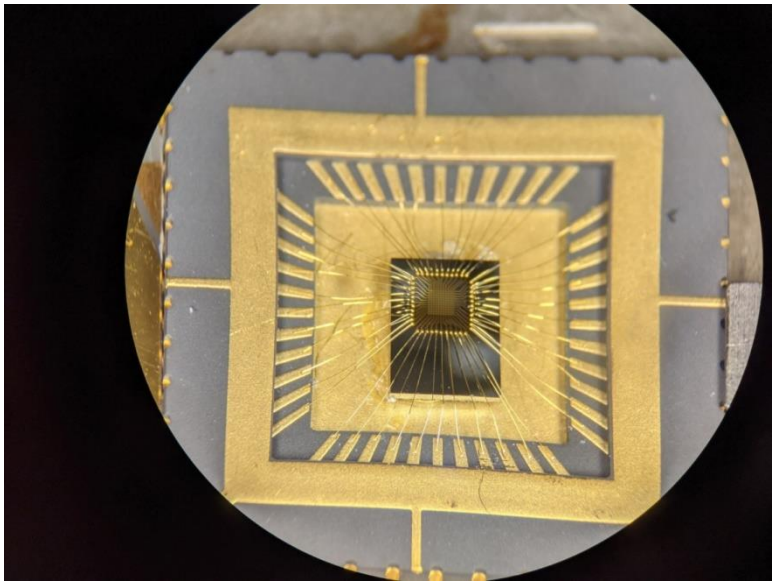

Figure 4.55: Wire bonded memristors, ready for packaging.

4.6 Fifth Generation Memristors

The process for the fourth generation was repeated, one change made at the end of the fabrication process was the incorporation of an anneal step based on a paper by Molina, et al. [Molina 2017] and a paper by Zhang, Hsu, et al. [Zhang 2019] as per their data, annealing HfOx leads to better crystallization and a stronger κ-value for the dielectric strength. The annealing was done at 400 °C for thirty minutes in a 98%-2% nitrogen/hydrogen gas mixture after the final metallization step in the Jepelec Rapid Thermal Anneal system. Two of the four samples were subjected to the anneal, to ensure that the electrical characteristics could be compared and contrasted within the RRAM generation. As can be seen in Figure 4.56, there was heavy carbonization of organic residues on the surface, future annealing will incorporate a ten minute strip cycle in oxygen plasma before anneal to ensure the surface is as clean as possible.

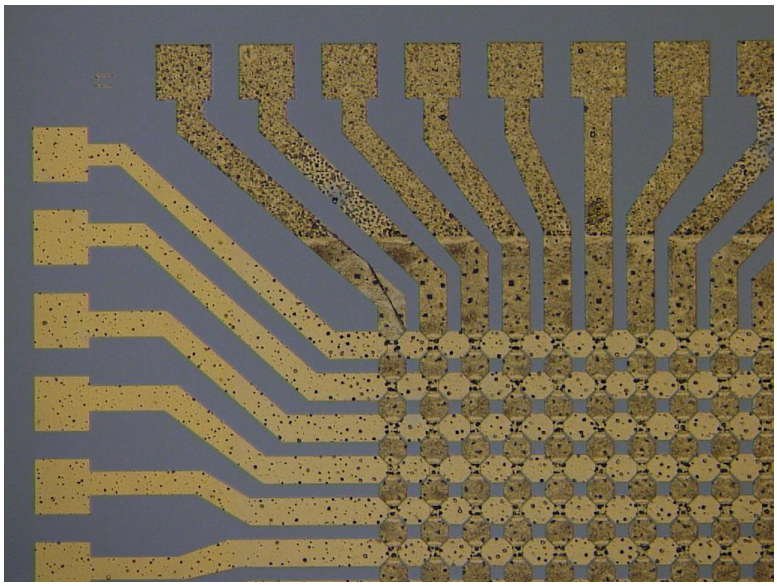

Figure 4.56: Memristor array, post-anneal. Carbonized residue visible across surfaces.

The devices were again characterized electrically at CINT, both groups were tested as can be seen in Figures 4.57 through 4.60. Unfortunately it became rapidly clear both sets of devices were shorted electrically, which should not have happened.

Checking the resistivity of the substrate revealed that the silicon wafer used for the RRAM fabrication had an extremely low κ-value, leading to the entire arrays being shorted as the conduction pathways between the probes was via the substrate, rather than through the fabricated RRAM devices. Work in the spring of 2021 will focus on redoing the previous permutation of oxide layers with substrates that are empirically validated as having a high κ-value before the fabrication begins.

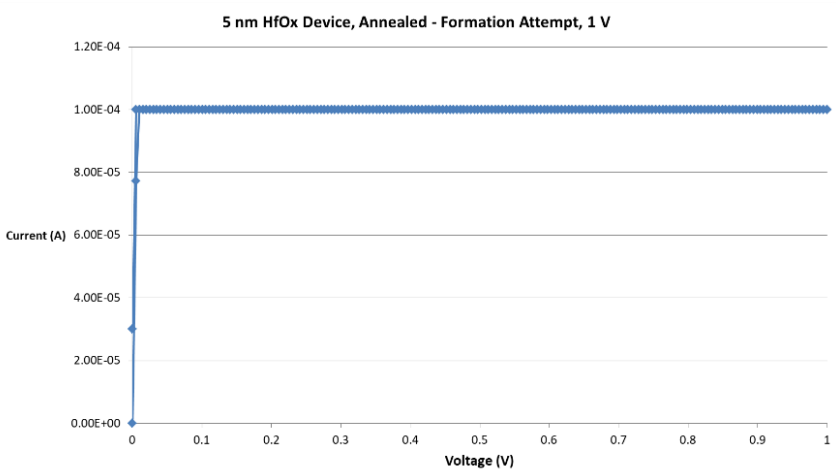

Figure 4.57: Annealed memristor device, formation attempt.

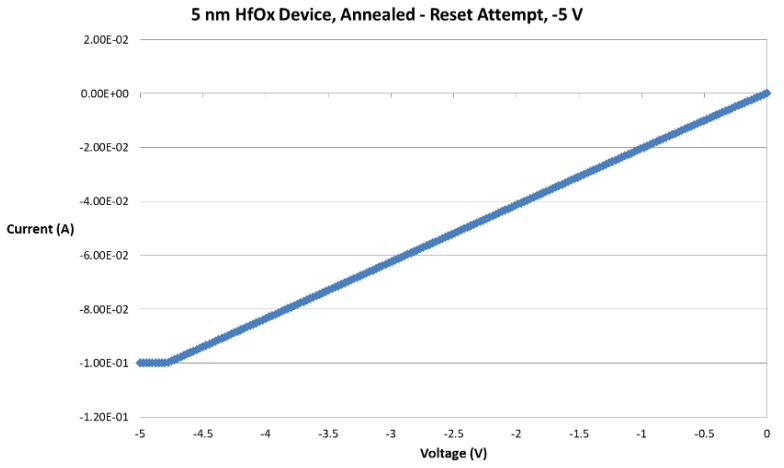

Figure 4.58: Annealed device, reset attempt.

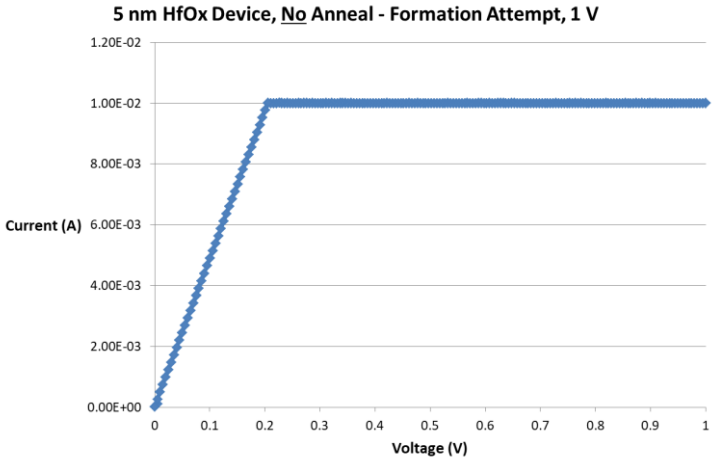

Figure 4.59: Formation attempt, no anneal.

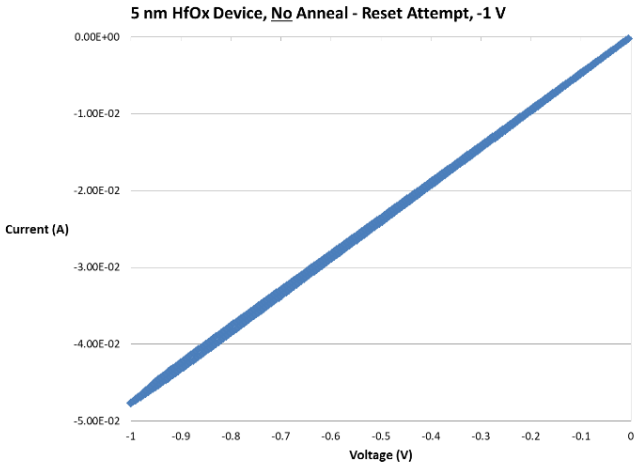

Figure 4.60: Reset attempt, no anneal.

4.7 Sixth Generation Memristors

The process for the fifth generation of hafnium oxide memristor was repeated for this generation with additional steps being incorporated for cleaning the surface of the sample substrates to ensure no organic contamination was present during the annealing of the oxide layer after the top electrode pattern was placed via lithography and metal deposition.

The major change incorporated into this memristor generation is a 10 minute oxygen plasma strip in the LOLA post-lift off of the top electrode to ensure no carbonization occurred during the 30 minute anneal. As can be seen in Figure 4.61, the sample was visibly cleaner and none of the carbonization was observed when the samples were removed from the rapid thermal annealing system.

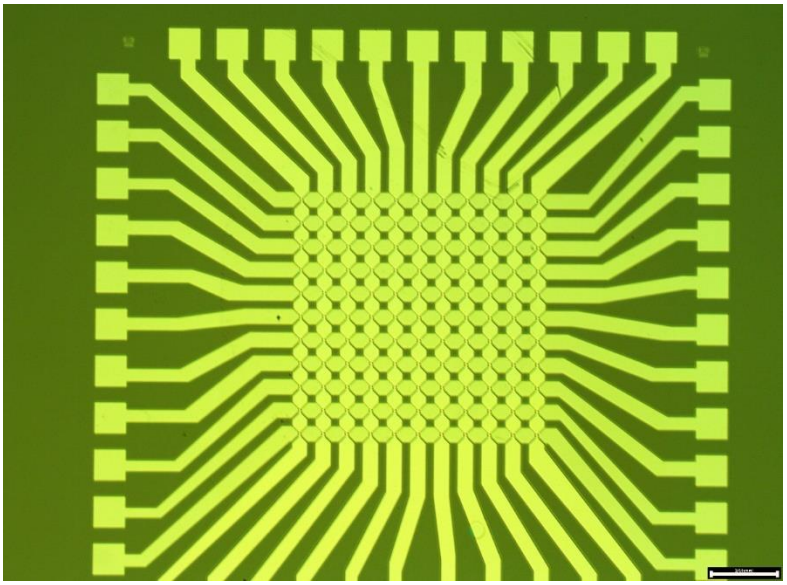

Figure 4.61: Sixth Generation memristors, post-anneal in the RTA.

After the samples were removed from the RTA, they were then characterized electrically using the B1500 Agilent Semiconductor Parameter Analyzer at CINT. Unfortunately the devices were still short circuited, as can be seen in Figures 4.62 and 4.63, so the changes made to the process did not resolve the problems observed previously.

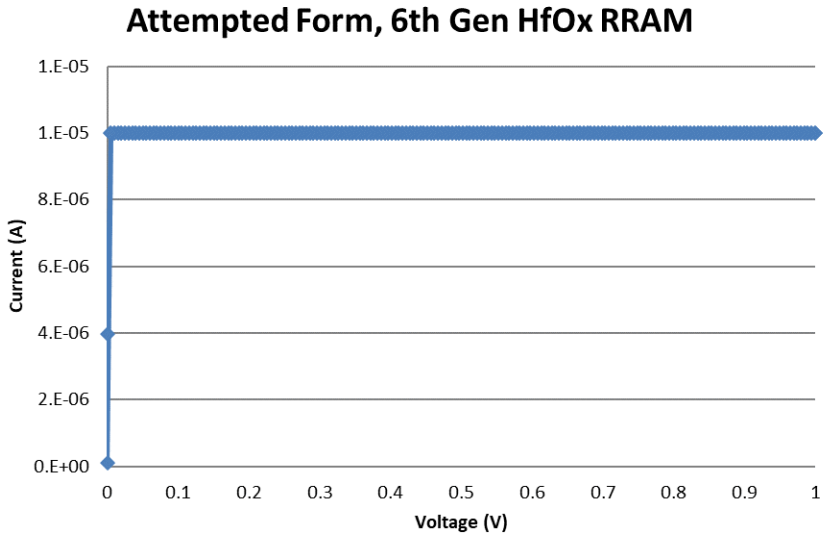

Figure 4.62: Sixth generation memristors, attempted formation.

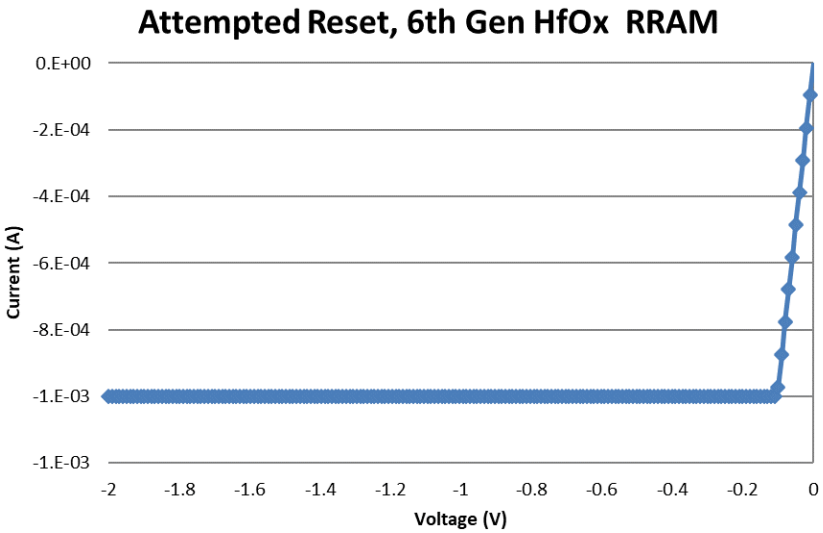

Figure 4.63 Sixth generation memristors, attempted reset.

The mask file was then reevaluated and it was determined that it was possible that the surface was potentially over exposed during the buffered oxide etch step. As hydrofluoric acid is an extremely aggressive etchant even in a buffered state, it was possible that the HF was breaking down too much of the hafnia layer even with the BOE dip being carefully timed to be no greater than 30 seconds before the samples were rinsed with deionized water.

The mask file was then modified in AutoCAD to reduce surface exposure to only the bottom contact pad areas. Figure 4.64 shows the old mask and Figure 4.65 shows the corrected mask. In addition, blank pieces of SiO_2 were cleaned and the oxide layer deposited on them to be inspected via scanning electron microscopy to verify that the oxide layer was not exhibiting crystalline defects.

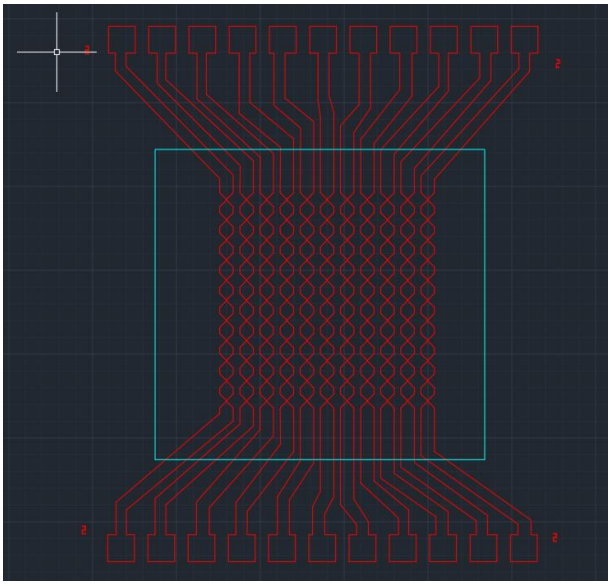

Figure 4.64: Original oxide mask. The area inside blue box is protected, the rest is exposed to BOE.

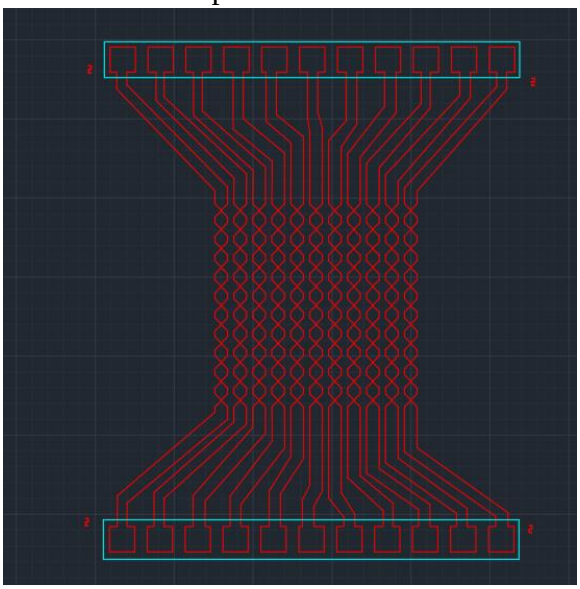

Figure 4.65: Modified oxide mask. The small blue rectangles are the areas exposed to BOE, dramatically reducing the possibility of excessive etching.

Area inside the blue box over the contact pads is exposed, the rest is protected from the BOE so the oxide layer is not undercut by the etch process in the crossbar area. This will hypothetically lead to better results when the memristors are characterized electrically.

4.8 Seventh Generation Memristors

The seventh generation of memristors was fabricated using the modified oxide protection mask with no other changes made to the process to gauge if this change would resolve the short circuit problem. The mask change on the wet etch can be seen in Figure 4.66, where the area exposed is solely the parallelogram over the contact pads.

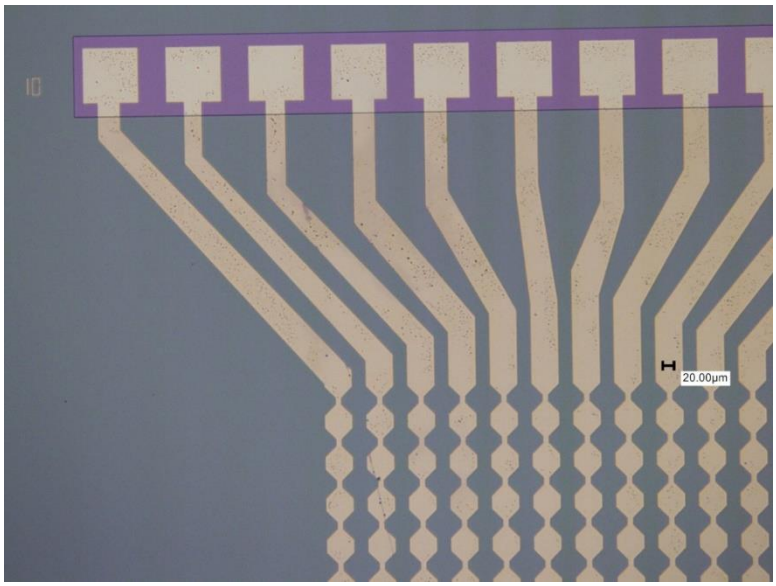

Figure 4.66: Sample from the seventh generation memristors, prepared for BOE dip.

Top metal traces were then laid down via photolithography and the devices characterized electrically. However, the devices were still exhibiting shorted characteristics as can be seen in Figures 4.67 and 4.68.

In addition, blank pieces of SiO_2 were placed into the ALD chamber and hafnia deposited on them as well. One sample was not annealed and the other was subjected to the anneal step in order to compare the results by inspecting them via scanning electron microscopy. As can be seen from Figures 4.69 and 4.70 however, there were no visible crystalline formations or defects which eliminated that as a possible explanation for the electrical shorting being observed in memristors.

After some discussion and debate in the research group meetings as well as consulting with another student, a 20 minute oxygen plasma strip in the LOLA system was incorporated into the fabrication process both before and after the ALD run to ensure no organic contamination was occurring from residues post-liftoff or precursor residuals being left on the surface of the devices.

As titanium chloride had been added to the ALD system, a test run of titania memristors was fabricated in parallel with the eighth generation of hafnia memristors.

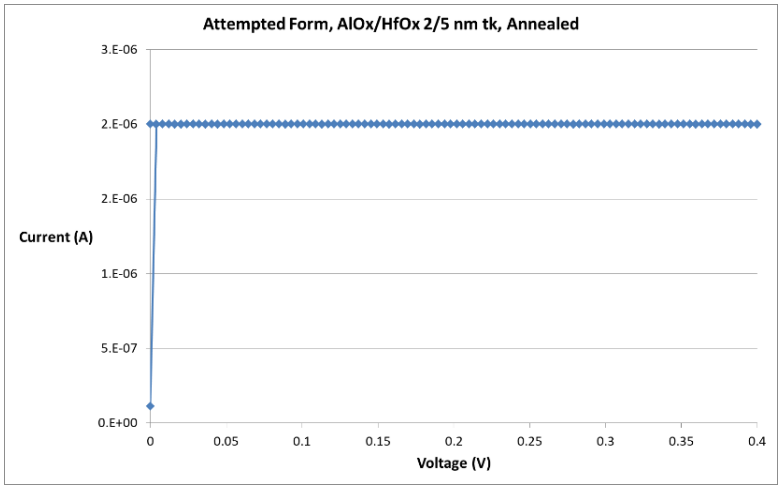

Figure 4.67: Attempted formation, seventh generation memristors.

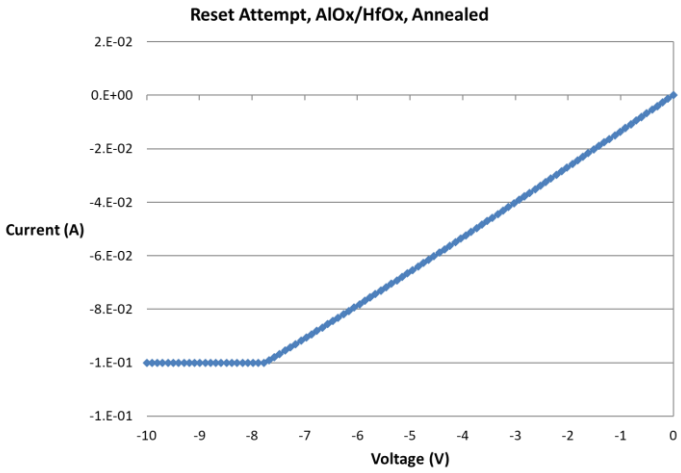

Figure 4.68: Attempted reset, seventh generation memristors.

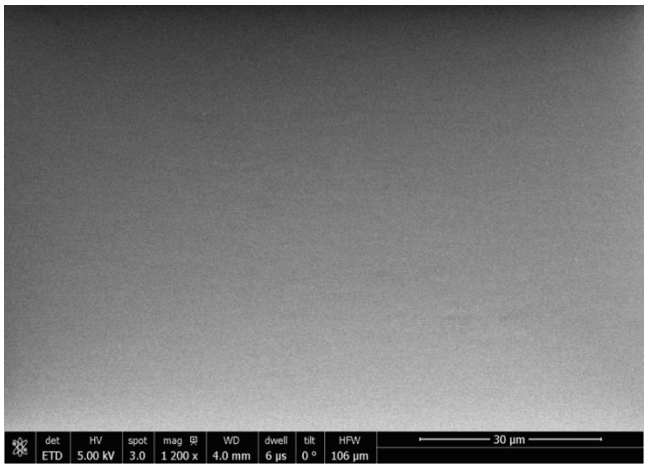

Figure 4.69: Scanning electron microscopy of hafnia with no anneal. No defects.

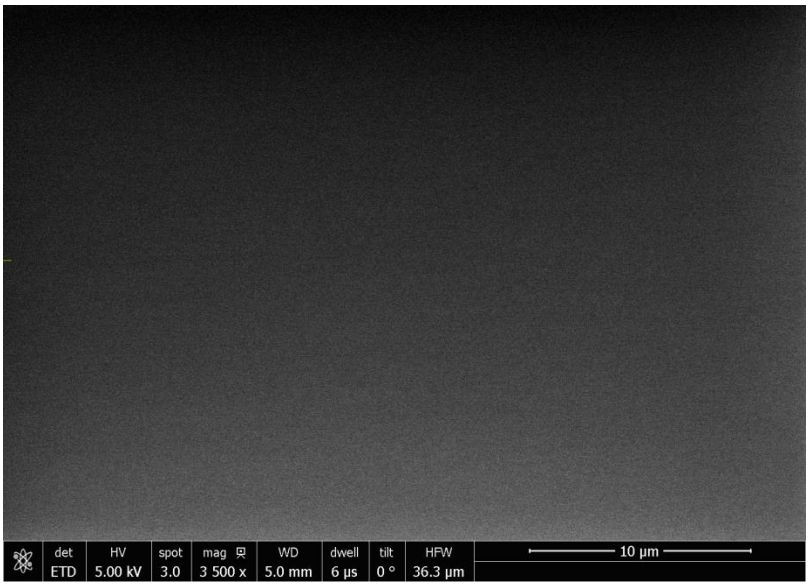

Figure 4.70: Scanning electron microscopy of hafnia with anneal. No defects.

4.9 Eighth Generation Memristors

The eighth generation of hafnia memristors was fabricated with no changes aside from the 20 minute oxygen plasma strip before and after the atomic layer deposition, before the anneal step is conducted.

The titanium dioxide RRAM was fabricated as follows based on the material stack from [Stathopoulos 2017]. The initial layer is 5 nm of alumina formed via TMAH and water at 250 °C. Titania is then grown then on the samples in the ALD system using titanium tetrachloride and water and grown to a thickness of 40 nm at 250 °C. The samples were then annealed for one hour at 600 °C in forming gas to ensure that the titania is in the anatase state, rather than amorphous state that it was grown on the substrate.

The top metal contacts were deposited on both the hafnia and titania memristors in the same metal evaporation run and then the devices were characterized electrically. Unfortunately as can be seen from Figures 4.71 through 4.74, both the hafnia and the titania memristors were shorted electrically again.

This necessitated a thorough review of the fabrication process as no changes made thus far had solved the problem of all devices being shorted or performing poorly, instead of the desired variable resistance performance required for the memristors. Review of the developer solution used in the lithography process revealed that it is composed of 2.38% TMAH in water. As TMAH is one of the precursors used for the creation of the hafnium oxide and the lithography process is a positive-tone process, this led to the formulation of the following hypothesis:

It is possible that the TMAH in the developer was interacting with the oxide layer as it is directly exposed as the developer breaks down the photoresist directly over the areas where the material stack is in order to deposit the top metal for the electrode contacts [Micromaterials 2021]. In turn, this weak chemical breakdown in the oxide layer would cause the electrically shorted behavior observed in all memristors to this point in the fabrication process.

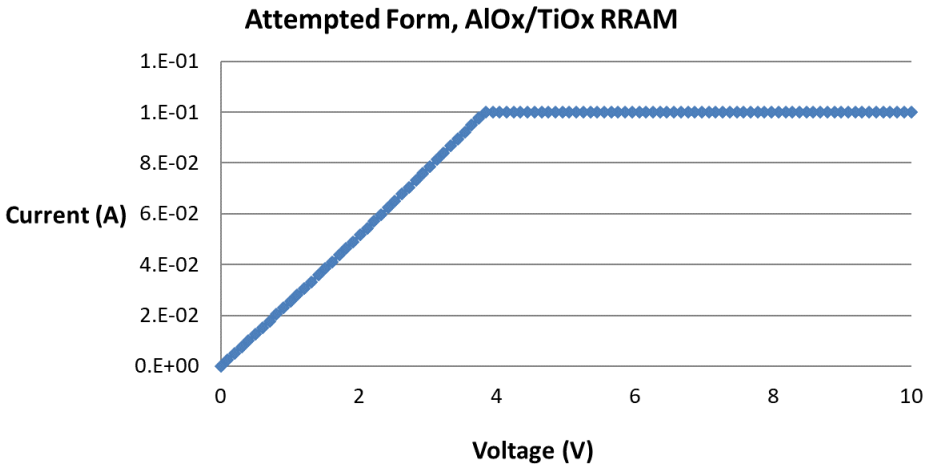

Figure 4.71: Attempted formation, eighth generation hafnia memristor.

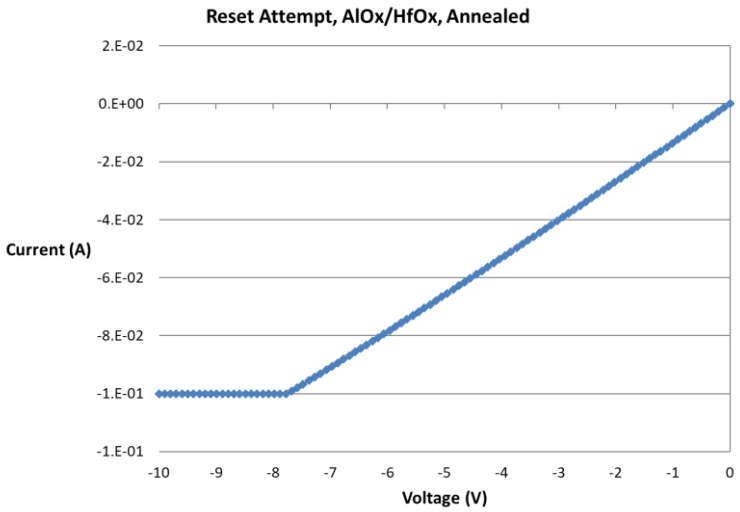

Figure 4.72: Attempted reset, eighth generation hafnia memristor.

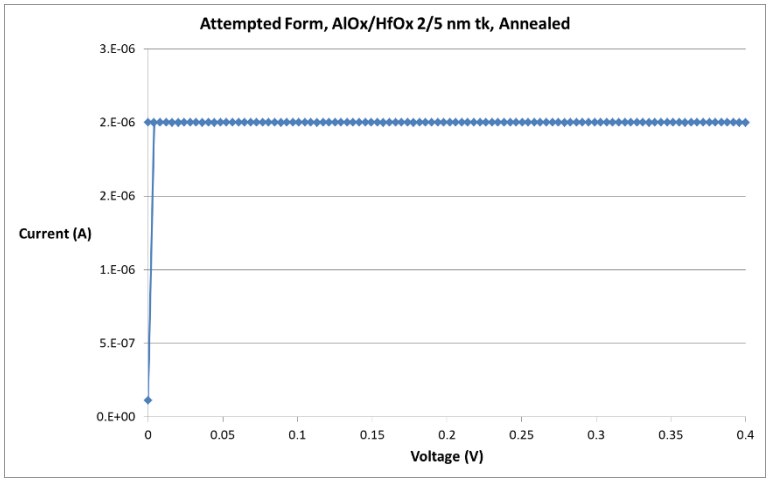

Figure 4.73: Attempted formation, first generation titania memristor.

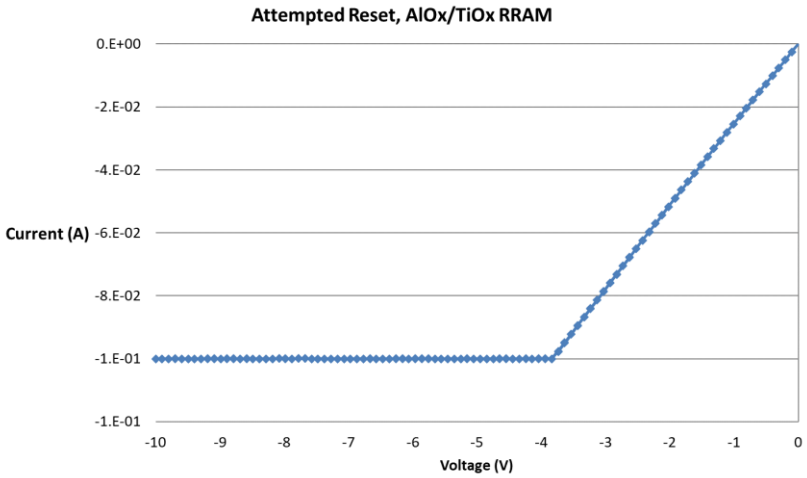

Figure 4.74: Attempted reset, first generation titania memristor.

This hypothesis further suggested that the is a possible solution in that rather than using lithography for the top metal contact, ion milling excess metal away might lead to the desired results. The process for the top metal contact was then completely reworked for the next generation of RRAM to be fabricated.

4.10 Ninth Generation Memristors

The bottom contact was deposited using photolithography, the oxide layer deposited via ALD and the oxide annealed. The major change is that the titanium/platinum layer was deposited without lithography in a blanket coat. After the metal deposition, the samples were then spin coated with AZ5214E photoresist at 5000 rpm for 30 seconds. The samples were then baked at 110 °C for one minute and then the samples exposed at 120 mJ/cm^2 laser energy.

The mask file was inverted, so that when the samples were exposed to MIF 300 developer for 45 seconds, the photoresist would wash away from all areas except the features to be preserved under the ion mill. The samples were then bonded to a carrier wafer with photoresist and etched for 5 minutes to remove the excess metal using the ion mill with the samples orthogonal to the beam. The samples were then soaked in Remover PG overnight and cleaned with acetone, methanol and IPA. Figures 4.75 through 4.78 show the process steps.

The sample was then characterized and the results recorded. The process change was a definite success as three different devices were characterized and all successfully reset and cycled as seen in Figures 4.79 through 4.82. One minor point of concern is the devices all showed as being in the ON state with no formation required and why this is the case is uncertain. But the fact the memristors are now in a working state is a critical step forward.

CINT was closed for several weeks for a maintenance cycle on the cleanroom which, led to switching over to getting the testing apparatus up and running at CHTM. At this time, feedback was received from the reviewers for the *Transactions in Nanotechnology* paper submitted requesting more data in greater detail on the memristors. So it is fortunate this generation of memristors led to working devices for updating the data in the paper.

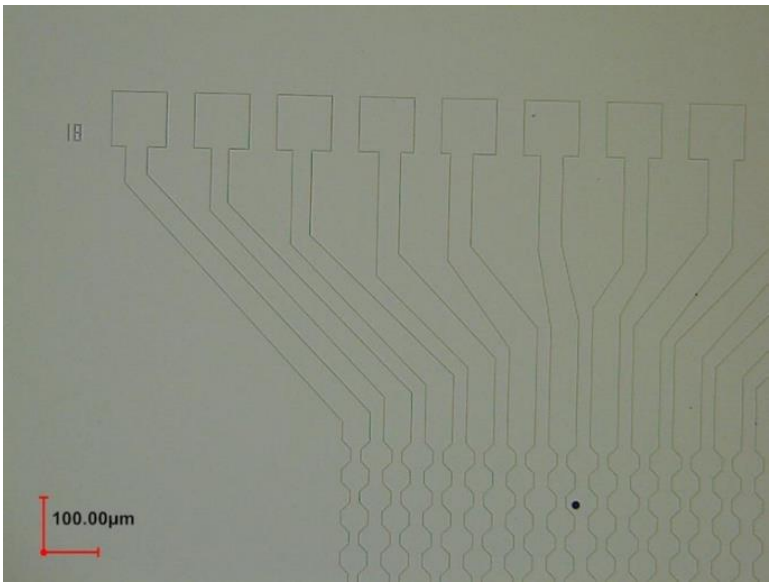

Figure 4.75: Blanket metal coat on sample.

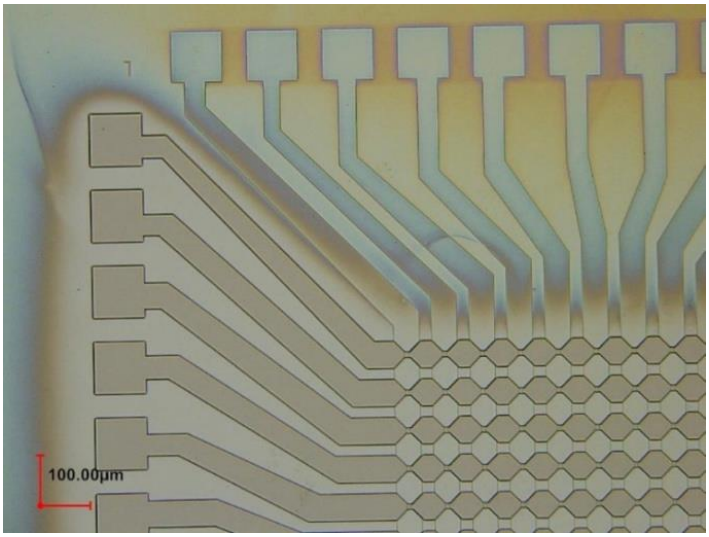

Figure 4.76: Lithography for top electrode pattern.

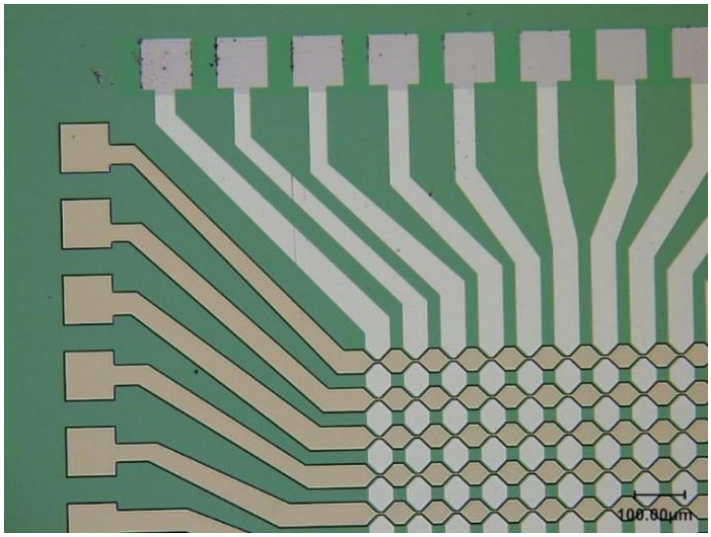

Figure 4.77: Sample post-ion mill, resist still visible on top electrode.

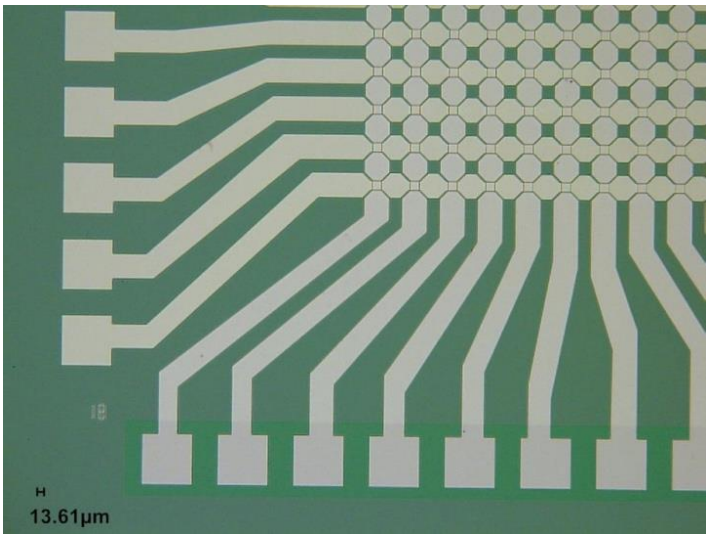

Figure 4.78: Sample post-Remover PG soak. Photoresist fully removed.

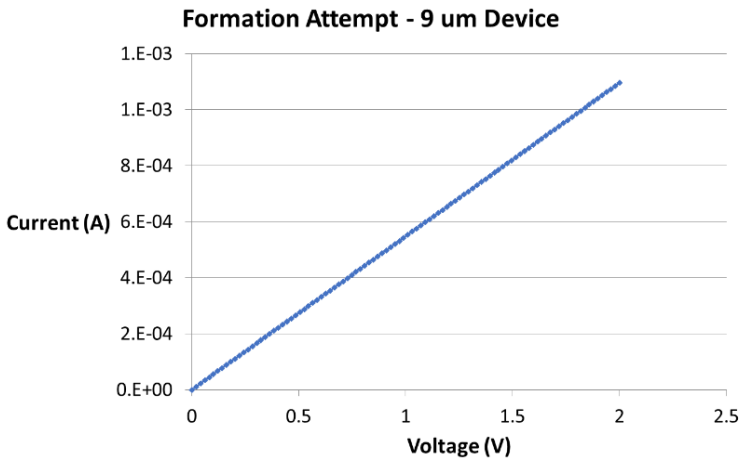

Figure 4.79: Initial formation attempt, memristor would not change state.

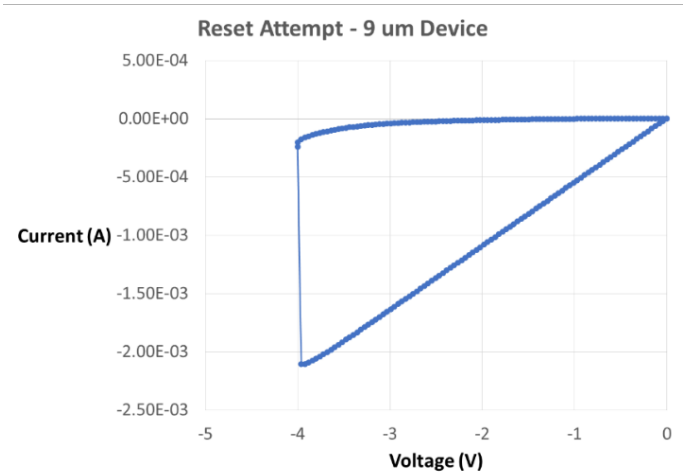

Figure 4.80: Reset attempt, very strong change in state.

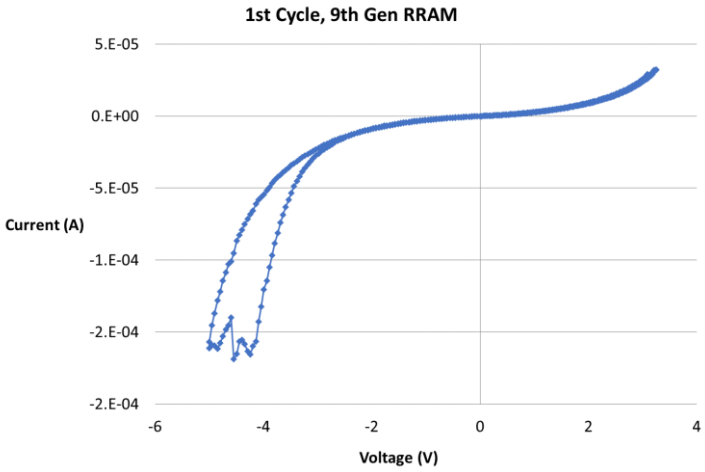

Figure 4.81: First full cycle, hysteresis very pinched in the ON state.

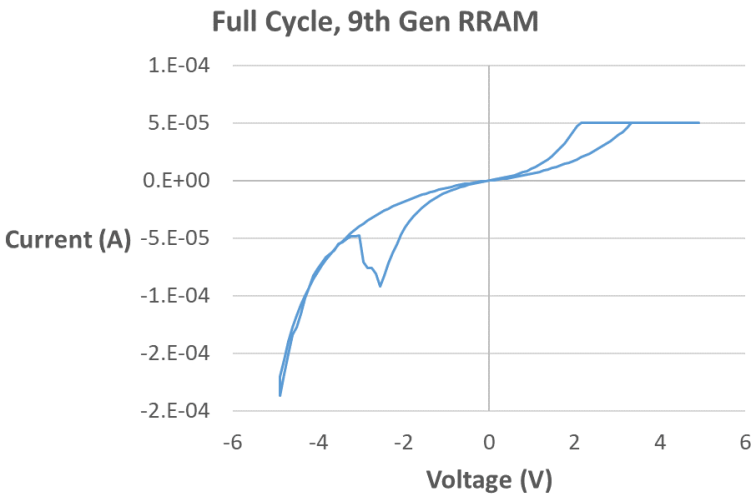

Figure 4.82: Second cycle, hysteresis much broader and state changes well defined.

While the characterization setup at CINT is useful for checking the prototype devices for any working RRAM arrays, it was far too cumbersome for use in characterizing an entire array. Alignment of the whisker probes on the 100 x 100 micron pads while observing their positions via microscrope is a time consuming process. An estimate in terms of the time cost to manually check all devices on an 11x11 array (121 devices total) runs upwards of 24 hours of time using the whisker probes.

Fortunately, the printed circuit board (PCB) designed by Kevin Hastings Barnett enabled much more efficient characterization. The PCB was designed with multiple relays that allow pathways to be made rapidly by bringing individual devices into and out of the testing circuit via commands sent via LabView interface on the computer controlling the testing setup as can be seen in Figures 4.83 and 4.84.

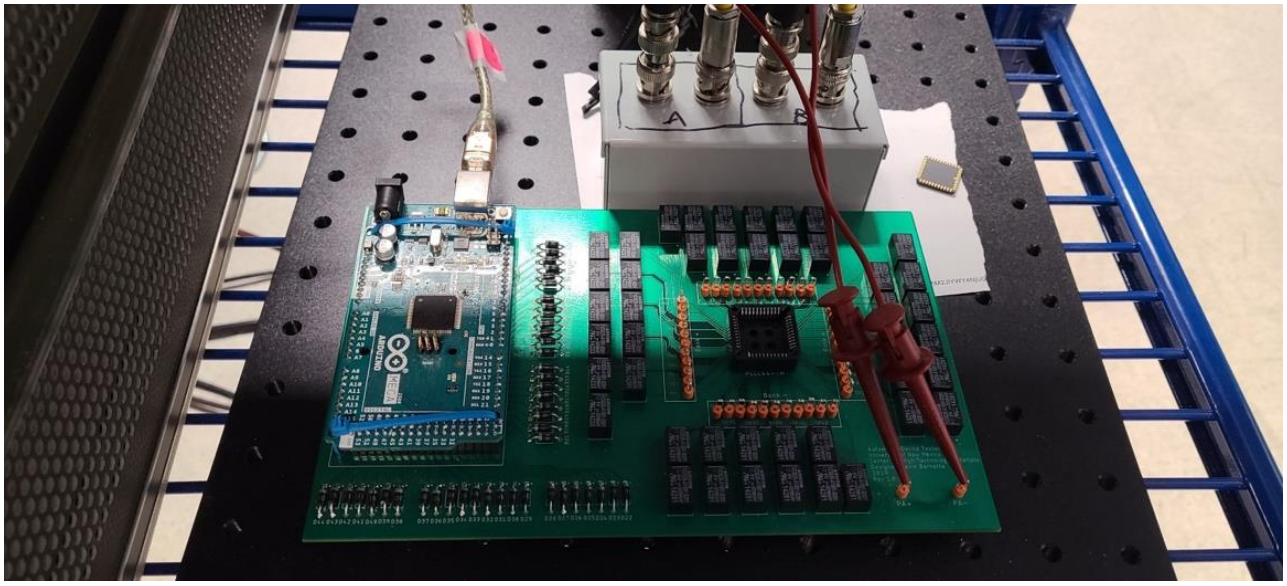

Figure 4.83: Testing circuit board and packaged RRAM [Credit: Landon Schmucker 2021].

Figure 4.84: HP 4145B Semiconductor Parameter Analyzer connected to PCB [Credit: Landon Schmucker 2021].

While fully automating this setup is desirable from an efficiency standpoint, that ideal has not yet been realized due to the sheer technical complexity of doing so from a programming point of view. However, Landon was able to successfully get the PCB, parameter analyzer and Labview control interface talking to one another with minimal delays which was acceptable given the two week deadline we had for data collection. Memristors from the ninth generation were wire bonded, packaged into the LCC04435 packages and then characterized. An entire row of the 11 micron devices was then fully tested and cycled successfully and the updated information was incorporated into the TNANO paper as seen in Figure 4.85.

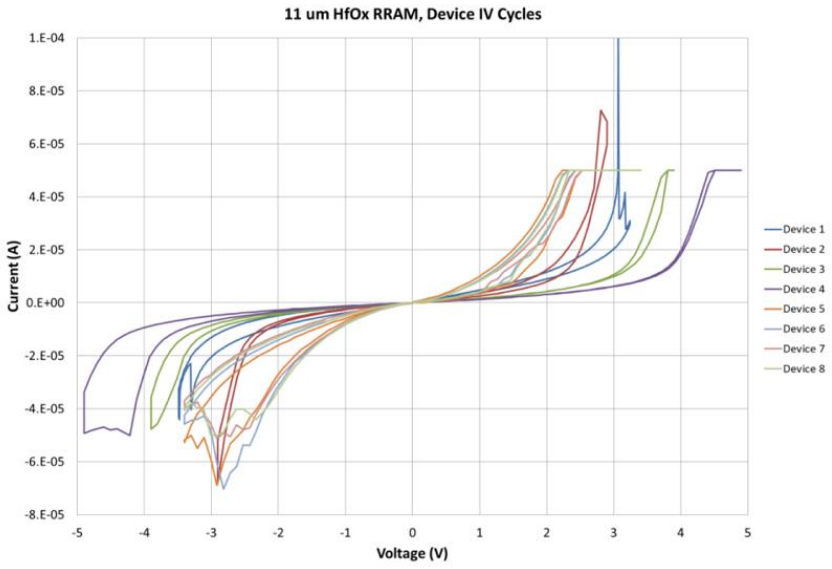

Figure 4.85: All cycled devices from the 11 um array, one row fully characterized. The three memristors that failed characterization were omitted.

Several other rows were characterized, but did not show good results unfortunately. The yield for the entire array was then estimated as being ~27% which is not terribly high, but improvements made to the process should lead to greater overall yields as the fabrication is refined further. Problems were encountered in cycling the 6 micron array as all previously tested devices were showing as open circuits on testing on the second day. Investigation revealed that there were high levels of electrostatic discharge (ESD) occurring around the testing station, leading to the conclusion that ESD was causing the metal traces to blow out. An ESD wrist connector was added to the station, as well as additional grounding for the PCB to ensure this did not continue. Concurrent to the data collection, Landon was trained on how to characterize the RRAM so this part of the process could be handed over to him while I returned to CINT to fabricate further generations of RRAM.

The tenth generation of RRAM was fabricated using the exact same process of the ninth generation to validate the fabrication process fully.

4.11 10th Generation

Process was run successfully up to the ion mill processing stage, at that point there were some serious problems with the process as seen in Figures 4.86 and 4.87. At this point the exact problem had not been isolated so a rework of the process was redone with a new generation.

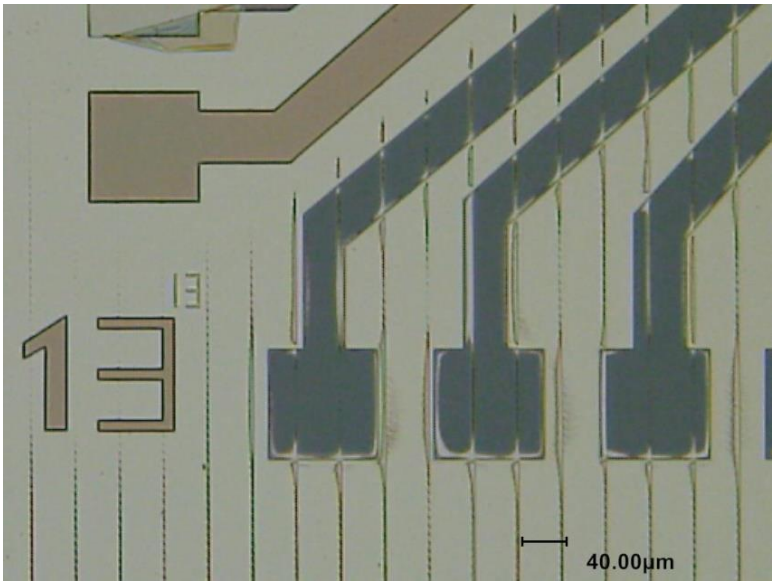

Figure 4.86: Bottom trace gone while ion milling incomplete.

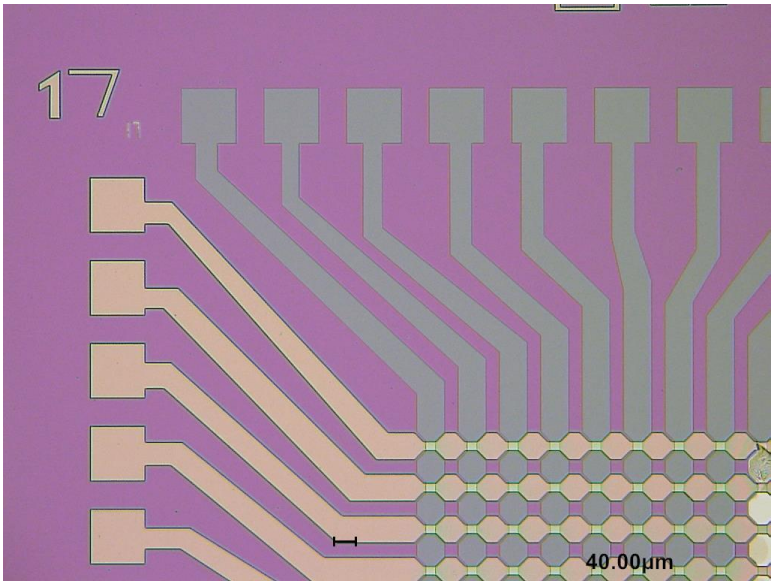

Figure 4.87: Platinum milled off from bottom trace when finished. This should not have happened based on programmed parameters for the ion mill.

4.12 Eleventh Generation Memristors

The fabrication process from the 10th generation of RRAM was done a second time and the calculations for the ion mill were recalculated as follows in Equations 4.1 and 4.2 based on the initial etch rate values, per the chart for the ion mill.

Equation 4.1 Mill rate for platinum: $620\frac{\text{Å}}{\text{min}} * 1\frac{\text{nm}}{\text{Å}} = 62\frac{\text{nm}}{\text{min}} \ \therefore 300\ \text{nm} \div 62\frac{\text{nm}}{\text{min}} = 4.83\ \text{min}$

Equation 4.2 Mill rate for titanium: $330\frac{\text{Å}}{\text{min}} * 1\frac{\text{nm}}{\text{Å}} = 33\frac{\text{nm}}{\text{min}} \ \therefore 40\ \text{nm} \div 33\frac{\text{nm}}{\text{min}} = 1.21\ \text{min}.$

As can be seen from the theoretical calculations, six minutes should be sufficient to remove the excess metal from the top layer and the bottom metal traces would remain intact. However, consultation with John Nogan revealed that the problems I was seeing was elamination of the bottom metal due to organic residue contamination on the substrate. As the sample heated under the ion mill, the residue was changing to a gas state which would break the adhesion of the metal, in turn leading to the bottom metal trace being milled away. So I then ran the ion mill testing a preliminary sample of the four prototypes that showed irregular coloring under the blanket metal coat which in turn confirmed that I was indeed seeing delamination as seen in Figure 4.88.

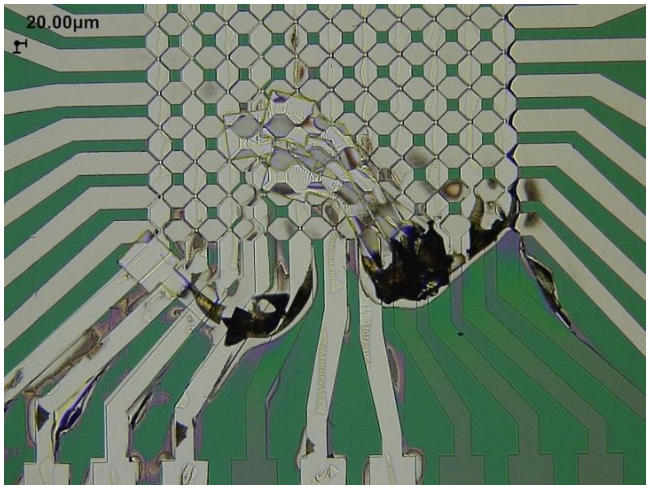

Figure 4.88: Delamination extremely visible on test sample.

The remaining 3 samples were then run with a shorter mill time, decrementing the total mill time by 15 seconds each time to evaluate the final results. The results from the next mill were still showing delamination as can be seen in Figure 4.89.

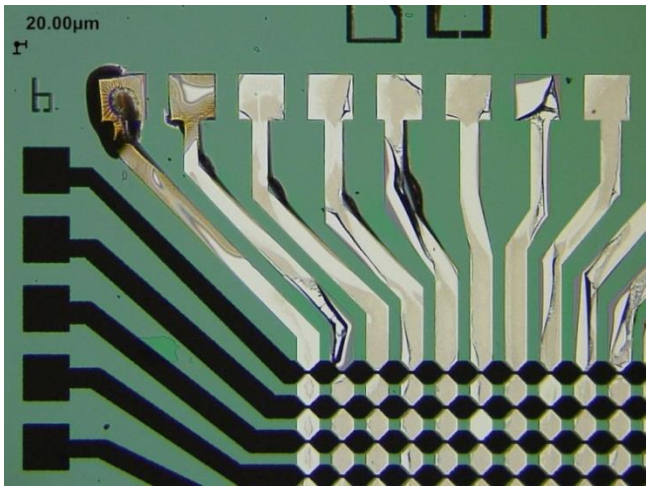

Figure 4.89: Delamination still occurring on the sample.

The next sample was then run with another decrement of 15 seconds for a total reduction of 30 seconds from the original mill time and the results were much closer to the desired outcome as seen in Figure 4.90.

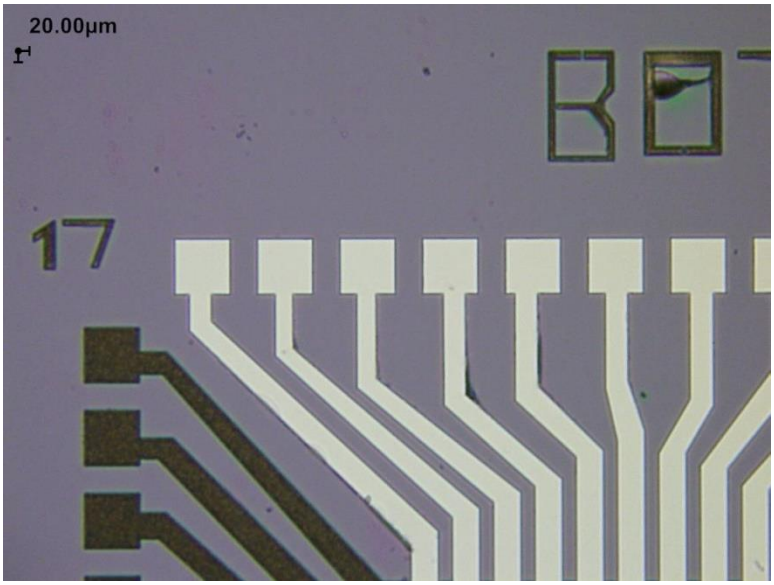

Figure 4.90: Delamination eliminated, ideal etch result.

The process with the mill time from the third sample was then run for the fourth sample, unfortunately the carrier wafer cracked while the sample was being milled as shown in Figure 4.91. This led to over milling the metal as the sample was closer to the ion beam than it should have been as can be seen in Figure 4.92.

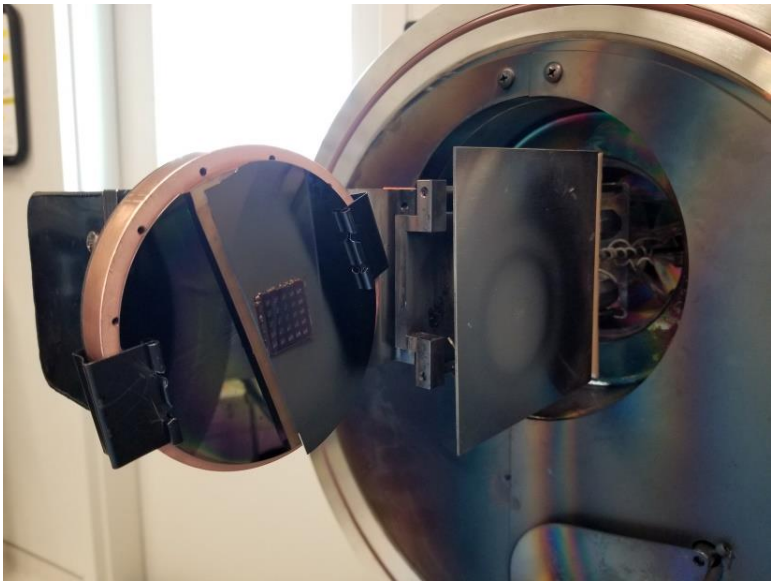

Figure 4.91. Carrier wafer on removal, visibly cracked in half.

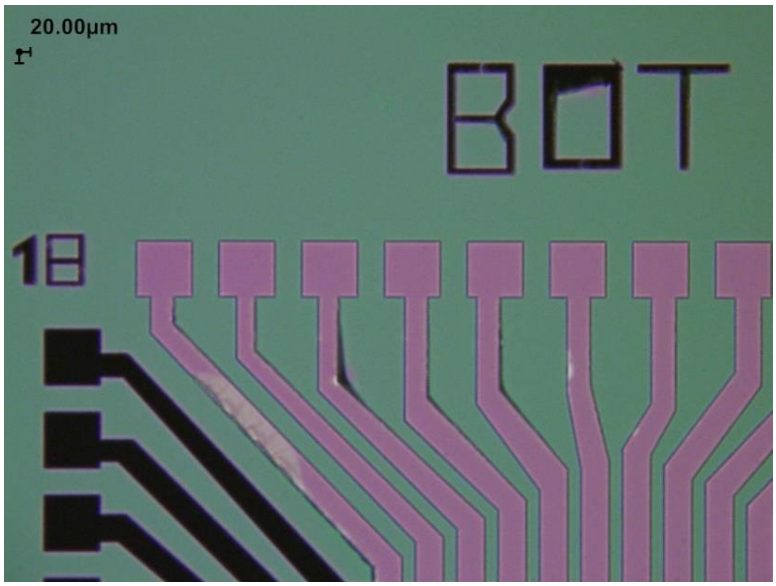

Figure 4.92. Overmilling visible and the metal for the bottom trace milled away due to beam angle and distance changing as a result of the wafer breaking mid-process.

The third sample was then characterized electrically, which did show good hysteresis curves as can be seen in Figures 4.93 through 4.95. This empirically validated the fabrication process as capable of fabricating working memristors on a consistent basis.

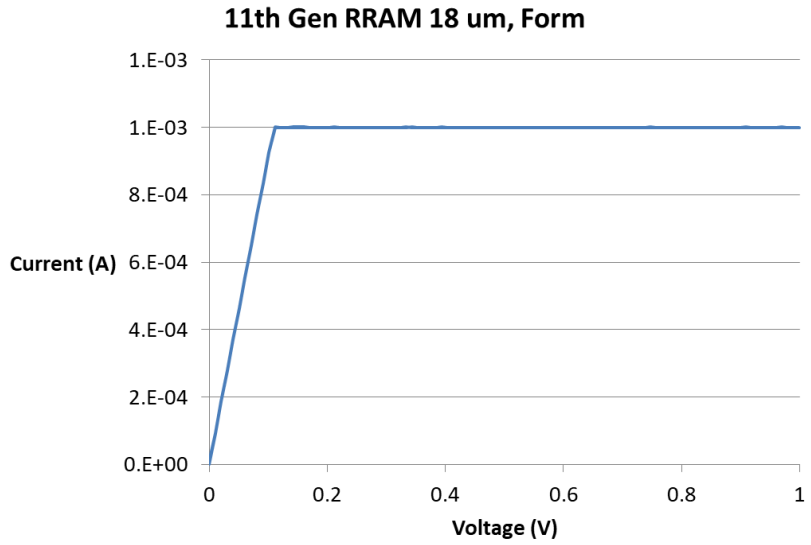

Figure 4.93: Eleventh generation hafnia memristor formation attempt, device pre-formed.

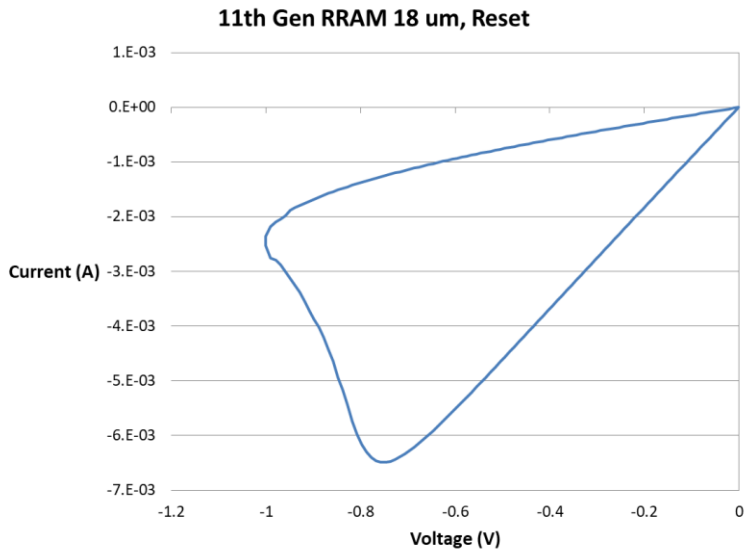

Figure 4.94
: Eleventh generation hafnia memristor reset, device reset successfully.

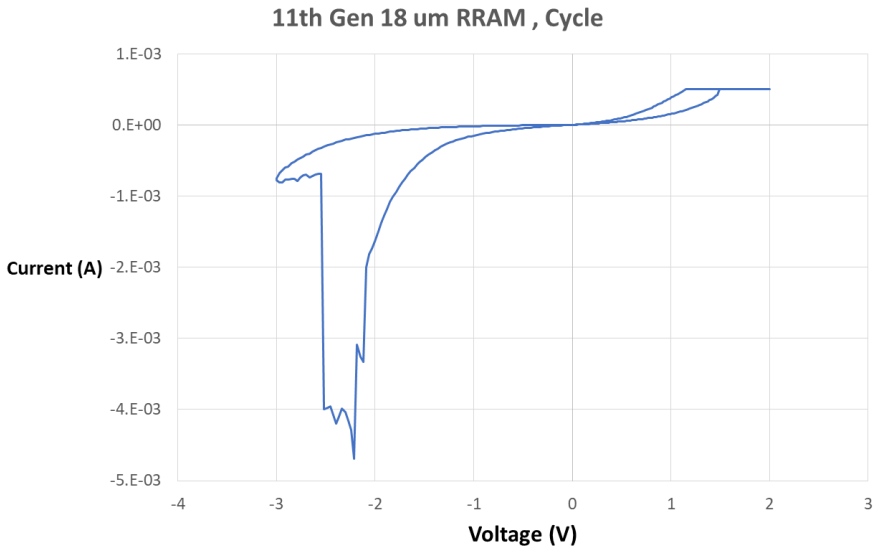

Figure 4.95: Eleventh generation hafnia memristor cycle, hysteresis not ideal but still viable.

The twelfth generation of RRAM was then fabricated with a process change incorporated into the substrate clean steps where the samples are then given a 10 minute oxygen plasma scrub before the lithography is done for the bottom and top metal traces so as to guarantee no organic contamination from solvents and that the delamination does not occur.

4.13 Twelfth Generation Memristors

The twelfth generation of RRAM was successfully fabricated with the process changes made to ensure no organic contamination occurred under the metal traces as can be seen from Figures 4.96 and 4.97.

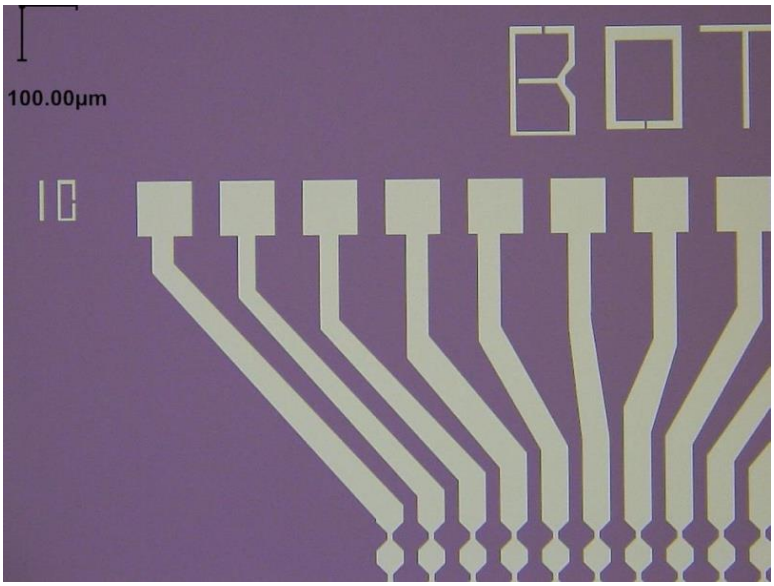

Figure 4.96. Bottom metal trace post-liftoff, no irregularities observed in array.

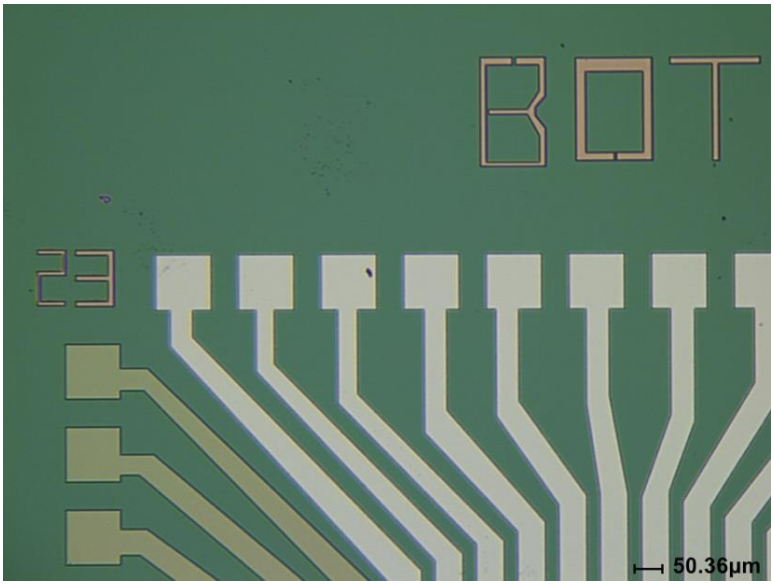

Figure 4.97. Top metal trace post-ion mill, no delamination visible.

However, when testing the devices a problem arose which is that the RRAM was all shorted electrically as can be seen in Figures 4.98 and 4.99. This was a serious issue, as the devices by all logic should have worked in a fashion similar to the prior working generations of RRAM. Deeper investigation suggested that it was possible contamination from prior ALD runs in the system used for oxide growth may have caused faults that were not visually observable, but would lead to electrical failure when tested. To check this hypothesis, the thirteenth generation was fabricated in two forms. One set of RRAM would be fabricated using the common-access ALD system. The other set was fabricated using a dedicated ALD system reserved solely for alumina and hafnia, courtesy of Troy Hutchins-Delgado having access to this system through another research group at CINT.

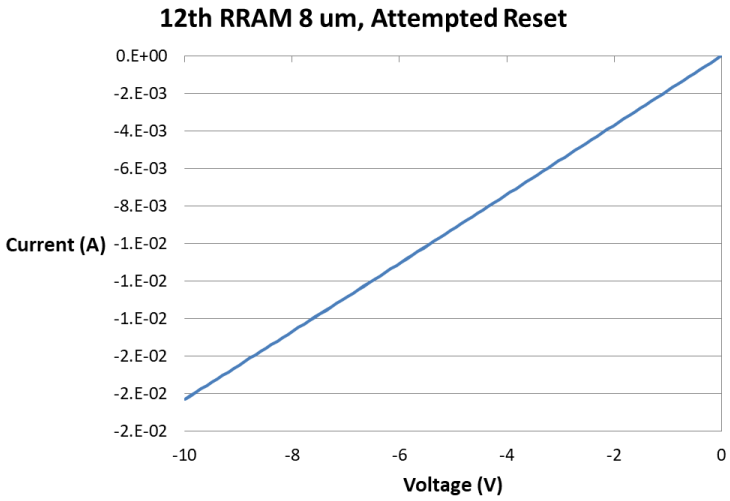

Figure 4.98: Attempted reset for 13 micron twelth generation memristor. No change at -10 volts.

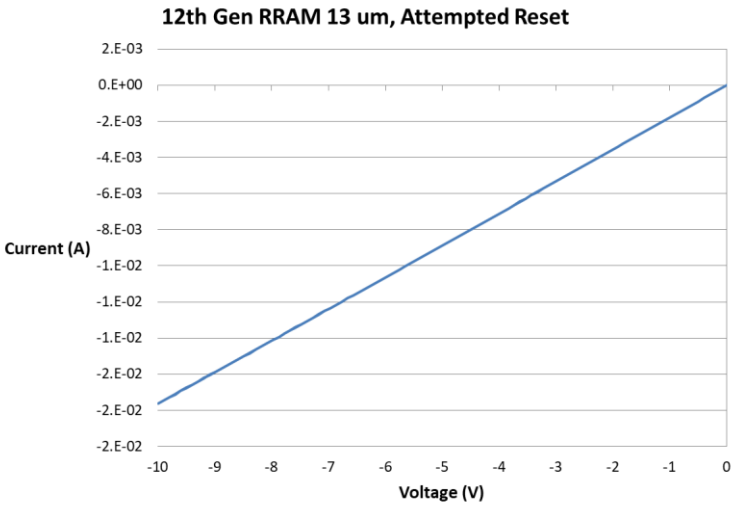

Figure 4.99: Attempted reset for 8 micron twelfth generation memristor. No change at -10 volts.

4.14 Thirteenth Generation Memristors

The thirteenth generation of memristors followed the same fabrication process as the twelfth generation, with the major variation occurring in the oxide growth. Group A had oxide deposited using the regular ALD system, Group B had the same thickness of oxides (2 nm alumina, 5 nm hafnia) grown on them in an ALD system that is reserved solely for the growth of alumina and hafnia and no other oxides. The samples were successfully milled with the ion mill as can be seen in Figure 4.100, showing that the oxygen plasma strip before metal deposition for top and bottom contacts successfully removed all possible contaminants from the surface. Then one sample was characterized electrically from the regular ALD system and one sample from the dedicated ALD system was characterized and the results compared. Analysis of the hysteresis curves shows that the regular ALD system did indeed have contamination affecting the electrical performance of the ultrathin hafnia films as shown in Figures 4.101 through 4.104.

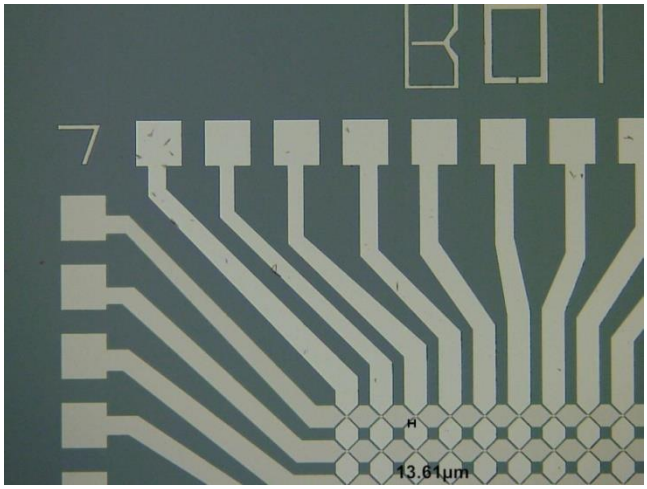

Figure 4.100: Thirteenth generation memristor post-ion mill and resist removed.

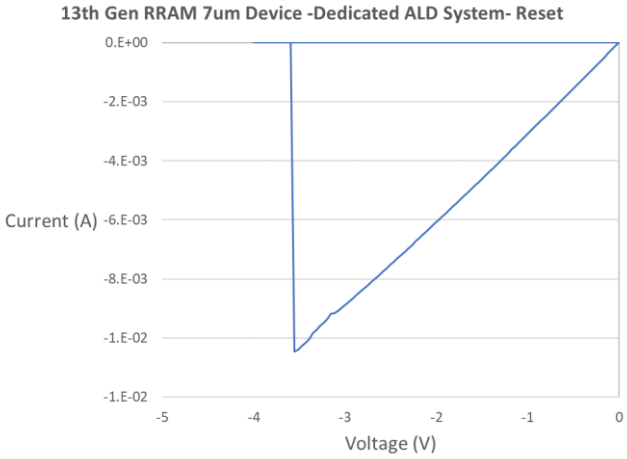

Figure 4.101: Thirteenth generation memristor, reset well defined at -3.5 volts. From the dedicated ALD system.

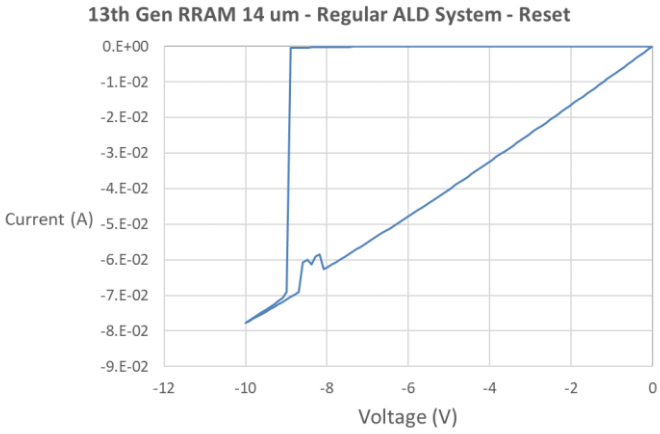

Figure 4.102: Thirteenth generation memristor, reset at -9 volts. From the open-access atomic layer deposition system.

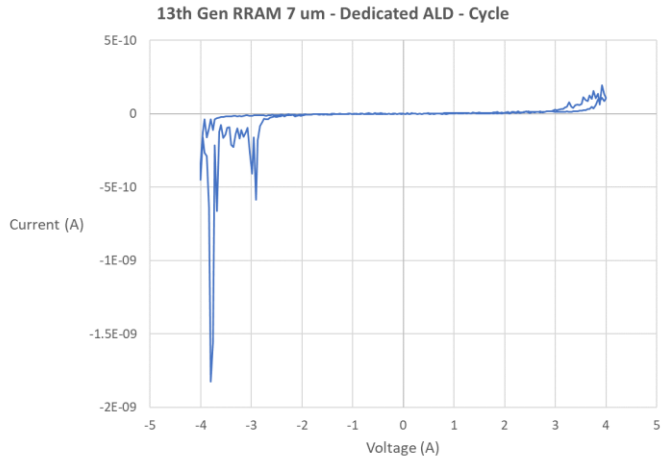

Figure 4.103: Thirteenth generation memristor, full cycle.
From the dedicated ALD system.

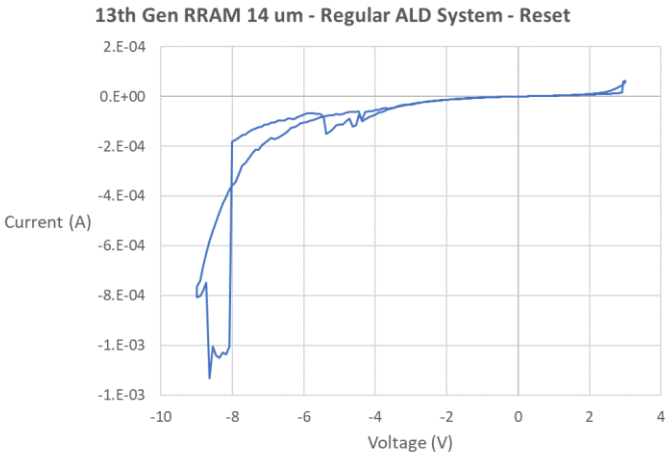

Figure 4.104: Thirteenth generation memristor, full cycle.
From the normal open-access ALD system.

In order to resolve this issue, the ALD system will be subjected to an oxygen plasma strip to first clean the chamber, as well as a preconditioning run with the planned recipe. Then the actual deposition will occur. In this way, contaminants can be controlled and kept to a minimum. This process change will be deployed in the fourteenth generation of hafnia memristors.

4.15 Fourteenth Generation Memristors

The fourteenth generation of hafnia memristors was fabricated with the changes made in how the ALD system was utilized for oxide growth. The reaction chamber was scrubbed with an oxygen plasma strip for ten minutes at 250 °C to remove any and all possible organic contaminants. The chamber was then preconditioned by running a full deposition cycle for 2 nm alumina and 5 nm hafnia without the memristor samples in the reaction chamber. The memristor samples were then loaded into the chamber and the 2/5 nm alumina/hafnia layers deposited. The rest of the process following this change was identical to prior generations. Once completed, the memristor arrays were characterized electrically to observe how this impacted their performance as shown in Figures 4.105 through 4.107.

The conclusions that were drawn from this generation are as follows:

Devices are still registering as pre-formed, likely due to residual charge trapped in the oxide layer from the ion milling process, leaving the memristors into the ON state.

Reset and cycle hysteresis curves are much improved, demonstrating that the cleaning and preconditioning of the ALD system is improving the overall performance of the memristor oxide layer.

At this point, it can be concluded that the 2/5 nm alumina/hafnia memristors are working as intended and the process sheet shall be fully updated and frozen.

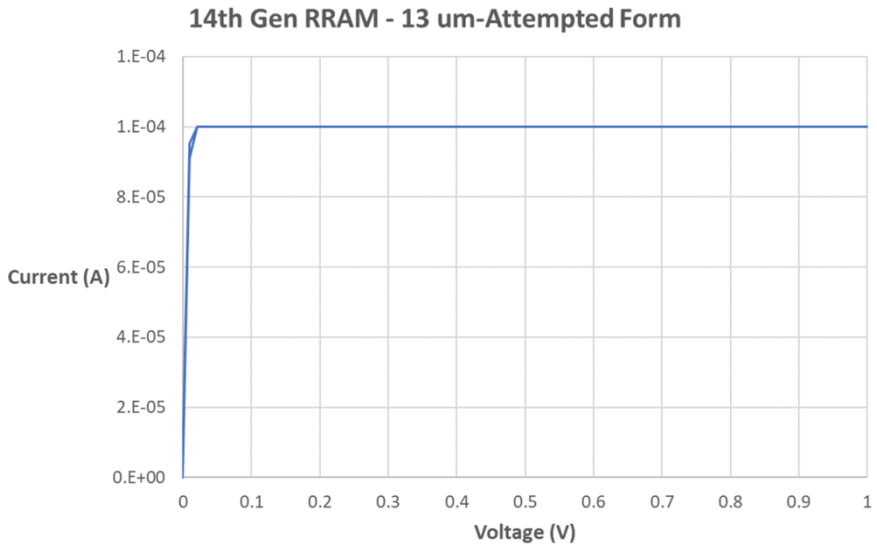

Figure 4.105: Fourteenth generation hafnia memristor, formation attempt.

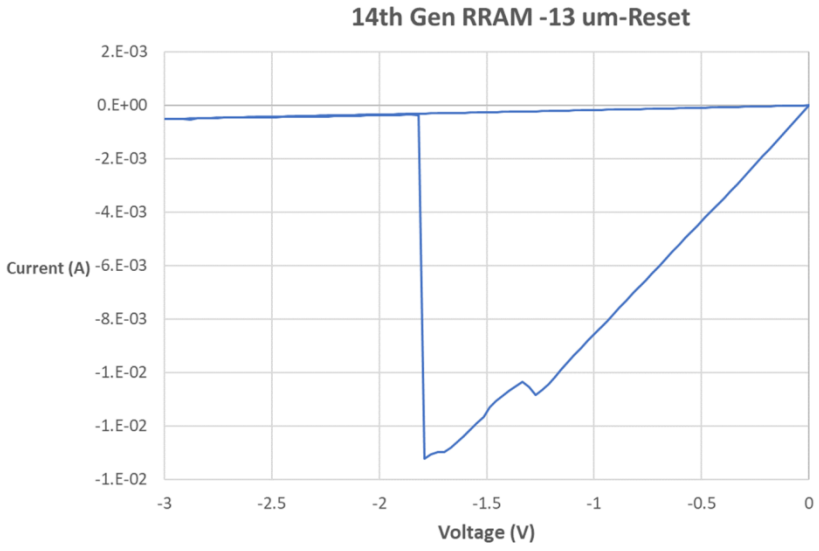

Figure 4.106: Fourteenth generation hafnia memristor, reset.

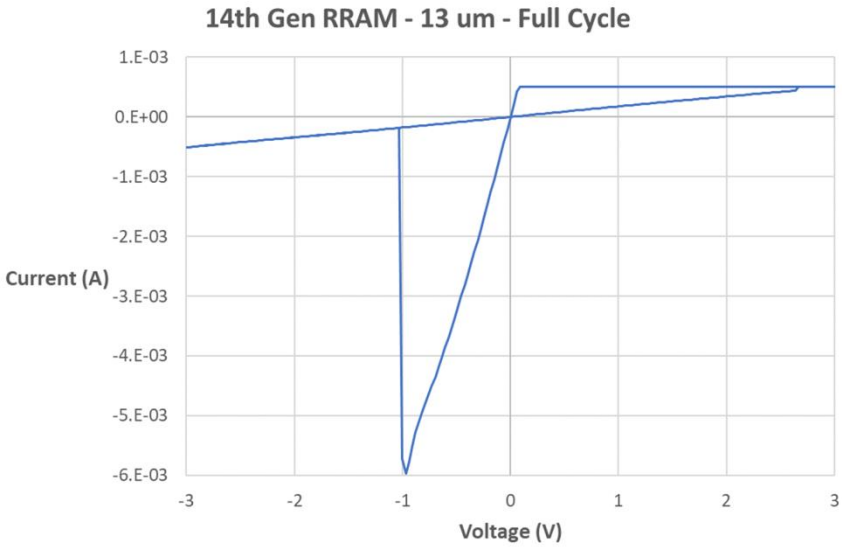

Figure 4.107: Fourteenth generation memristor, full cycle.

4.16 Fifteenth Generation Memristors

In the fifteenth generation of memristors, hafnia memristors were fabricated using the exact same process as the fourteenth generation with no significant changes to ensure successful replication of the fabrication process. Titania memristors were also fabricated for a second time using a process outlined previously from [Stathopoulos 2017] while also implementing the ion mill process for the top electrode pattern.

The bottom electrode pattern resolved successfully for all samples as they were all given the same lithography and metal deposition of 10/150 nm titanium/platinum as can be seen in Figure 4.108.

The samples were then split for the separate atomic layer deposition processes.

The hafnia memristors received the 2/5 nm alumina/hafnia layer and the titania memristors received a 5/40 nm alumina/titania layer. It was noted that the oxide layer was clearly visible on the titania memristors, so a determination was made to attempt a buffered oxide etch for three minutes to see if it would remove the excess oxide as seen in Figures 4.109 and 4.110.

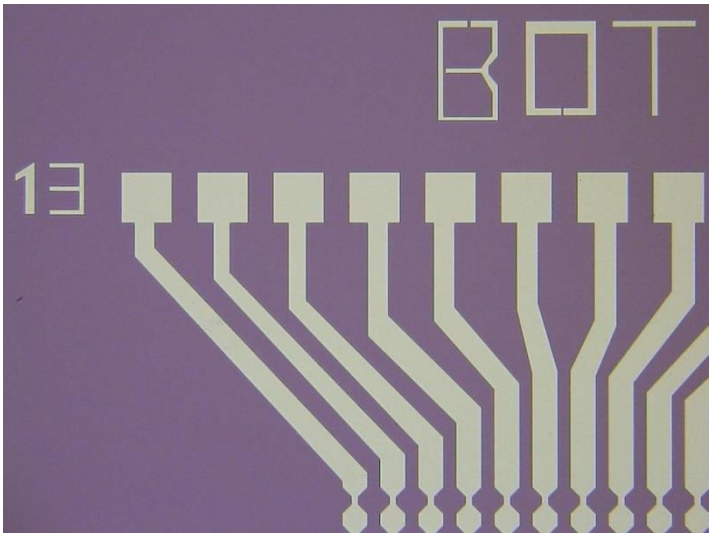

Figure 4.108: Fifteenth generation, bottom electrode post lift off.

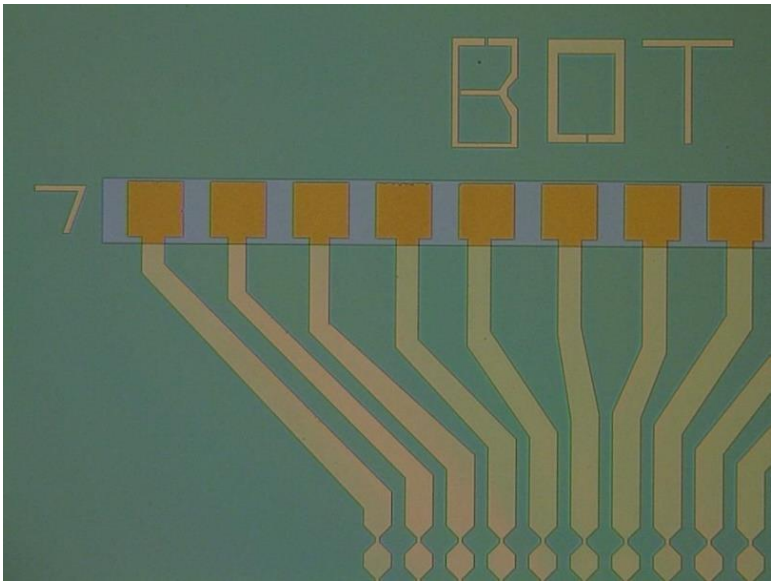

Figure 4.109: Second generation titania memristors. Lithography for BOE etch clearly defined.

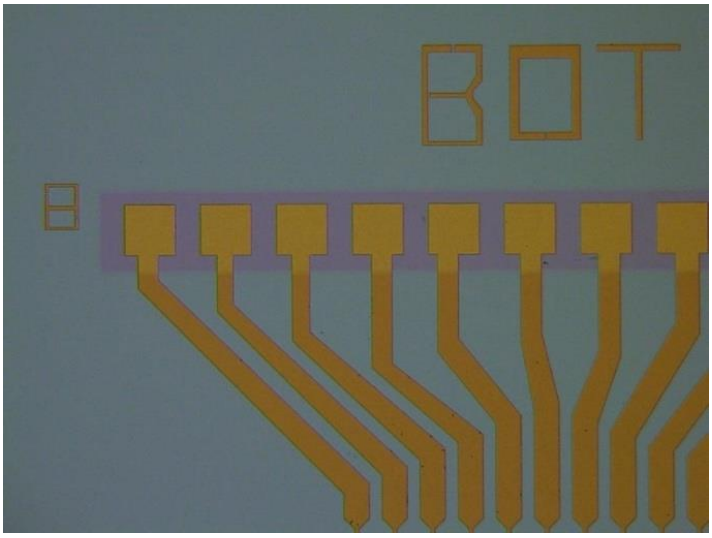

Figure 4.110: Second generation titania memristors after BOE dip.

The samples were then given a blanket metal deposition of 10/300 nm titanium/platinum, spin coated at 5000 rpm with AZ5214 photoresist and then exposed at 120 mJ/cm^2 and developed with AZ MIF 300 developer solution for 45 seconds. The patterns were well defined as can be seen in Figure 4.111.

The samples were then bonded to carrier wafers, and exposed to the ion mill for 5 minutes and 15 seconds to ablate away the excess metal as can be seen in Figures 4.111 and 4.112. However, the bottom electrode pattern showed unexpected breakdown as seen in Figure 4.113. This indicated that the buffered oxide etch had undercut the metal-silicon bond and the ion mill beam then broke the metal traces down. Therefore, the BOE step will be removed from the titania memristor fabrication process.

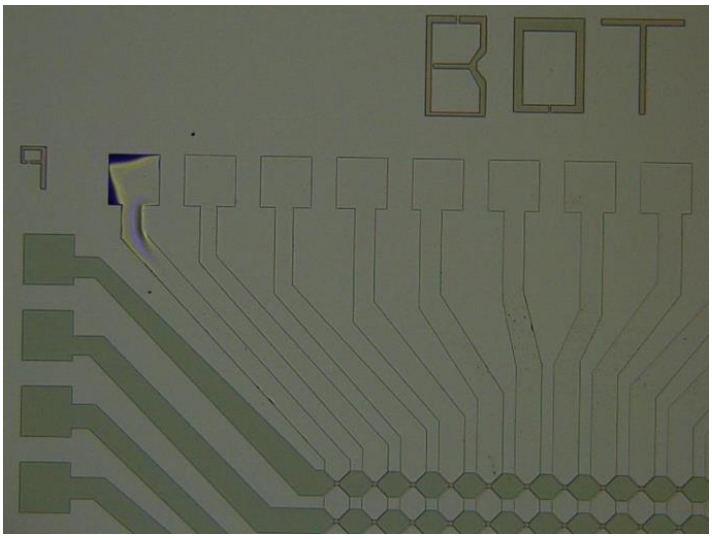

Figure 4.111: Fifteenth generation memristors, top electrode lithography.

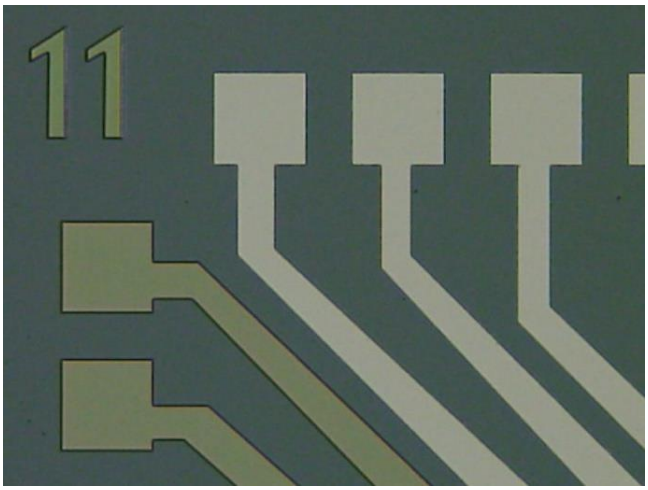

Figure 4.112: Fifteenth generation hafnia memristors, post ion mill.

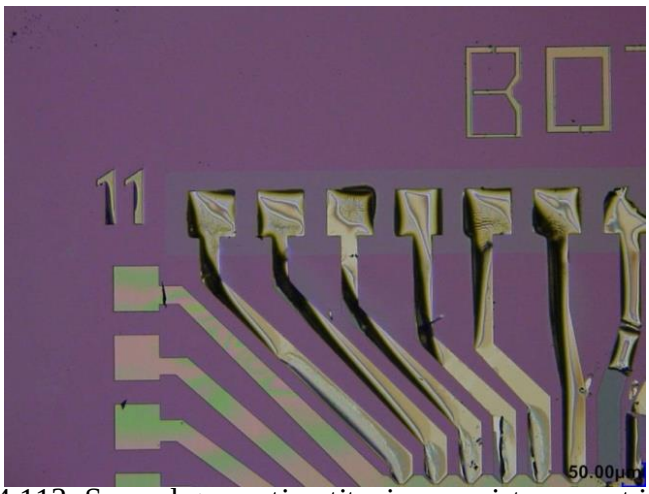

Figure 4.113: Second generation titania memristors, post ion mill.
Delamination clearly visible on bottom traces.

The hafnia memristors were then characterized electrically using the Agilent B1500A Semiconductor parameter analyzer at CINT. The results show a strong reset and clear hysteresis characteristics when the devices were cycled on and off as can be seen in Figures 4.114 and 4.115.

A change request was submitted from the postdoc for the total surface area of the memristors to be increased from 2 mm^2 to 3 mm^2 to reduce the total wire length on the wire bonds to ensure that the wires would be less likely to break while packaging the devices. It was also requested that the contact pads were expanded to 200 microns as well. The mask was then extensively revised for the sixteenth generation to accommodate this technical need.

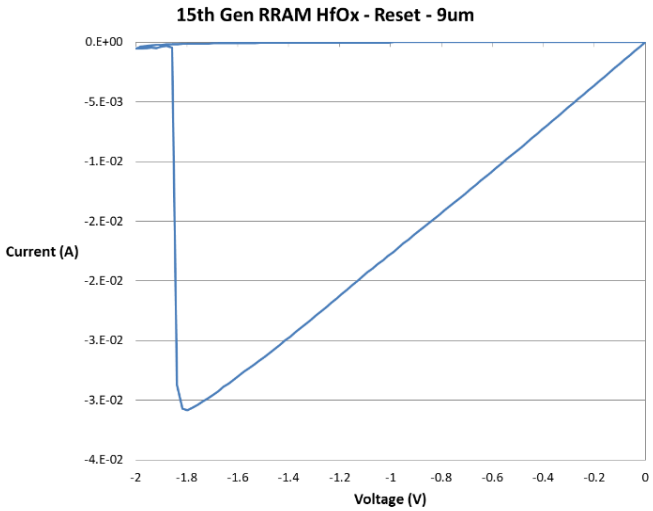

Figure 4.114: Fifteenth generation hafnia memristor, reset.

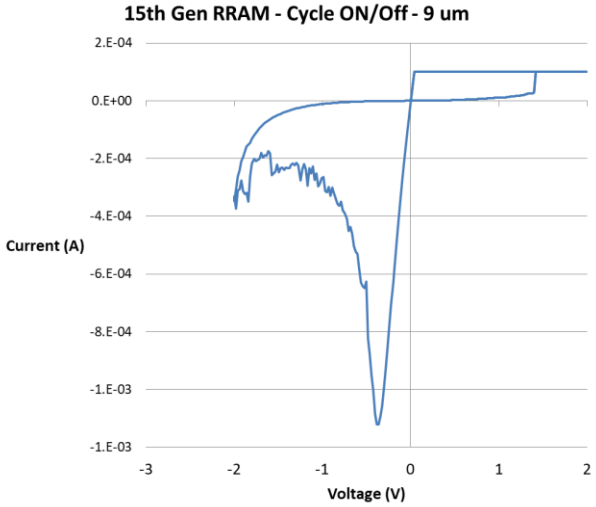

Figure 4.115: Fifteenth generation hafnia memristor, full cycle.

4.17 Sixteenth Generation Memristors

The mask was modified to expand the footprint of the diced devices along with the contact pads as can be seen in Figures 4.116 and 4.117.

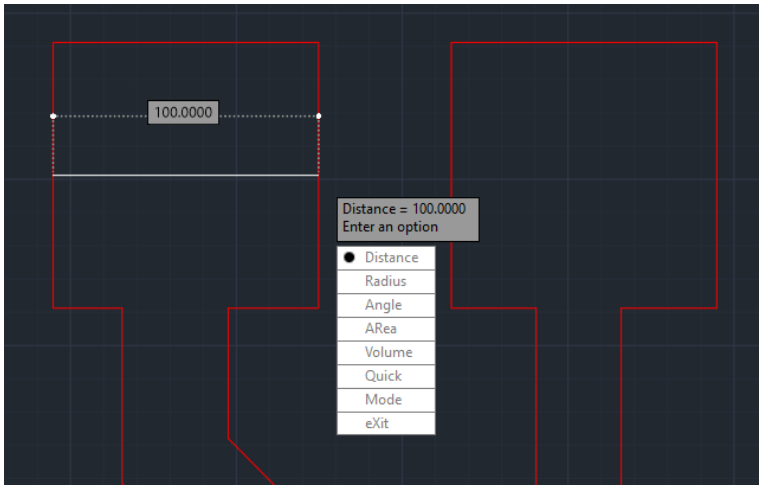

Figure 4.116: Earlier generation memristor mask, pad size is 100 microns and the gap between pads was 50 microns.

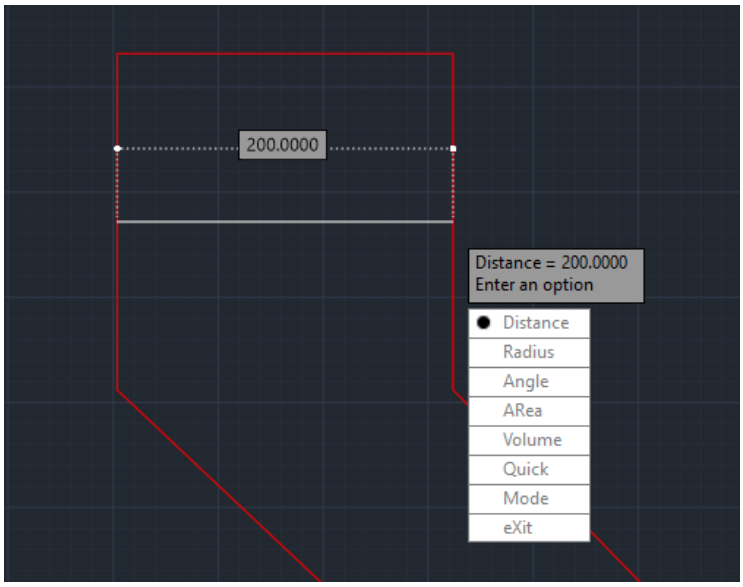

Figure 4.117: Sixteenth generation memristor mask, pad size increased to 200 microns and spacing between pads increased to <200 microns.

Due to the overall increase of the mask footprint from 100 mm^2 to 225 mm^2, the process was converted to using 2 in^2 wafers per device array rather than dicing a 4 in^2 wafer into 2 cm^2 squares. The samples were then prepared following the prior outlined steps for the fourteenth and fifteenth generations as can be seen in Figures 4.118 and 4.119.

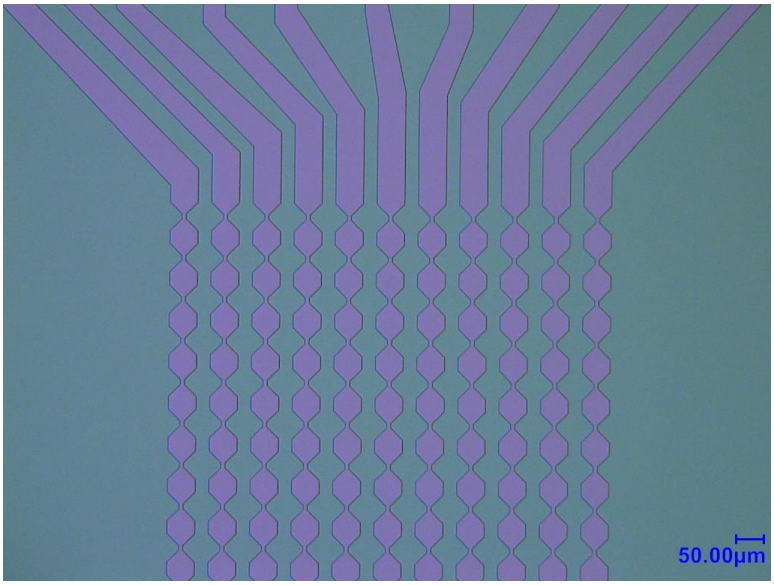

Figure 4.118: Sixteenth generation memristor, bottom electrode lithography.

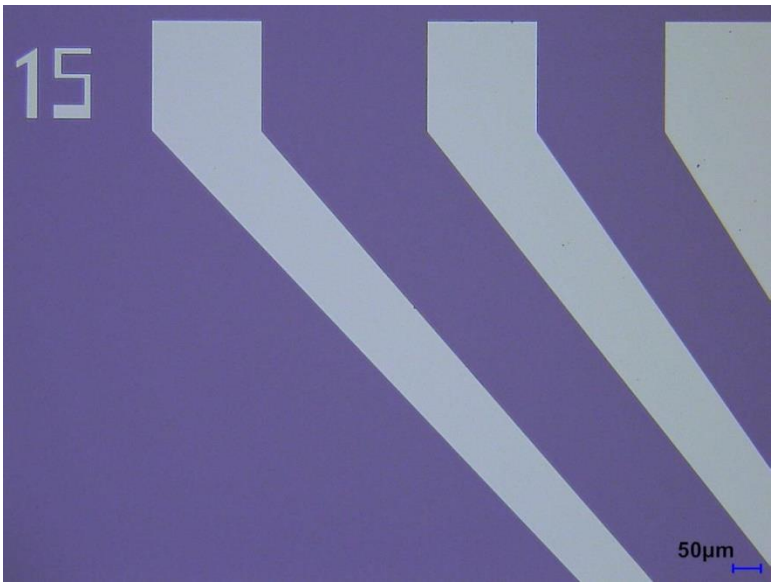

Figure 4.119: Sixteenth generation memristor, bottom electrode post lift off.

The samples were then split into two lots. Group A received a 2/5 nm alumina/hafnia oxide stack, Group B received a bilayer oxide laminate of 2/5 nm alumina/hafnia grown twice for a total stack height of 4 nm alumina and 10 nm hafnia. This design was revisited to determine if it would offer greater reliability and duration as the 2/5 nm hafnia memristors have had low yield rates thus far.

The samples were then given a top metal coat of 10 nm titanium and 300 nm platinum and spin coated at 5000 rpm with AZ5214 photoresist as shown in Figure 4.120.

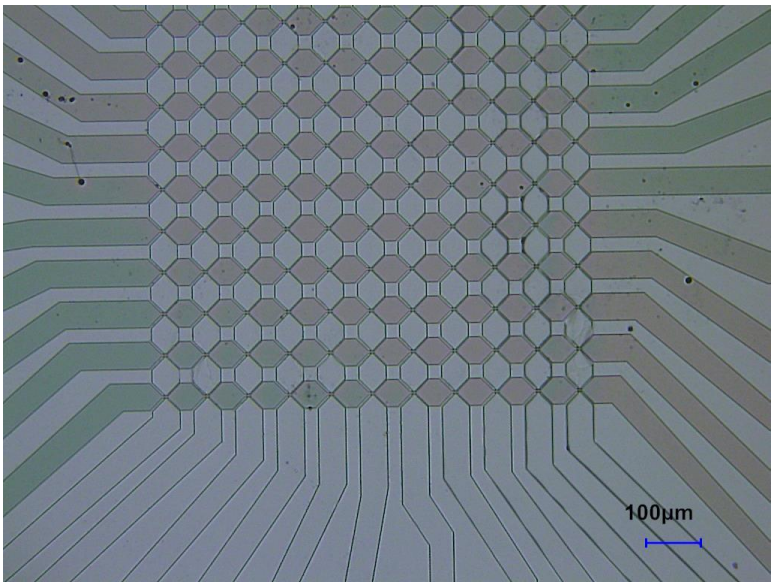

Figure 4.120: Sixteenth generation memristor, bottom electrode post lift off.

The samples were then bonded to carrier wafers with photoresist and placed in the ion mill for 5 minutes and 15 seconds. One notable problem that came up during the milling process is the total area of the device arrays are slightly larger than the beam area, leading to some parts of the samples not being fully milled as can be seen in Figure 4.121.

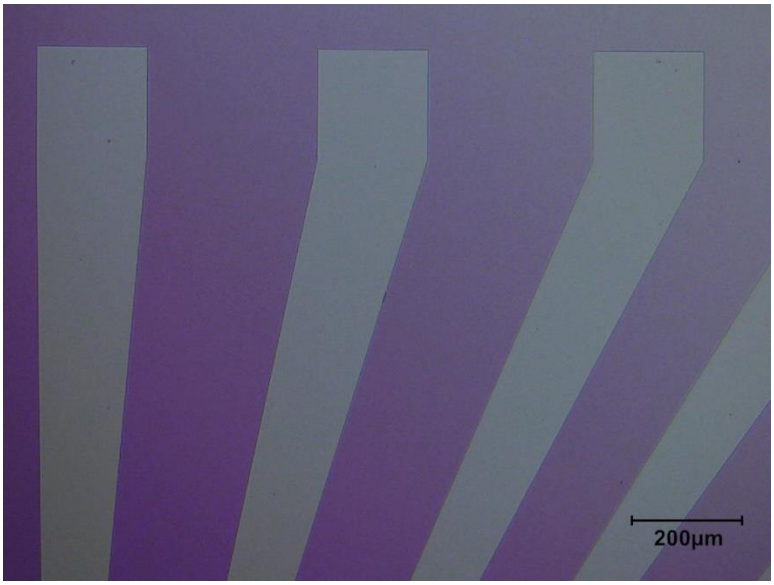

Figure 4.121: Sixteenth generation memristor, post ion mill. The metal in the top right corner is not fully milled as it lay at the outer radius of the ion beam.

The samples were then characterized before dicing, after dicing and then after packaging as problems had been observed with devices properly cycling after being packaged and it was uncertain as to where the fault in these steps was that led to total electrical failure of the memristors. Electrical characterization data was then collected at each stage as can be seen in Figures 4.122 through 4.125.

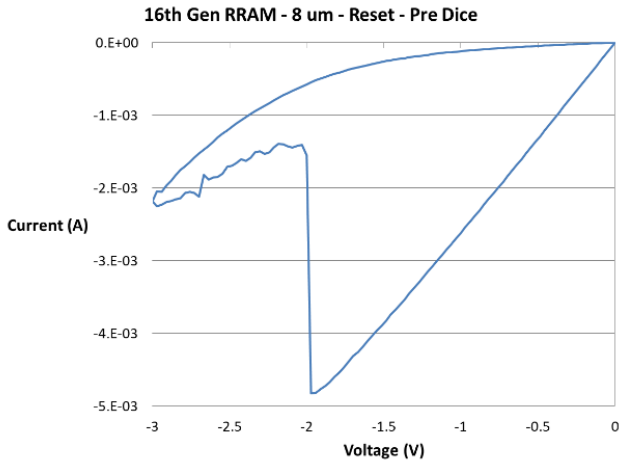

Figure 4.122: Sixteenth generation memristor. Reset taken before dicing.

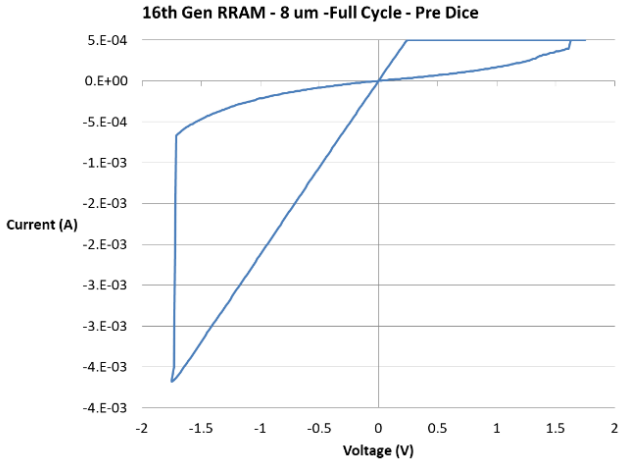

Figure 4.123: Sixteenth generation memristor. Full cycle taken before dicing.

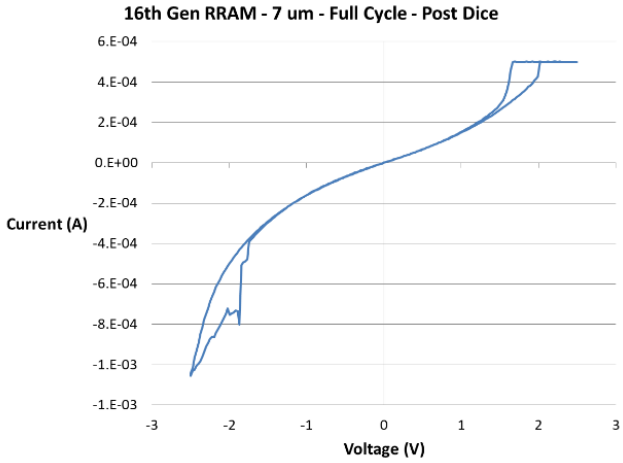

Figure 4.124: Sixteenth generation memristor. Full cycle taken after dicing.

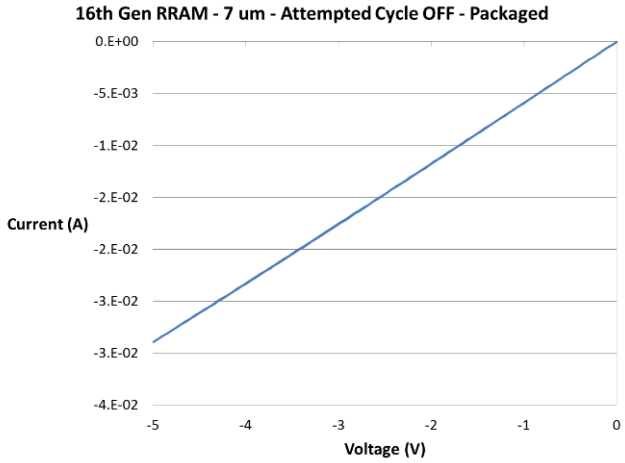

Figure 4.125: Sixteenth generation memristor.
Attempted cycle to OFF state after packaging the array.

Out of the 7 micron array, post packaging there were approximately 2 out of 13 devices that successfully reset and cycled which is a yield rate of approximately 15%. This is unacceptable as two out of three devices tested on the 7 micron array successfully reset and cycled after dicing and before packaging, which was a yield rate of 65%. It also came to light that the earlier packaged devices were exhibiting similar behavior.

Further testing was conducted on the diced and unpackaged individual arrays of the 16th generation arrays, as well as on the packaged devices from the 14th and 15th generations. The packaged devices from the 14th and 15th generations were found to all be electrically shorted as can be seen from Figures 4.126 and 4.127.

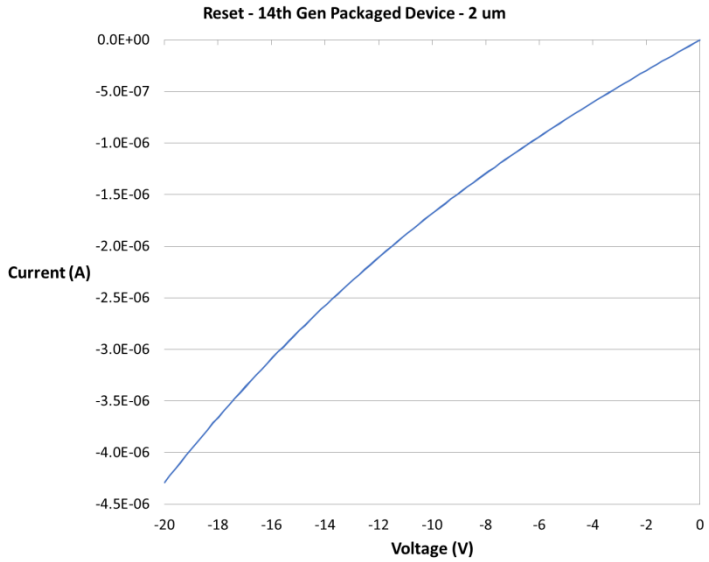

Figure 4.126: Fourteenth generation packaged memristor.
Did not reset at -20 volts.

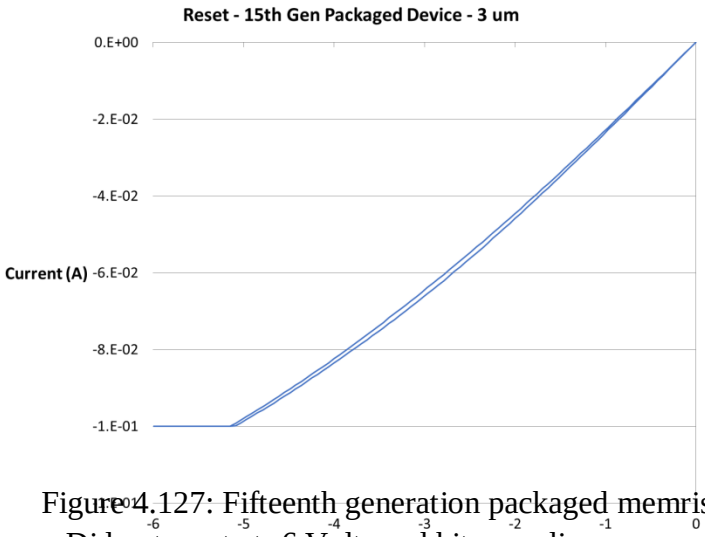

Figure 4.127: Fifteenth generation packaged memristor.
Did not reset at -6 Volts and hit compliance current.

The diced 16th generation memristors were working when initially tested, but retesting the same array at a later date would reveal electrically shorted behavior as shown in Figures 4.128 and 4.129. This was inexplicable until additional research revealed that copper ions are capable of diffusing through silicon and silicon dioxide at room temperature and moderate voltage bias [Caucoris 1999]. The reason this mattered is the chuck plate where the samples were placed for probing, is grounded with copper as shown in Figure 4.130.

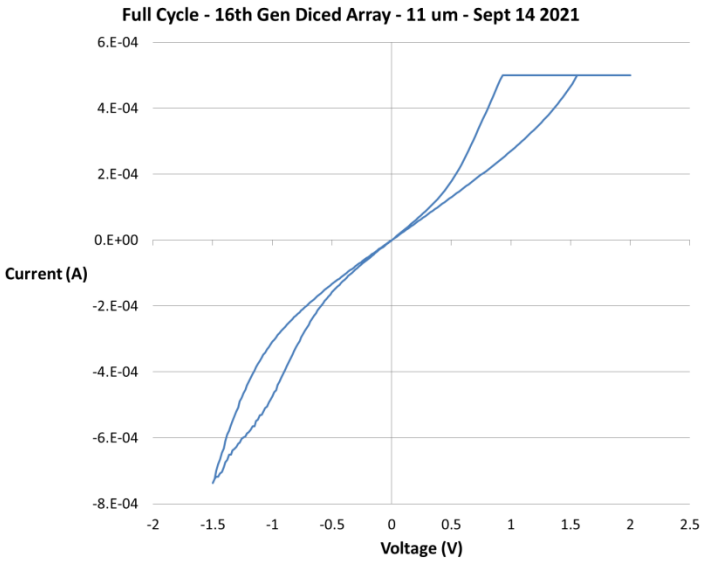

Figure 4.128: Sixteenth generation diced memristor, tested September 14th 2021.
Good signal, strong hysteresis.

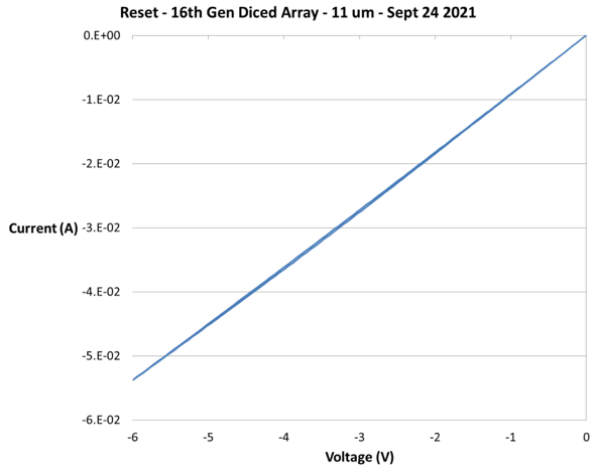

Figure 4.129: Sixteenth generation diced memristor, tested September 24th 2021. Array now electrically shorted.

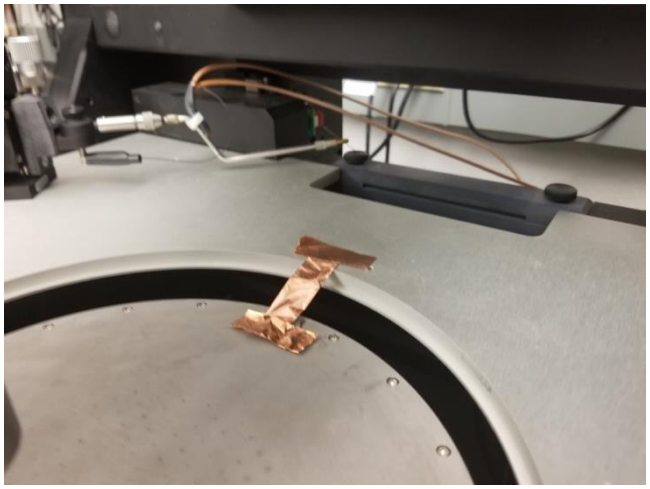

Figure 4.130: Copper tape used to ground chuck plate.

A hypothesis was then formulated that the chuck plate was contaminated with copper ions and as the devices were subjected to voltage bias, the copper would then diffuse through the samples. The process was not an immediate one, but if the devices were tested at a later date they would be all shorted as copper is an excellent conductor and has a documented history of shorting transistor-based logic gates as well as other dielectrics [Caucoris 1999].

An experiment was then conducted to check this hypothesis using two previously tested die, where the whisker probes were connected to two of the ground traces in parallel. Under ordinary conditions, the ground traces are not connected electrically and so should read as an open circuit. However, if the die were irreversibly contaminated with ionic copper, they would not read as open. As can be seen from Figures 4.131 and 4.132, this hypothesis is a potential explanation for the problems observed. However, further research and experiments should be conducted in the future to verify its' validity. The simplest future test would be to characterize the memristors while isolating the arrays from the chuck plate, wait approximately one week and then attempt to re-characterize the working devices to assess any changes to their functional state.

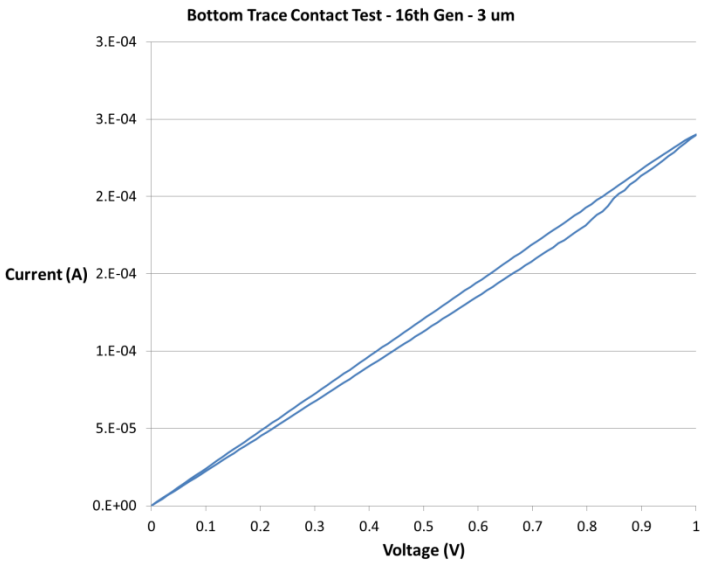

Figure 4.131: First bottom trace test, reads as a conductor rather than an open circuit.

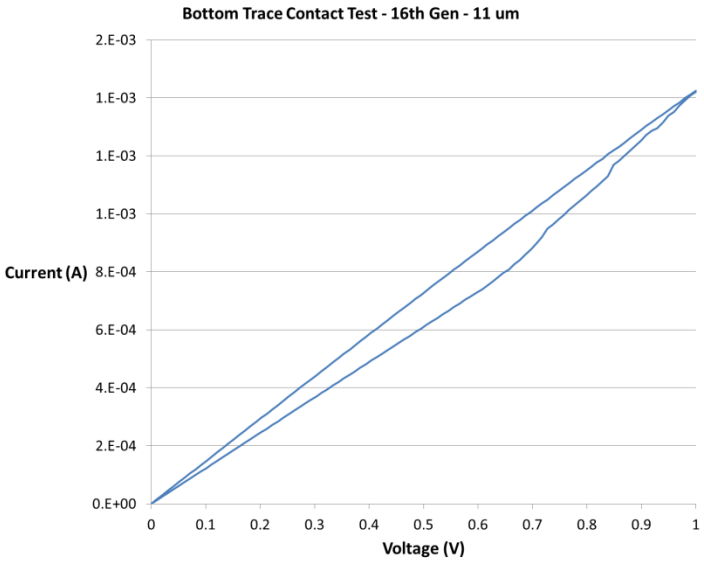

Figure 4.132: Second bottom trace test.

Chapter 5

Conclusions

Memristors have the potential to be used in overcoming different technical problems as discussed in Chapter One, however there are many challenges involved in first fabricating working memristors and then improving both yield and reliability. The processes developed in the course of thesis offer lines of future inquiry for producing memristors that can be refined to greater levels of quality and reliability.

I learned a great deal about electronic fabrication in the process of this thesis, both some of the common and more obscure pitfalls in semiconductor fabrication work came up and were overcome through careful application of scientific process as well as designing changes in an iterative fashion. It is unfortunate that the theoretical work that was expected to take place in the course of this research failed to occur, mostly due to unanticipated labor shortages, but the empirical data and its' value for future research remain.

Appendix A
Hafnia Memristor Fabrication Process Sheet

Step #:	Process: HfOx ReRAM Photolithography Process	Tool:	
PREPARATION			
1	**Clean** - Acetone spray, Methanol spray, isopropyl alcohol rinse. N2 spray until dry (~60 sec).	SOLV 2	
2	**AZ 4330 Photoresist spin** - 3000 rpm for 30 seconds (Recipe 3). Soft bake at 90 °C, 60 seconds.	SPIN 1	
3	**Dice** - 2 cm x 2 cm samples from wafer	DICE 1	
4	**Swab** - lightly around edges to remove any particles from cleaving process with isopropyl alcohol.	N/A	
5	**Clean** - Acetone 5 min, Methanol 5 min, Isopropyl Alcohol 5 min in ultrasonic bath, then deionized water rinse. Dehydration bake 120°C for 10 min.	SOLV 2	
6	**Inspect** - Check sample under optical microscope using backlight illumination to verify no surface contamination exists from dicing process. ***If*** contamination present - repeat cleaning process.	SCOPE	
7	**Store** -Diced samples stored in cleanroom locker until ready for contact litho **or** proceed to contact litho steps.		
LITHO BOTTOM ELECTRODE MASK, ETCH AND METAL DEPOSITION			
8	**Clean** - Acetone spray, Methanol spray, isopropyl alcohol rinse. N2 spray until dry (~60 sec).	SOLV 2	
9	**Strip** - Oxygen plasma for 10 minutes.	LOLA	
10	**AZ 5214E Photoresist spin** - 5000 rpm for 30 seconds (Recipe 5).	SPIN 1	
11	**Bake** - Soft bake at 110 °C, 60 seconds.	HOT PLATE	

12	**Contactless Litho expose** - Postive Tone Mask: 10 x 10 mm. Exposure: 120 nJ at 405 nm wavelength	MLA 1	
13	**Contact Litho development** -MIF 300 developer 45s soak, DI Rinse to 13 M-Ohm, dry N2.	SOLV 3	
14	**Process inspection** - inspect sample under microscope to verify pattern has good resolution.	SCOPE	
15	**Plasmaline descum** - O2 100W, 1 torr, 3 minutes.	ASH	
16	**Ti/Pt Deposition** - load sample into EG and deposit 10 nm Ti and 100 nm Pt via electron beam evap.	EG 1,2,3	
17	**PG Soak** - Soak in Remover PG for 24 hours. Ultrasonic bath for 60 second intervals until resist and excess metal is fully removed	SOLV 1	
18	**Liftoff** - Use Acetone N2 gun to clean out any lingering metal not removed via ultrasonic bath. ~ 25 PSI to avoid removing actual metal pattern.	SOLV 1	
19	**Liftoff** - Finish cleaning sample with methanol and isopropyl alcohol (IPA), dry with N2 gun ~ 30 PSI	SOLV 1	
18	**Inspect** - Check sample under optical microscope to verify the liftoff and that the pattern is well resolved.	SCOPE	
19	***Store*** -Diced samples stored in cleanroom locker until ready for ALD or proceed to ALD steps.	LOCKER	
ReRAM Layer Deposition & Anneal			
20	**Clean** - Acetone spray, Methanol spray, isopropyl alcohol rinse. N2 spray until dry (~60 sec).	SOLV 2	
21	**Oxygen Plasma Strip** - 10 minute O2 plasma strip	LOLA	
22	**Oxygen Plasma Chamber Clean** - 10 minute O2 plasma strip of ALD chamber.	ALD	

23	**Chamber Precondition** - Run ALD system with no samples using AlOx/HfOx Recipe	ALD	
24	**Oxide Deposition** - load sample into ALD and deposit 25 angstroms (2.5 nm) AlOx via atomic layer deposition. (10 nm) HfOx via atomic layer deposition.	ALD	
25	**Oxygen Plasma Strip** - 10 minute O2 plasma strip	LOLA	
26	**Anneal** - 30 minute anneal @ 400 C in forming gas mix. (Recipe Name: FA_T_400_30_min_WH)	RTA	
ION MILL TOP ELECTRODE MASK			
27	**Clean** - Acetone spray, Methanol spray, isopropyl alcohol rinse. N2 spray until dry (~60 sec).	SOLV 2	
28	**Strip** - Oxygen plasma for 10 minutes.	LOLA	
28	**HMDS Photoresist spin** - 3000 rpm for 30 seconds.	SPIN 1	
29	**Prebake** - 90°C for 60s.	HOT PLATE	
30	**Ti/Pt Deposition** - load sample into EG and deposit 10 nm Ti and 200 nm Pt via electron beam evap.	EG 1,2,3	
31	**AZ 5214 Photoresist spin** - 5000 rpm for 30 seconds. - Recipe 5	SPIN 1	
32	**Prebake** - 110°C for 60s.	HOT PLATE	
33	**Contactless Litho expose** - Postive Tone Inverted Mask: 10 x 10 mm. Exposure time:: 6 s, 120 nJ at 405 nm wavelength	MLA 1	
34	**Contact Litho development** -MIF developer 45s soak , DI Rinse to 13 M-Ohm, dry N2.	SOLV 3	
35	**Process inspection** - inspect sample under microscope, validating top electrode pattern is perpendicular to bottom electrode.	SCOPE	

36	**Plasmaline descum** - O2 100W, 1 torr, 3 minutes.	ASH	
37	**AZ 5214 Photoresist spin on Carrier Wafer** - 3000 rpm for 30 seconds. - Recipe 3	SPIN 1	
38	**Bond Sample to Carrier Wafer** -Add one small drop of AZ5214 to the center of the carrier wafer. Place sample on top of drop of resist.	SPIN 1	
39	**Carrier Wafer to Sample Bonding** - Soft Bake 110°C for 3 minutes.	HOT PLATE	
40	**Ion Mill** - 2.5 minute etch on the Ion Mill, set for Pt & Ti etch. Inspect after first run and if there is still excess metal, run the etch cycle a **second** time.	MILL	
41	**Process inspection** - inspect sample using under optical microscope to verify success of milling process.	SCOPE	
42	**PG Soak** - Soak in Remover PG for 24 hours.	SOLV 1	
43	**Clean** - Acetone spray, Methanol spray, isopropyl alcohol rinse. N2 spray until dry (~60 sec).	SOLV 1	
44	**Strip** - Oxygen plasma for 10 minutes.	LOLA	
45	**Process inspection** - inspect sample using under optical microscope to verify that all photo resist has been removed.	SOLV 1	

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