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Etched-and-Regrown Diodes on M-Plane GaN for Next Generation Power Electronic Devices

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ETCHED AND REGROWN DIODES
ON M-PLANE GAN
FOR NEXT GENERATION
POWER ELECTRONIC DEVICES

by

Name:
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Degrees:
B.S., Electrical Engineering, University of New Mexico, 2012
M.S., Electrical Engineering, University of New Mexico, 2014

DISSERTATION

Submitted in Partial Fulfillment of the
Requirements for the Degree of

Doctor of Philosophy
Engineering

The University of New Mexico
Albuquerque, New Mexico

May 2021

DEDICATION

This dissertation is dedicated to my family and friends: My mother, for pushing me to be the best I can, and giving me the example, motivation, and encouragement to pursue my education. My father, for telling me to always keep "my eye on the prize." My sister, for her support and encouragement. My many friends, who have helped me in various ways to encourage and support me. To family and friends who are no longer with us, I hope to do you all proud.

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Etched-and-regrown diodes on *m*-plane GaN for next generation power electronic devices

by

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ABSTRACT

Demand for next-generation power electronic devices is driven by continually evolving requirements of power systems. Devices utilizing III-nitride materials (GaN) and vertical selective-area doped architectures are advantageous due to their wide-bandgap, thermal management, small form-factor, and current handling.

Such devices incorporate junctions at multiple crystalline planes. Thus, effects of impurity contamination and etch damage are investigated on the *m*-plane (10-10) of GaN. Impurites (Si, O, and C) are shown to reduce blocking voltage (~ 10^2 ×) and increase forward leakage current (~ 10^4 ×) in regrown versus continuously-grown *p*-*n* diodes. Elevated deep level defects at E_c – 1.9, 2.9, and 3.3 eV are identified with increased reverse leakage (~ 10^3 ×) in etch-and-regrown versus continuously-grown Schottky diodes. Post-dry-etch methods are used to reduce defects and reverse current leakage (~ 10 – 10^3 ×). Additionally, leakage current mechanisms are investigated via an RF method to extract dynamic parameters of etched-and-regrown *p*-*n* diodes.

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Chapter 1 Introduction

The interest in next generation power electronics is driven by the demand of evolving power systems. It has been estimated that 30% of energy passes through power electronics today with a projection of 80% passing through power electronics by 2030 [1]. The power systems impacted by this demand span across power generation, power transmission, and power storage. Many applications, to name a few, are power converters and inverters for power generation, power flow controllers for power transmission, variable frequency drives for motor drives, AC-DC converters for power supplies, and battery charging and traction drive inverters for electric automobiles [2]–[9]. Advances in power electronics for these systems and applications promise energy efficiency gains which may include reduction in electricity consumption, reduction in the cost of electrification of automobiles, reduced losses and cost of renewable energy solutions, and increased efficiency of the expanding electric transmission networks [10]–[13]. Thus, low-loss power semiconductor devices are required in order to achieve high power conversion efficiency in these systems and applications.

Limitations of current electronic devices must be considered when developing the next generation of semiconductor power electronics. Today's semiconductor power technology is based on silicon (Si) devices such as metal oxide semiconductor field-effect transistor (MOSFETs), insulated-gate bipolar transistors (IGBTs), and thyristors [14]. Silicon power semiconductor devices have several important limitations such as high losses, low-switching frequency, and poor temperature performance [15]–[17]. Therefore, consideration of the semiconductor material system and device design must be a critical

factor in the next generation of development and design. We will develop within this chapter a motivation for the change to GaN (Gallium Nitride) based systems with an emphasis on vertical power device structures. Within this motivation will arise several benefits and challenges towards achieving significant figure-of-merit performance metrics with the intention to surpass Si based power electronic devices.

The primarily focus of this dissertation is solving challenges of incorporating vertical power electronic devices on GaN. However, we first will take into consideration the motivation of device architecture, and the motivation for perusing GaN as a suitable material for investigation. Therefore, the chapter will begin with a brief discussion of the fundamental concepts of device architecture, followed by the group III-nitride material system, emphasizing the nonpolar crystal orientation and its challenges. Lastly, the chapter will provide a review of existing design considerations for *m*-plane *p-n* diodes explaining the motivation behind our design.

1.1 Device Architecture

The device architecture plays a critical role in the performance of power electronic devices. We classify two different types of designs: lateral and vertical architectures. The architecture is defined by the channel or junction orientation in which current flows with respect to the substrate. Figure 1 shows two examples of a lateral electron flow in a GaN based Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and also a High Electron Mobility Transistor (HEMT) device. With regard to the MOSFET in the forward active regime, current flows in the opposite direction of electron flow from source to drain though an inversion layer called a channel due to the voltage between the gate and bulk semiconductor. The current is tightly confined within this layer which is often only a

few microns long and a few microns wide, for power applications [18]. This tight confinement and placement of the source and drain contacts restricts the current handling of such devices which in turn increases forward on-resistance. Also, in the reverse regime, current is restricted due to an induced depletion region between source and drain. However, an electric field is present between source and drain which is limited to the length between source and drain. This may lead to increased electric filed induced breakdown at high voltages due to the geometry of the device [19]. In the case of the HEMT device, current flows in the opposite direction of electron flow from source to drain through a two-dimensional electron gas (2DEG) formed between a heterojunction. Again, the electrons are tightly confined within the 2DEG of the HEMT in the forward regime which again leads to current handling restrictions and larger on-resistances [20]. Also the induced electric field confined between source and drain in the reverse regime limits high blocking voltages [21].

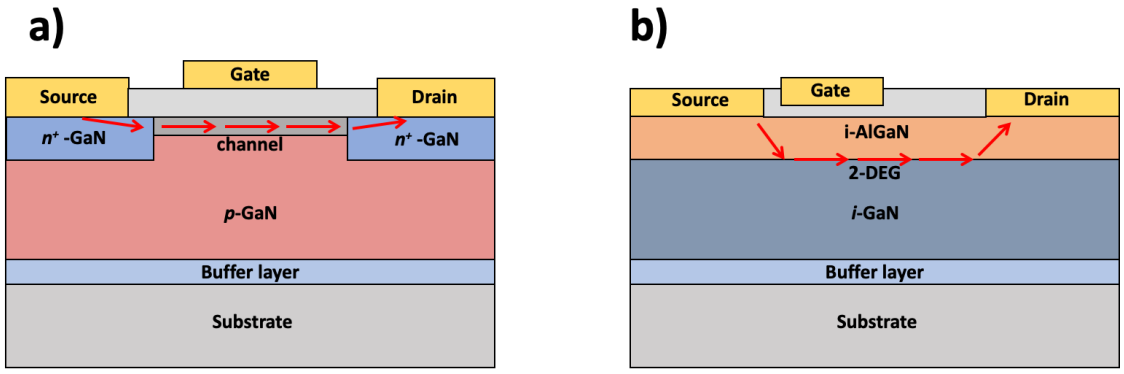

Figure 1.1. Lateral power electronic devices: a) Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) showing direction of electron flow through the inversion layer channel. b) High Electron Mobility Transistor (HEMT) Device showing the direction of electron flow in the 2DEG layer between AlGaN and GaN.

It is important to look at the limitations of these lateral structures in order to understand the electrical current and electric fields present within these devices in the forward and reverse regimes. Of primary concern is the ability of these structures to

maintain high-blocking voltages while maintaining low on-resistances. From our quick analysis of these two examples of lateral device, we can see some disadvantages with these types of geometries. Therefore, a motivation to pursue vertical geometries will be presented as follows.

The basic classification of vertical power devices is the direction of current flow in the forward regime and the direction of the critical electric field in the reverse regime [22]. Figure 1.2 shows a cross-sectional schematic of a vertical junction field-effect transistor (JFET) device with the flow of electrons indicated. The opposite flow of electrons from source to drain constitutes the forward regime current. The current is not restricted in such devices by short channels or tight bends within the device, leading to an increase in current handling with low on-resistances [23]. In the reverse bias, the depletion region between source and drain in a JFET is limited by the electric field between the two. By using a vertical geometry, the critical electrical field may be increased due to the large distance from source to drain which increases the maximum breakdown voltage [24]. An additional benefit is the reduction of current collapse which, in the presence of large electric fields, results in the transfer of hot carriers from the conducting channel to an adjacent region of devices such as JFETs [25].

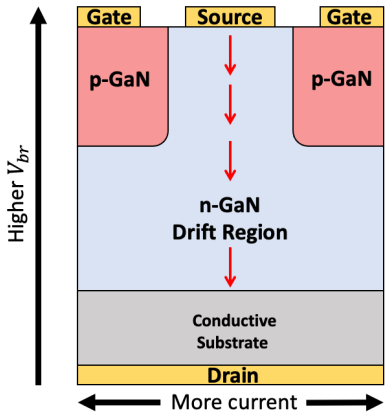

Figure 1.2. Vertical power electronic devices: Junction Field-Effect Transistor (JFET) showing direction of electron flow from source to drain

The vertical geometry allows for small-form factor devices, as the critical geometric distances are vertical as opposed to lateral [26]. An additional benefit of vertical geometries comes about with low parasitic inductance, which is attributed to the magnetic fields induced by current flow in opposite directions on the same plane which is prevalent in lateral geometries [27]. Therefore, we can quickly see the advantages of vertical designs over lateral designs due to the increase in breakdown voltage V_{br}, low on-resistance, increased current handling, suppressed current collapse, low parasitic inductance, and small form factor.

1.2 III-Nitride Material System

Devices on wide bandgap materials are continuing to be developed to achieve higher efficiency for power electronic systems and applications [28]. Table 1 compares several metrics of different wide bandgap (WBG) materials along with Si which are important to the development of power electronic devices [10], [29]–[31] . Three critical aspects for power electronics are: 1) low-loss high voltage operation, 2) high speed operation, and 3) low degradation at high temperature. The low bandgap (1.1 eV) and low breakdown electric field of Si requires devices to have large thicknesses which in turn lead to high resistances and conduction loss [32]. Thus, power electronics on Si require large form factors in order to keep conduction loss low. However, this increases the associated capacitances which produce large peak currents and losses at high frequencies. Also, the low saturation velocity and long carrier lifetimes reduce the frequency limits of Si power electronics [33], [34]. Another downfall of Si is the low bandgap which contributes to a

high intrinsic carrier concentration, which results in high leakage currents at elevated temperatures.

Table 1.1 Material properties of select (Si, GaN, 4H-SiC, and Diamond) power semiconductor materials. Data from Refs. [10], [29]–[31]

property	unit	GaN	Si	4H-SiC	Diamond
Band Gap	Eg (eV)	**3.39**	1.1	3.26	5.45
Intrinsic Concentration	n_i (cm-3)	**1.9×10^{-10}**	1.5×10^{10}	8.2×10^{-9}	1.6×10^{-27}
Electron Mobility (low)	μ_n (cm2/V s)	**500**	1350	700	1900
Electron Mobility (high)	μ_n (cm2/V s)	**2000**	1450	950	4000
Electron Saturation Velocity	v_{sat} (10^7cm/s)	**2.5**	1	2	2.7
Breakdown Electric Field	E_{br} (MV/cm)	**3.5-3.75**	0.3	2	5.6
Baliga Figure-Of-Merit	BFOM (GW/cm^2)	**67-83**	0.004	6.5	355
Thermal Conductivity	K (W/cm °K)	**2.3**	1.5	4.9	20

One key metric for materials for power electronics is known at the Baliga Figure-of-Merit (BFOM) [35]. The BFOM relates the reverse blocking voltage with the forward on resistance. The derivation of the BFOM is found in Appendix A. The BFOM is shown in equation 1.1. By inserting the relationship between the critical electric field (E_C) and on resistance (R_{on}) we obtain Equation 1.2.

$$\mathrm{BFOM} = \frac{V_{BR}^2}{R_{on}} \tag{1.1}$$

$$\mathrm{BFOM} = \frac{\varepsilon_s \mu_n E_c^3}{4} \tag{1.2}$$

By comparing the BFOM among the materials in Table 1 it is apparent that GaN stands out among Si and SiC. However, diamond exhibits the largest BFOM among the materials compared. However, implementing diamond into power electronics devices has many challenges such a cost of manufacturing, material growth, and device fabrication [36]. Much progress on wide bandgap-based power devices developed on SiC and GaN has been made in the past decade. Some examples include 1200 V SiC devices[37] and 600 V GaN[38] devices which have been qualified and are commercially available. However, SiC and GaN device technology remains relatively immature relative to Si, but they remain as commercially viable materials for power electronic devices[39]. Thus, cost for an equivalent functional performance remains a major barrier to the widespread adoption of WBG devices, despite opportunities for superior performance (including reductions in system costs) [40]. WBG devices will have to approach functional cost parity with Si power devices in order to gain widespread adoption. Therefore, devices on wide bandgap materials must meet or exceed the cost effectiveness of Si based devices. Nevertheless, the performance benefits from switching to WBG devices is justification for the investigation and development of next generation power electronics.

The benefits of utilizing GaN are in that the material inherently possesses distinct advantages over Si and SiC. The large breakdown electric field and high electron mobility yield a substantial BFOM over both Si and SiC [41] simultaneously allowing for low-loss, high voltage operation, and high-speed operation. The larger thermal conductivity coupled with a low intrinsic carrier concentration allow GaN to mitigate excess leakage current at much higher temperatures than Si [42]. Thus, investigation of

GaN as a suitable material system is a continuing effort for next generation power electronics.

1.3 Selectively doped *p-n* junctions

The complex vertical designs of devices such as junction field effect transistors (JFETs), ex. in Figure 1.1, and current aperture vertical electron transistors (CAVETs) typically require selectively doped regions in their architecture [43]–[45]. Therefore, to investigate and develop selectively doped regions we will consider the most basic selectively doped device which is the vertical selectively doped *p-n* diode device. A schematic of the vertical selectively doped *p-n* diode is shown in Figure 1.3. By considering this device we can more easily analyze and understand the challenges that arise through implementing selectively doped regions on more complex devices.

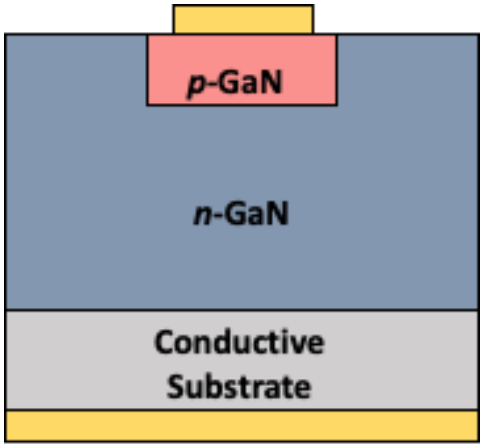

Figure 1.3. Vertical selectively doped *p-n* diode device.

The primary methods to implement selectively doped regions within a device architecture is by selective-area ion implantation and selective-area doping. We will look at both these methods and discuss the advantages and disadvantages of both, and

determine the most suitable method for implementing selective doping for the purpose of achieving the best selectively doped *p*-*n* diode.

Selective-area ion implantation uses heavy-ion bombardment on selective regions in order to implant dopant atoms within a semiconductor material [46]. A schematic representation of the selective-area ion implantation into GaN is represented if Figure 1.4. Heavy ions are selected for their appropriate donor/acceptor doping species. Ions are implanted based on the accelerating voltage, ion species, and material of implantation. A mask of dielectric or metal is used to shield the regions that are not desired to be exposed to ion bombardment. Ions penetrate to a desired depth within the semiconductor crystal in order to define the region of selective doping.

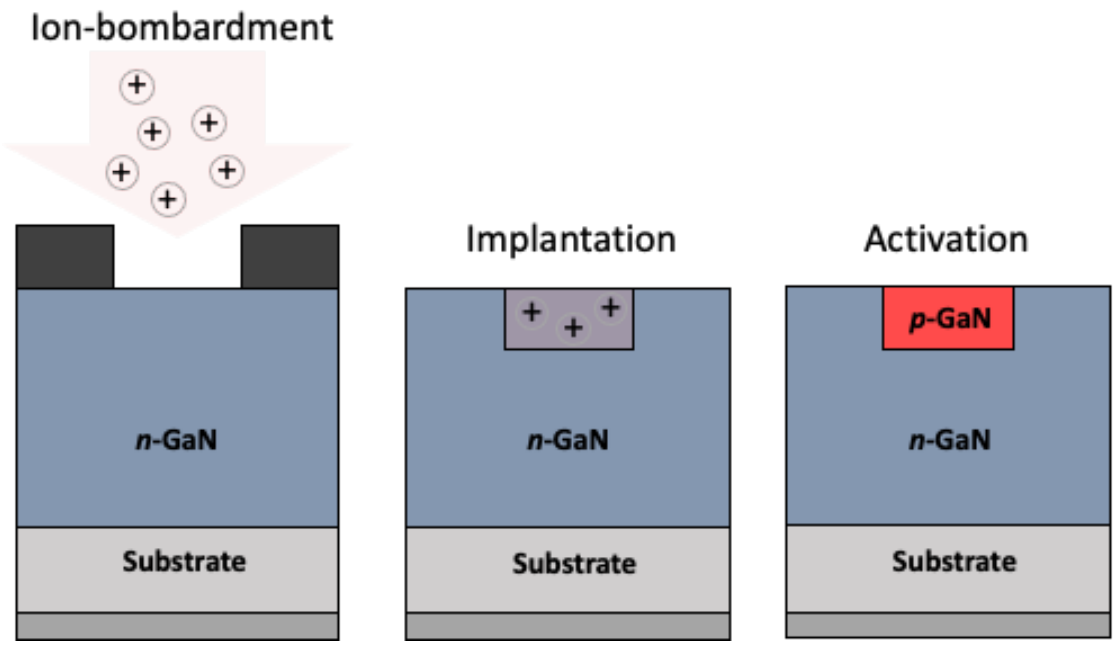

Figure 1.4. Selective-area ion implantation showing ion bombardment, implantation, and activation for a *p*-type region within bulk *n*-type GaN

An activation process such as multicycle rapid thermal annealing is used in order to activate the implanted ions [47]. This activation process may also remove implantation induced damage.

Many disadvantages of selective-area ion implantation arise specifically for the application of power electronics. As the selective-area region is defined by accelerating voltage, ion species, and implanted material, it may be difficult to achieve uniform doping profiles and abrupt junctions [48]. This is critical when junction power electronic devices are operated in the extreme reverse bias. Any doped region that is not uniform or non-abrupt may lead to elevated electric fields which may lead to early breakdown. Furthermore, a downfall of this method is that ion implantation causes damage within the lattice due to displacement of the semiconductor atoms. Thus, damage induced into the semiconductor crystal lattice by ion-implantation may lead to defect-assisted leakage current both in the forward and reverse regimes of operation [49]. Therefore, an alternative method to defining selective-doping must be investigated.

The second method to implement selective-doping is known as selective-area doping. This method requires the predefinition of the selective-area in order to grow the material of interest within this area [50]. Figure 1.5 shows a schematic representation of selective-area doping utilizing a dry etch process to define the selective-area within a bulk n-type GaN material before growth of p-type GaN within the defined region. The main difference between this method and selective-area ion implantation is the predefinition of the selective area. In most cases, the use of a dry etch process is required [51].

This definition of the selective-area regions can be quite reliable and uniform since commercial dry etching processes are robust for many materials including GaN. For GaN

in particular, the growth of p-type GaN and its activation process is quite widely known and standard in industry. Therefore, a selective doped region can be realized using this method without many of the disadvantages prone to selective-area ion implantation.

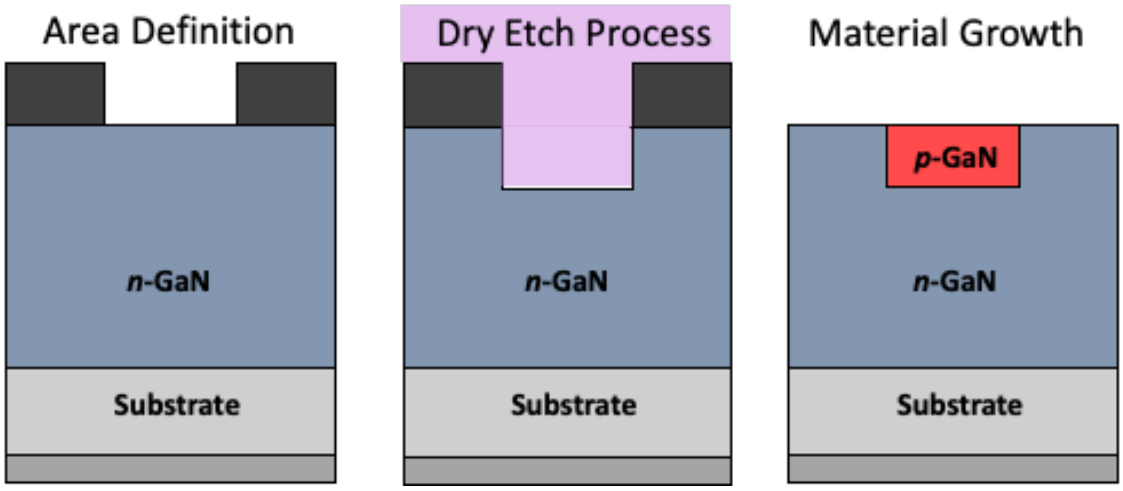

Figure 1.5. Selective-area doping showing area definition, dry-etch definition, and subsequent regrowth of *p*-type GaN within a bulk *n*-type GaN material

However, this method is prone to many challenges, and understanding them and mitigating these challenges is the motivation of this dissertation. The challenges that arise from the development of the selectively doped region using the selective-area doping technique are on-going for the implementation of power electronics on GaN. The primary challenges will be discussed in the subsequent section, and a move to planer diodes as a testbed for experimentation will follow.

1.4 Challenges of vertical selective area devices

As mentioned in the previous section, there arise some challenges with implementing selective-area doping for vertical power electronics on GaN. We will take

a quick look at the main challenges and will discuss and elaborate on them in the subsequent chapters of this dissertation. However, a quick look at these challenges will give some context for the motivation of our experimentation, methods, and analysis. Therefore, our primary focus will be concentrated on the two main challenges identified during the development of this work: 1) the effects of interfacial impurities at the regrown junctions, and 2) the effects of dry-etch enhanced damage.

The first challenge we will briefly look at is the effects of interfacial impurities at the regrown junction of selective-area doped devices. This challenge arises as a direct consequence of having to define the selective-area region by methods such as dry etching. In order to perform dry etching, the semiconductor device structure must be removed from the vacuum environment of the growth chamber into the outside environment to be taken to an area where the dry-etch process is to be conducted. Subsequent dry-etching is performed to define the selective-area region. Consequently, during and/or after this process, a sufficient amount of impurities (Si,O,C) accumulated at the selective-area interface. Subsequent regrowth of the selective-doped region was performed. The interfacial impurities are present at this junction between the two types of materials and affect the electrical characteristics of the device [52], [53]. A schematic representation is shown in figure 1.6 of the presence of interfacial impurities at the junctions of the selective-area doped region.

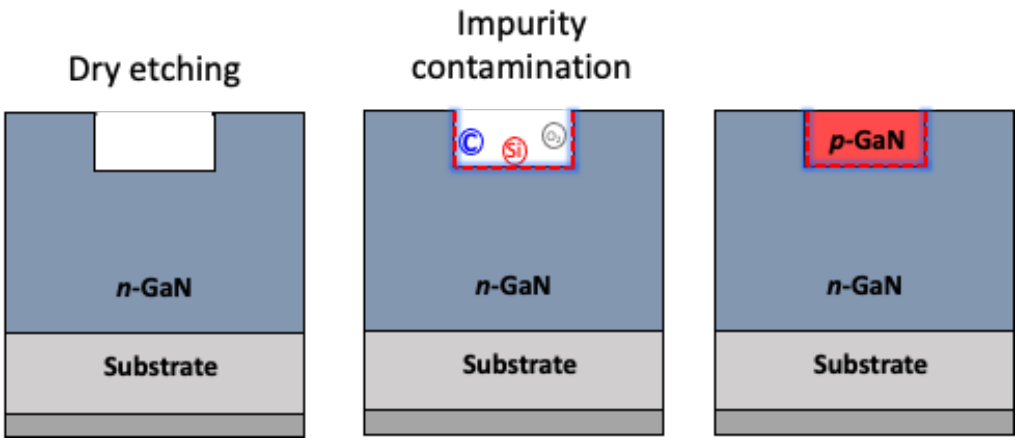

Figure 1.6. Schematic of the presence of interfacial impurities at the junctions of selective-area doped regions after the dry-etch process and after the regrowth process

The challenge presented by these interfacial impurities substantially affects the electrical performance of junctions, and much effort is required to mitigate these effects. A more detailed analysis of this challenge, its effects, and mitigation is presented in Chapter 2 of this dissertation. However, a basic principle of this challenge is presented which will guide us in our methodology and approach to understanding and solving this issue.

The second challenge we will give a brief look at is the effects of dry-etched enhanced damage on the underlying material and the subsequently regrown material. The damage enhanced by dry etching is schematically represented in Figure 1.7. During the dry-etch process, material is actively being removed by sputtering and chemical processes. These processes are sufficient to remove material, and subsequently damage the surface being etched. Since sputtering is a process involved, sub-surface damage is also present. Additionally, damage to the subsequent regrown material occurs due to a non-ideal surface for regrowth.

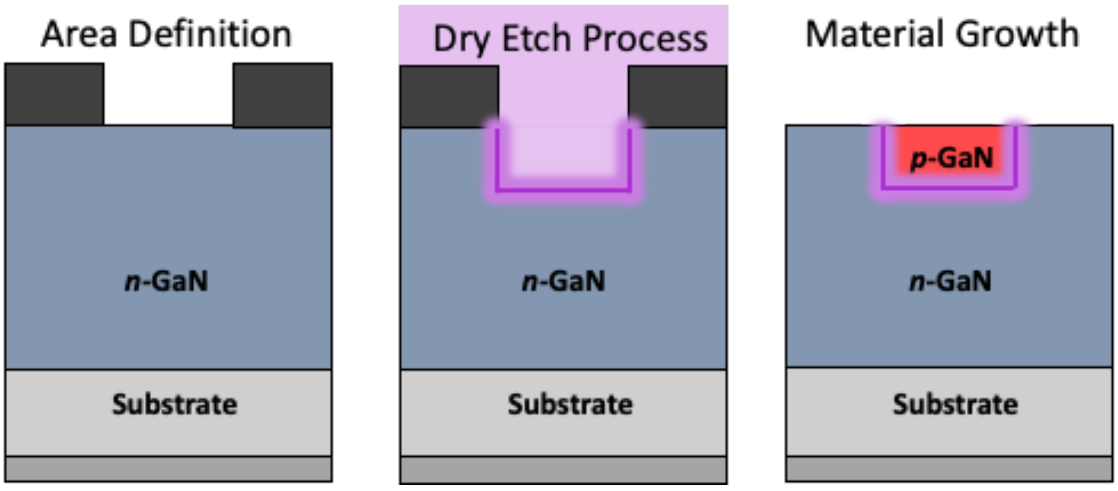

Figure 1.7. Schematic of the dry etched enhanced damage. Damage represented by purple line at the regrown interface: damage present at, below, and above the regrown interface

The challenges presented by the dry-etched enhanced damage below, at, and above the regrown interface affect the electrical performance of junctions [54]. A more detailed analysis of this challenge, its effects, and mitigation is presented in Chapter 3 of this dissertation. As with the challenge of interfacial impurities, a basic principle of this challenge is presented for a better understanding of the motivation of this work.

1.5 Planar *p-n* diodes

The motivation for selective-doped power electronic devices on GaN using selective-area doping and its challenges has been discussed previously. Thus, the fundamental device of interest which may be the launchpad into more complex device architectures is the vertical selective-area doped *p-n* junction. A schematic representation of the vertical selective-area doped *p-n* junction has been previously presented in Figure 1.3. Therefore, we must identify some performance metrics to achieve in the vertical selective-area doped *p-n* junction. If we can achieve these figure-of-merit metrics it will follow that more complex electronic devices can benefit from the understanding and analysis performed on this device. We can define some of these requirements for a selective-area doped *p-n*

junction in Table 2. The requirements for the selective-area doped *p-n* junction have been set by the funding agency, ARPA-E, under the project PNDIODES. The motivation of these requirements is to meet the challenges of the selective-area doped *p-n* junction and achieve these specific metrics for the continuing effort of investigating of wide bad-gap materials for use in high power electronic devices. These performance metrics are designed for implementation of a selective-area doped *p-n* junction on GaN, and thus reflect the essential limits of this material. However as will be discussed in the next section, these metrics will additionally motivate our implementation of planar vertical *p-n* diodes as well.

Table 1.2 Requirements for a selective-area dope d *p-n* junction

ARPA-E PNDIODES requirements	Value
Range of Controlled Selective Doping for Holes (*p*)	$1x10^{16} – 4x10^{17}$ cm^{-3}
Range of Controlled Selective Doping for Electrons (*n*)	$1x10^{16} – 1x10^{18}$ cm^{-3}
Breakdown Voltage	>= 1200 V
Leakage Current	<= $1x10^{-9}$ A (@ 600V)
Turn-on Voltage	2.6-3.4 V
Specific R_{DSON}	< 3 $m\Omega \cdot cm^2$
I_{on}/ I_{off} Ratio	> 10^{10}
Avalanche Capability	No parametric shift after repetitive avalanche testing
Surge Capability	>20A surge capability for 10μs pulse at 25°C

Nevertheless, these metrics represent the ultimate goal for GaN-based selectively doped vertical *p-n* diodes. The range of controlled selective doping for holes (*p*) and electrons (*n*) are within the ranges of $1x10^{16} – 4x10^{17}$ cm^{-3} and $1x10^{16} – 1x10^{18}$ cm^{-3}, respectively. As we consider device design, we will concentrate primarily on the selective doping for holes (p). This range is achievable as these doping ranges are typical for most GaN growth [55], [56]. The next two performance metrics are the most challenging as will be the premise of considering these metrics in this dissertation. The device should have a breakdown voltage of ≥ 1200 V and a leakage current of $\leq 1\times10^{-9}$A (@ 600 V). The challenges of achieving these metrics will be elaborated more in Chapter 2 & 3 of this dissertation. The breakdown voltage and leakage current is associated with the device operated in the reverse regime. Metrics in the forward regime are also imposed. The specific on resistance (R_{DSON}) must be < $3m\Omega\cdot cm^2$ with a I_{on}/I_{off} of $>10^{10}$. Metrics on the avalanche capability require no parametric shift after repeated avalanche test, and a > 20 A surge capability for 10μs pulse at 25°C.

Now that the requirements of the selective-area doped *p-n* junction have been considered we will develop a testbench for the subsequent experimentation and analysis. The selective-area doped *p-n* junction has many challenges inherent to the design, specifically the aforementioned interfacial impurity and dry-etched enhanced damage. Therefore, to more easily understand the effect of these challenges we will study these challenges on even simpler device test structures (i.e. planar *p-n* diodes). Thus, the basic premise of this work is to understand the effects of the regrown junctions on these

simpler device structures which are integral to the architecture of the selective-area doped *p-n* junction.

In these complex device structures there are more than one crystalline plane of GaN which constitute the planes of the regrown at the junctions. Two important planes within Wurtzite GaN crystal structures are schematically represented in Figure 1.8. In Wurtzite GaN the III-V species are Ga and N, respectively. These planes are identified, in Figure 1.8.a, as the polar *c*-plane with miller indices (0001) and the nonpolar *m*-plane with miller indices $(10\bar{1}0)$. Each plane is identified as polar or nonpolar due to discontinuities in spontaneous and piezoelectric polarization from the configuration of the III-V species within the Wurtzite crystalline lattice [57]. The polarization has been used as an advantage for work on optoelectronic devices previously [58]. A cross-sectional crystalline lattice structure of GaN for basal *c*-plane and *m*-plane is represented schematically in Figure 1.8.b. An important difference between the two crystalline planes is the arrangement of the III-V species (Ga and N) at any plane, specifically the terminating plane. It may be observed that in the *c*-plane orientation there is a uniform amount of either Ga or N at the terminating planes which may be classified as either Ga-polar or N-polar termination. In the case of *m*-plane GaN there is an equal amount of Ga and N species at the termination plane of the crystalline structure. This fundamental difference has lead to an increased amount of impurity incorporation in *m*-plane GaN due to the presence of N atoms at the nonpolar surface [59].

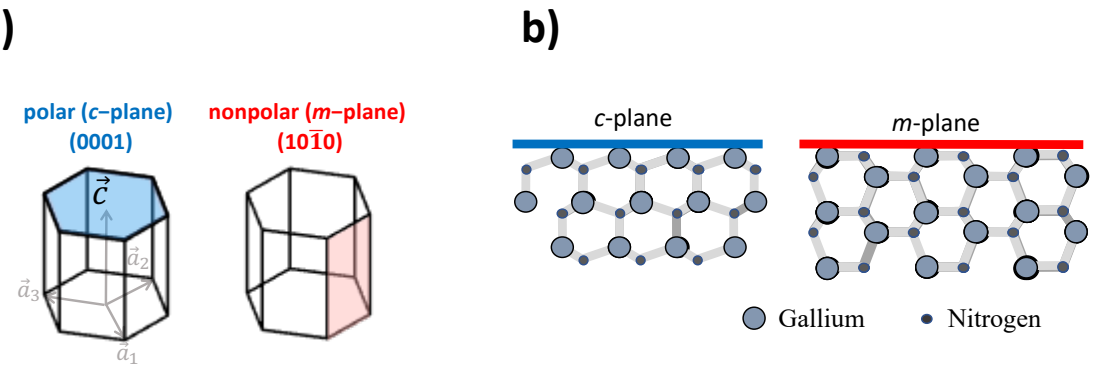

Figure 1.8. a) Crystal orientation representation of m-plane and c-plane in Wurtzite GaN GaN b) Schematic of crystalline lattice for *m*-plane and *c*-plane in Wurtzite GaN

Therefore, we can identify an example of the two important planes that are present within a selective-area doped *p-n* junction on GaN schematically in Figure 1.9.a. The basal (bottom) plane is constituted by the *c*-plane (0001) orientation. The basal *c*-plane orientation is suitable for industrial applications, specifically for light emitting diodes (LEDs), because of many benefits of this plane [60]. The cost effectiveness of *c*-plane GaN on sapphire substrates is very established. In turn, applications for electronics on GaN will most likely utilize the basal *c*-plane. However, junctions also exist at the side-wall planes of the vertical selective-area doped *p-n* diode, such as the *m*-plane (10$\bar{1}$0), in Figure 1.9.a. Additional planes, such as the *a*-plane (11$\bar{2}$0) or other semipolar planes, may also constitute the sidewall planes. The junctions at these additional planes play as much a critical role in the device performance as the basal *c*-plane. It follows that, in order to completely understand the effects of each plane on a selective-area doped *p-n* diode we must investigate each plane individually. Therefore, the motivation to perform studies on the less complex planar *p-n* diode on *m*-plane will be discussed.

A schematic representation of a planar *p-n* diode device architecture with the *m*-plane orientation highlighted is shown in Figure 1.9.b. As can be observed, *m*-plane junctions are present on the sidewalls of the trenches within selectively doped regions.

However, studying the sidewall junctions directly is difficult to accomplish. Thus, investigation on planar diodes allows us to investigate *m*-plane junctions more easily. The availability of free-standing *m*-plane substrates further enables this investigation. Additionally, work on the *m*-plane orientation for applications in power electronics has not been widely investigated as of late. Therefore, the junctions at the sidewall of the trenches within vertical selective-area doped *p-n* diodes will be studied more easily by investigating *m*-plane planar diodes.

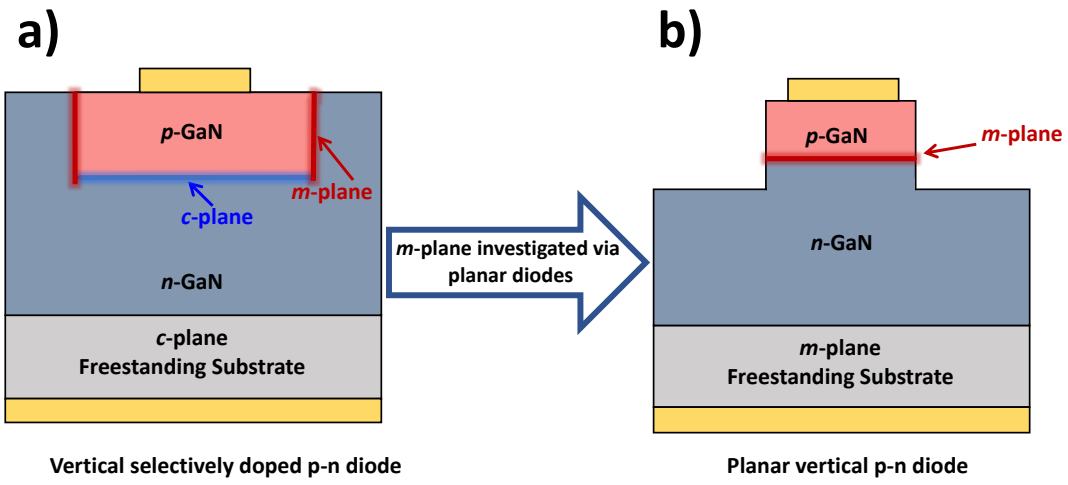

Figure 1.9 a) Schematic of relevant crystalline planes for selective-area doped *p-n* diode, and b) planar vertical *p-n* diode on *m*-plane orientation

As stated previously, the primary focus of this work is to be carried out on the *m*-plane orientation due to junctions present on the sidewalls of the trenches of selectively doped regions. Thus, the performance metrics of Table 1.2 will not specifically be targeted for the investigation of planar diodes on *m*-plane GaN, but they will guide us in our design and analysis. Nevertheless, on-going research is also being conducted in parallel on the *c*-plane orientation. Previous research on GaN vertical *p-n* diodes on the *c*-plane orientation without a selectively doped region has shown large blocking voltage (>

3.7 kV) [61], [62]. However, when introducing an etch-and-regrown process, GaN vertical *p*-*n* diodes on the *c*-plane orientation have shown lower blocking voltages (< 1.27 kV) [63]. Thus, the extension of the etched-and-regrowth process analogous to vertical selective-doped regions has proven to be much more challenging. Therefore, with on-going investigation on both *c*-plane and *m*-plane, a more complete understanding of vertical selective-area doped *p*-*n* diodes will hopefully motivate the next generation of power electronics on GaN.

1.6 p-n diode considerations

We previously described the motivation for studying planar diodes on the *m*-plane orientation due to junctions present on the sidewalls of the trenches of selectively doped regions. Therefore, some considerations must be taken in order to investigate the aforementioned challenges of interfacial impurities and dry-etched enhanced damage on these devices. Thus, the performance requirements for vertically selective-area doped *p*-*n* diodes, from Table 1.2, can be considered for our investigation on vertical planar *p*-*n* diodes. The three most important requirements are the breakdown voltage, reverse leakage current, and on-resistance (R_{DSON}). By considering these requirements for vertical planer *m*-plane *p*-*n* diodes, we may begin to develop some understanding of the most probable design architecture for our investigation.

The preeminent metric for design will be the breakdown voltage. The critical electric field and device dimensions will thus be tailored to increase this metric. Therefore, let us consider a one-sided junction. This design choice is made in order to allow the reverse-bias depletion region to extend predominantly in one region. An

additional design consideration is to use a p^+n junction because issues with *p*-type material quality manifest predominantly as p-type epitaxial layers become thick [64], [65]. Also, the conductivity of *p*-type GaN is substantially less than *n*-type GaN [66], [67]. Therefore, we will limit the dimensions of the p-type material which can be done by allocating it to the higher doping concentration layer in a p^+n one-sided junction. Under the one-sided junction approximation, the acceptor carrier concentration is much larger than the donor carrier concentration ($N_a \gg N_d$). Therefore, the majority of the depletion region depletion width (W) extends on the n-type side (x_n). Therefore, the depletion width (W) under reverse bias ($V_R \gg V_{bi}$) can be expressed as follows:

$$W \approx x_n \approx \left\{\frac{2\varepsilon_s(V_R)}{e}\left[\frac{1}{N_d}\right]\right\}^{1/2} \tag{1.3}$$

The terms in Equation 1.3 are denoted as the reverse bias voltage (V_R), the donor concentration (N_d), the charge of an electron (e), and the permittivity of the material (ε_s). By inspection we can observe that the depletion width (W) has a square root dependence on the reverse bias voltage (V_R). We may also write the maximum electric field (E_{max}) within the depletion region which occurs at the metallurgical-junction on a one-sided *p-n* diode as:

$$E_{max} = \frac{eN_d x_n}{\varepsilon_s} \tag{1.4}$$

By also considering the reverse bias voltage (V_R) at the maximum blocking (V_R) when the E_{max} is the critical electric field E_{crit}:

$$V_R = V_B \text{ at } E_{max} = E_{crit} \tag{1.5}$$

Substituting these into equation 1.3 and 1.4 and rearranging we get:

$$V_B = \frac{\varepsilon_s E_{crit}^2}{2eN_d} \tag{1.6}$$

The relationship between the maximum blocking voltage (V_B) and critical electric field (E_{crit}) will guide us into determining the thickness of the *n*-type GaN. The depletion region will extend primarily into this region when considering the one-sided junction design. We will denote the *n*-type GaN side of the junction as the "drift" region due to the mechanism in which current flows within the depletion region. As carriers enter the depletion region they are swept by a drift mechanism in the presence of the electric field.

From Equation 1.3 we can see the depletion region width (W) is a function of the carrier density of the *n*-type region (N_d). We may also observe that the maximum blocking voltage (V_B) is also a function of the carrier density of the *n*-type region (N_d). Therefore, to increase the maximum blocking voltage (V_B), the carrier density of the *n*-type region (N_d) must be decreased. This also has the advantage of reducing the maximum electric field (E_{max}) in the depletion region. Thus, the doping density of the p-type region is selected to be the maximum allowable, which for our case is $N_a = 1\times10^{19}$ cm^{-3}. Also, the free-carrier donor density in the n-type region is selected to be $N_d = n_o = 1\times10^{16}$ cm^{-3}. We will elaborate on the limitation of intentional doping concentrations in Chapter 2, during our discussion of growth. If we plot reverse bias

voltage (V_R) versus depletion region width in the n-side and p-side of the diode we obtain the plot presented in Figure 1.10.

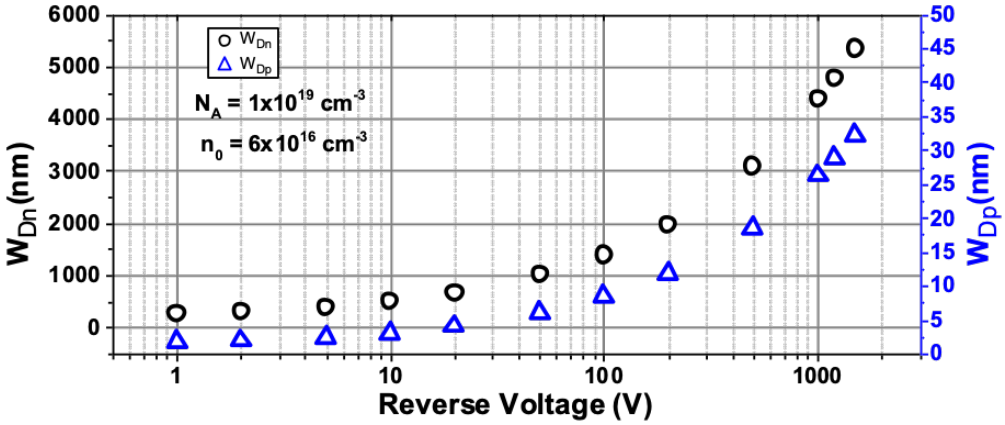

Figure 1.10 Depletion region thickness in p-type and n-type region of a one-sided *p+n* diode

If we consider a breakdown voltage of ≥ 1200 V for the one-sided *p-n* diode with the previous doping concentrations, the depletion region extends ~5000 nm into the *n*-type region and ~30 nm into the *p*-type region. Therefore, a minimum thickness of the *n*-type region is 5000 nm, and a minimum thickness of the *p*-type region is 30 nm in order to achieve a breakdown voltage of ≥ 1200 V. The *p*-type layer will be chosen to be a thickness of 400nm due to the design requirements for the vertical selective-area doped *p-n* diode structure. A cross-sectional schematic of the epitaxial structure based on these design principles for the vertical planar *p-n* diode is shown in Figure 1.11. The use of a conductive free-standing native substrate (*m*-plane) is used in order to ensure that the planar *p-n* diode may be fabricated into a vertical design. A 2 µm n-GaN template region is grown first in order to ensure smooth epitaxy of the subsequent layers.

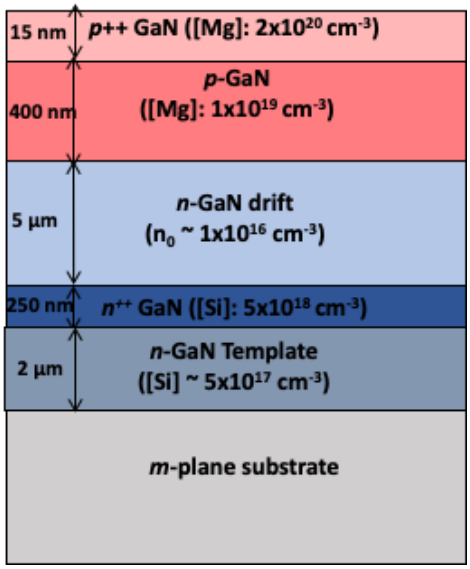

Figure 1.10. Cross-sectional schematic of a vertical *p–n* diode based of the design consideration for vertical selective-area doped *p-n* diodes for power electronics.

An additional n^{++} *n*-GaN layer is grown to ensure proper conductivity to the n-GaN drift region. The low doped ($n_o = 1\times10^{16}$ cm^{-3}) 5µm *n*-GaN drift region is grown next. After this step, the diode may be grown continuously, or undergo a treatment (dry-etching, acid exposure, ambient exposure, etc.). As mentioned previously, the basic premise of this dissertation is the investigation of these processes and their effects on the planar *p-n* diode. Nevertheless, 400 nm of *p*-GaN is grown/regrown with a high doping concentration ($N_a = 1\times10^{19}$ cm^{-3}). Subsequently, 150 nm of p^{++}-GaN is grown to constitute the *p*-type contact layer. More detailed explanation of the epitaxial growth process will be expounded upon in Chapter 2 of this dissertation.

We have quickly developed some design features for the planar *p-n* diode in order to minimize the maximum electric field (E_{max}) and ensure the depletion region extends primarily into the *n*-type side of the planar *p-n* diode. These features include a high doping concentration on the p-side of the junction, a low doping concentration on the n-

side of the junction, and a large drift region for an extended depletion width at high reverse voltages. In order to study the effects of incorporating a selective-area doped *p-n* diode structure the basic experimental design phase of diode growth will follow: 1) growth of the n-GaN template region, n^{++}-GaN contact layer, and the n-GaN drift region 2) surface treatment in or outside the growth chamber, and 3) regrowth on p-GaN and p^{++}-GaN contact layers. Therefore, the remaining content of this work will concentrate on the effects of this growth process on the planer *p-n* diode performance.

1.7 Summary and Organization of Dissertation

The motivation of next-generation power electronics has been considered with the requirements for higher efficiency devices in power generation, transmission, and storage. Applications range from power converters and inverters, power flow controllers, variable frequency drives, AC-DC converters, and battery charging and traction drive inverters, to name a few. Advances in reduced electrical consumption, reduced losses, reduced cost, and increased efficiency motivate the next generation of power electronics devices. Therefore, low-loss power semiconductor devices are continuing to be researched and developed to meet these goals.

The design architecture of these next generation power electronic systems also motivates the move toward vertical device geometries. Many benefits include current handling, increased blocking voltages, small form-factors, reduced parasitic inductance, low on-resistance, and suppressed current collapse. Therefore, a move toward these vertical architectures may enable low-loss and more efficient semiconductor devices for use in power electronics systems.

An additional motivation for next generation power electronic devices is the use of wide-band gap materials. Many benefits of the wide band-gap materials arise due to their ability to withstand higher critical electric fields while also maintaining low on-resistances. One material that stands out as a possibility for next generation power electronic devices is GaN. Inherently possessing a large bandgap (3.39 eV), high Baliga figure-of-merit (BFOM = 67-83), and wide adoption in industry for optoelectronics, GaN is ideal for power electronic devices.

Nevertheless, challenges must be overcome in order to implement vertical architectures for power electronic devices on GaN. The primary challenge is the implementation of selective-doped regions within the device of the aforementioned architecture. Two candidates to implement selective-doping are selective-area ion implantation and selective-area doping. The effect of each method is to create areas within a bulk semiconductor material with a specific dopant-type of material. Benefits and challenges were discussed briefly, and it was determined that the use of selective-area doping would be the more beneficial method.

Primary challenges associated with implementing selective-area doping are identified as interfacial impurities at regrown junction, and dry-etch enhanced damage on the semiconductor crystal. A brief origin and effect of these challenges for applications in vertical selective-doped devices was discussed. However, the remaining content of this dissertation is concerned with developing experiments in order to understand and mitigate these challenges.

Device performance requirements for a vertical selective-doped *p-n* diode was discussed briefly, with several figure-of-merit metrics being required. The three most

important are a breakdown voltage, reverse leakage current, and a specific on resistance (R_{DSON}). Furthermore, a motivation to investigate planar *p-n* diodes was made by considering the different crystallographic planes present on the sidewall of the trenches in vertical selective-doped *p-n* diodes. We identified the polar $(10\bar{1}0)$ *m*-plane as an important crystallographic plane as it often constitutes the sidewall of the trenches of vertical selective-doped *p-n* diodes. We briefly discussed the differences of this plane versus non-polar (0001) *c*-plane. We identified a different atomtronic arrangement at the surface between these planes and the unique challenges that must be considered. As mentioned, not much effort has been made on the investigation of the *m*-plane junctions for the purpose of vertical selective-doped devices for power electronics. Therefore, investigation of this plane will yield a more concise understanding of vertical selectively doped *p-n* diodes.

After developing the motivation for planar *m*-plane vertical *p-n* diodes as a testbench for experimentation, we considered some basic design considerations. By considering the requirements for the vertical selective-doped *p-n* diode, we developed the device design architecture. We briefly discussed the use of a one sided p^+n diode in order to minimize the maximum electric field (E_{max}) and ensure the depletion region extends primarily into the *n*-type side of the planar *p-n* diode. We proposed that in-order to achieve the maximum breakdown voltage, the device would require 1) high doping on *p*-side of the junction, 2) low doping on *n*-side of the junction, and 3) extended drift region to accommodate the large depletion width. By considering these requirements we have developed the testbench device for the remainder of this work. The subsequent chapter

will utilize this device in order to understand and mitigate the challenges of implementing a vertical selective-doped *p-n* diode.

1.8 Dissertation Organization

This dissertation will be organized into 5 chapters, including the introduction (Chapter 1), along with 3 appendices. Chapter 2 will present the effects of interfacial impurities on planar m-plane p-n diodes. Identification of these impurities and their effects on the electrical characteristics will be shown. Additional methods, such as surface treatment and device architecture changes, will be presented in an attempt to mitigate these effects.

Chapter 3 will study the effects of dry-etched enhanced damage on *m*-plane Schottky diodes. The motivation and analysis for using these structures with steady-state photocapacitance (SSPC) and lighted capacitance-voltage (LCV) measurements will be presented. Identification of elevated deep level traps and concentrations enhanced on dry-etched GaN Schottky diodes will be compared with electrical testing in order to identify the effects of such processes. Additionally, surface treatments will be investigated in order to mitigate the effects of dry-etched enhanced damage by showing a reduction of the concentrations of the elevated deep level traps.

Chapter 4 will present a novel electrical characterization method using a radio-frequency (RF) technique to investigate carrier dynamics in the presence of dry-etch enhanced damage at the junctions of p-n diodes. A small-signal model will be presented along with obtained experimental complex impedance data in order to determine

parameters such as, series resistance, differential resistance, capacitance, and minority carrier lifetimes of a p-n diode.

Chapter 5 consists of a conclusion of the dissertation and proposed future work. Future work focuses on the continuing development of selective-doped *p-n* diodes on GaN for application in power electronic devices. Further methods to mitigate the challenges of interfacial impurities and dry-etched enhanced damage will be presented. Further investigation of the effects of current leakage using various surface treatments using the RF technique may be developed. Additional techniques such as field-confinement structures and improved device isolation will be discussed in order to achieve greater efficiency. Finally, the implementation of a complete vertical selective-doped p-n diode on the m-plane orientation may be realized.

Appendix A provides relevant information and background for several derivations and equations utilized throughout this dissertation.

Appendix B provides additional information on MOCVD growth, process information, and dry/wet etching processes and calibration

Appendix C provides additional information on the electrical, optical, and morphological, characterization methods utilized in this work.

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Chapter 2 Interfacial Impurities: effects on planar m-plane p-n diodes.

In this chapter the impacts of interfacial impurities (silicon, carbon, and oxygen) on the electrical performance of high-voltage vertical GaN-based p–n diodes are investigated. Techniques for growing and fabricating *p-n* diodes are discussed in order to achieve the optimal design for the performance metrics required (Table 1.2). Moderate levels (~ $5x10^{17}$ cm^{-3}) of all interfacial impurities lead to reverse blocking voltages (V_b) greater than 200 V at 1 μA / cm^2 and forward leakage of less than 1 nA/cm^2 at 1.7 V. With higher interfacial impurity levels (> $5x10^{17}$ cm^{-3}), the performance of the diodes begins to degrade. From investigation, each impurity species has a different effect on the device performance as well. For example, a high carbon spike at the metallurgical junction of the *p-n* diode correlates with high off-state leakage current in forward bias (~ 100 higher forward leakage current compared with a reference diode), whereas the reverse bias behavior is not severely affected (> 200 V). The presence of high silicon and oxygen spikes at the metallurgical junction strongly affects the reverse leakage currents (~ 1–10 V at 1 μA cm^2). However, regrown diodes with impurity (silicon, oxygen, and carbon) levels below $5x10^{17}$ cm^3 show comparable forward and reverse results with the reference continuously grown diodes.

The effect of the regrowth interface position relative to the metallurgical junction on the diode performance is also discussed. By investigating the position of the regrown interface and metallurgical junction we determine the effects of interfacial impurities when located outside the depletion region. Blocking voltages are marginally improved, but as the depletion region extends past the regrowth junction the reverse leakage increases.

2.1 Growth rate of *m*-plane GaN

Considerations of the design of the optimal vertical *p*-*n* diode epitaxial structure have been made previously in Chapter 1. The design was selected to incorporate a one-sided p^+n junction in order to reduce the maximum electric field, extend the depletion region into the n-side of the diode, and thus increase the maximum blocking voltage of the diode. As we will investigate, epitaxial growth will play a critical role in the development of the vertical *m*-plane GaN *p*-*n* diodes. The two primary methods of epitaxial growth of GaN are metal organic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE). For the purposes of this dissertation, all epitaxial growth of GaN is produced by metal organic chemical vapour deposition (MOCVD). Growth of GaN has been readily established by this method for its many benefits such as fast growth rates and large throughput as compared to other methods which is advantageous for vertical power devices. Additional information on metal organic chemical vapor deposition (MOCVD) growth of GaN is presented in Appendix B.

Nevertheless, some growth considerations are required in order to further optimize the diode structure in order to achieve the best possible performance metrics. The two main considerations we investigate will be GaN growth rate and *n*-type doping control. These considerations are especially important due to their effects on impurity incorporation within the material. The incorporation of impurities has effects of increasing or reducing intentional doping profiles of desired devices. Thus, effectively minimizing the incorporation of impurities in epitaxial grown GaN material is very important for power device applications which are highly sensitive to doping profiles.

The first consideration we will investigate is the growth rate. The growth rate is especially important for vertical power devices due to the requirements of large (several um) regions within the device architecture that allow for increased blocking voltages, as discussed previously. Therefore, for purposes of large throughput, the growth-rate must be increased. However, challenges associated with an increased level of impurity incorporation accompany increased growth rates. A calibration sample with varying growth rates was grown on a free-standing *m*-plane substracte with a ~ 0.95 miscut toward the minus c-direction from Mitsubishi Chemical Corporation. Four regions each ~ 1 µm thick of unintentional-doped (UID) GaN were grown with growth rates of 0.49, 1.16, 1.89, and 2.56 µm/ hr, respectively. A schematic representation of the calibration sample is shown in Figure 2.1.

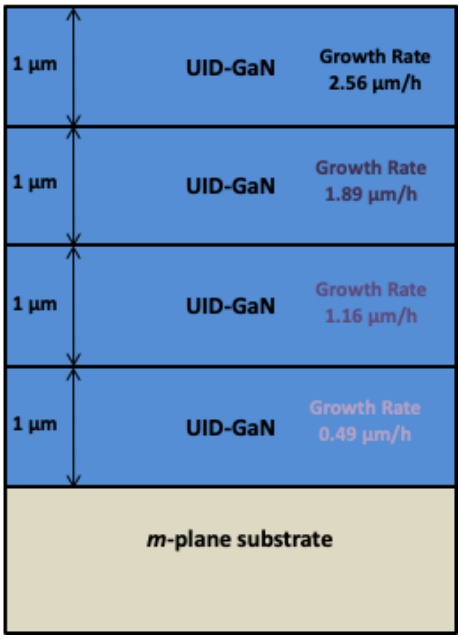

Figure 2.1. Schematic of calibration sample with four regions with differing growth rates (0.49, 1.16, 1.89, and 2.56 µm/ hr.) controlled by the flow of group-III source Trimethylgallium (TMG).

The epitaxial layers were grown at a pressure of 500 Torr using trimethylgallium (TMGa) and ammonia (NH_3) as precursors for elemental Ga and N, respectively, grown at a substrate temperature of ~960 °C measured by a pyrometer. The growth rates were controlled by the III-V ratio by the flow of the group-III source trimethylgallium (TMGa). By increasing the flow of the group-III source the III-V ratio is decreased. However, due to the increase in group-III species Ga, which is slower to incorporate into the lattice than N, the growth rate increases.

The concentration of impurities (Si, O, and C) of the calibration sample were analyzed by secondary ion mass spectroscopy (SIMS). The detection limits (sensitivity) of the analysis are: $Si = 3\times 10^{15}\text{cm}^{-3}$, $O = 1\times 10^{16}\text{cm}^{-3}$, $C = 5\times 10^{15}\text{cm}^{-3}$all with a depth resolution of 12.5 Å. The depth profiles of the impurities within the calibration sample are presented in Figure 2.2.a.

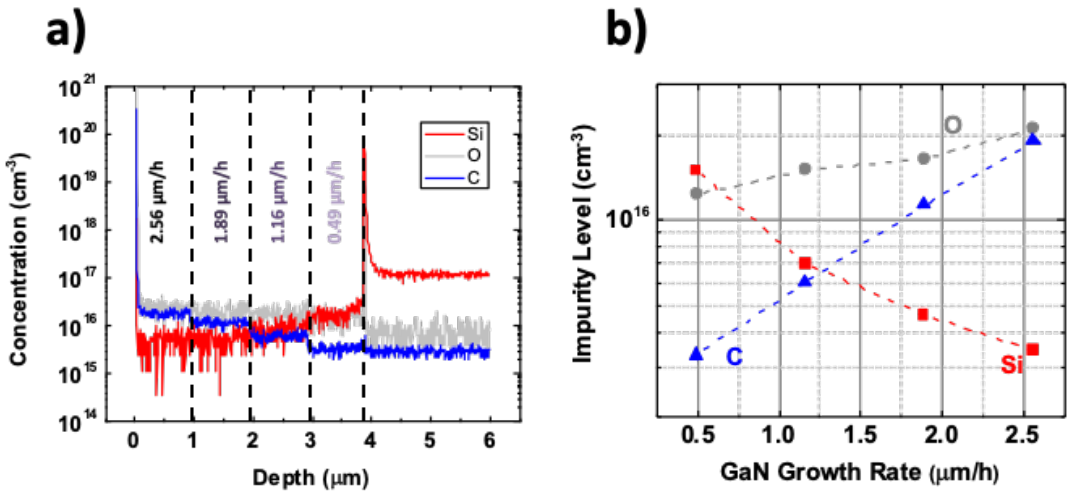

Figure 2.2. Secondary ion mass spectroscopy (SIMS) of calibration sample showing impurity concentrations of (Si, O, and C) versus a) depth, and b) growth rate.

Impurity concentrations within each level are shown within each region corresponding to the different growth rates of the varying III-V ratio. Impurity concentrations are averaged within each region and presented versus growth rate in figure 2.2.b. It may be observed that the impurity concentrations vary with respect to growth rate.

The background Si impurity level decreases from ~ $1.5\times 10^{16}cm^{-3}$ at 0.49 μm/ hr to to ~ $3.4\times 10^{15}cm^{-3}$ at 2.56 μm/ hr. The sharp spike in Si at ~ 4μm is associated with the interface of the grown epitaxial layer and the m-plane substrate. This elevation may be due to electro-chemical polishing of the substrate or ambient impurities as the substrate is being loading in the MOCVD reactor. Nevertheless, the decrease in Si in the grown epitaxial layers is associated with the increased group-III source Ga at higher growth rates. Si primarily occupies the Ga lattice position when used as a typical n-type dopant [1]. Therefore, Si is less likely to incorporate within the epitaxial layer when an increase in group-III Ga species present. Thus, high growth rates are beneficial for reducing the Si background impurities within epitaxial MOCVD grown GaN.

The background C impurity is observed to increase from ~ $3.3\times 10^{15}cm^{-3}$ at 0.49 μm/ hr to ~ $1.8\times 10^{16}cm^{-3}$ at 2.56 μm/ hr. The increase in C is attributed to the increase of the group-III flow TMGa ($Ga(CH_3)_3$). Previous publications have identified hydrocarbon contamination of TMGa to be the dominant source of carbon contamination in MOCVD grown n-GaN [2]. Thus, more hydrocarbon fragments are expected by increasing the growth rate through the increasing TMGa flowrate. Additionally, carbon is not favorable to occupy interstitial sites due to a large formation energy [3]. However, the presence of a Ga-rich environment, such as the case when obtaining high growth rates

by increasing the TMGa flowrate, has shown to increase the concertation of N vacancies [4]. Therefore, an increase probability of C on N sites (C_N) is expected, due to this being the lowest formation energy for C in UID-doped GaN. Thus, an increased growth rate has shown to be disadvantageous due to increased C impurity incorporation.

The background O impurity is observed to increase from ~ 1.2×10^{16}cm^{-3} at 0.49 µm/ hr to ~ 2.1×10^{16}cm^{-3} at 2.56 µm/ hr. However, the increase in O impurity is not as drastic as that of C. The source of O maybe due to contamination of the MOCVD chamber or contamination of the group-V source ammonia (NH_3) [5]. However, ammonia is held constant while increasing the growth rate through the increase TMGa flowrate. Thus, the increase in O is again attributed to the increase of the group-III flow TMGa ($Ga(CH_3)_3$). Again, O is not favorable to occupy interstitial sites due to a large formation energy [6]. But, as discussed previously, an increase in the concertation of N vacancies is present in the presence of a Ga-rich/ N-poor environment, such as the case when obtaining high growth rates by increasing the TMGa flowrate. Furthermore, O substituting N (O_N) has a low formation energy, and substitutional O_N typically acts as a shallow donor in GaN [7]. Additional complexes such as O_N-C_N and O_N-$C_{Ga,}$ also have low formation energies [8]. Nevertheless, an increase in O impurity is found with increasing growth rate, which again is disadvantageous.

We now have some key take-aways from looking at the background impurity incorporation as a function of growth rate. We have observed a decrease in the incorporation of the impurity Si as growth rate increases. The decrease is substantial at almost an order of magnitude from ~ 1.5×10^{16}cm^{-3} at 0.49 µm/ hr to to ~ 3.4×10^{15}cm^{-3} at 2.56 µm/ hr. Thus, higher growth rates are advantageous for Si incorporation.

However, increases in the impurities C and O are observed with increased growth rate. A substantial increase in C from ~ 3.3×10^{15}cm^{-3} at 0.49 μm/ hr to ~ 1.8×10^{16}cm^{-3} at 2.56 μm/ hr. A marginal increase in O is observed from ~ 1.2×10^{16}cm^{-3} at 0.49 μm/ hr to ~ 2.1×10^{16}cm^{-3} at 2.56 μm/ hr. Therefore, we must choose a faster growth rate which requires a trade-off of low Si impurity incorporation for marginal C and O incorporation. As we will discuss in the subsequent section, Si n-type doping can only be controllable down to ~ 5×10^{16}cm^{-3}. Therefore, choosing a growth rate which yields < 2×10^{16}cm^{-3} background impurities is reasonable to insure no effect on the intentional doping. Thus, all subsequent epitaxial layer grown by MOCVD on *m*-plane GaN within this body of research will have a growth rate of ~ 2.0 μm/ hr.

2.2 Silane (SiH_4) doping control of *m*-plane GaN

Doping control has been mentioned in Section 1.5 as one of the requirements for vertical selectively doped *p*-*n* diodes. We further elaborated that the precise control of doping profiles was advantageous for use in these devices. Thus, a move toward vertical planar diodes was made with the same requirements. In the device consideration in Section 1.6, we determined to incorporate a one-sided p^+n junction utilizing a low doped *n*-drift region as the region in which the depletion region must extend. The carrier concentration was selected to be $n_0= 1\times10^{16}$cm^{-3} in order to determine the length of the low doped *n*-drift in order to accommodate the depletion region extent. We will now discuss the selection of this carrier concentration in light of the minimum tolerable doping of the MOCVD system used for the duration of this work.

The n-type dopant which is widely used for doping MOCVD grown GaN is Silane (SiH_4). We have previously discussed Si when considering unintentional background impurities during epitaxial growth. However, Si will be considered here as a intentional impurity in order to control the doping profiles of the vertical planar *p-n* diodes. Again, a calibration sample is grown on free-standing *m*-plane with various doping levels in order to observe the minimum controlled tolerance of Si doping. Figure 2.3.a schematically shows the epitaxial stack of the Si doping calibration sample. Alternating layers of doped (250 µm) and unintentionally-doped (UID 150 µm) GaN are grown with the aforementioned growth rate of 2 µm/ with a V/III ratio of 1710. Other growth parameters are held constant which include N_2 flow of 3710 sccm, NH_3 flow of 2100 sccm, pressure of 500 Torr, and temperature of 970°C. Si molar flow is varied from 2.26×10^{-12} to 5.3×10^{-9} by controlling the raw flow, push flow, and double dilution of SiH_3.

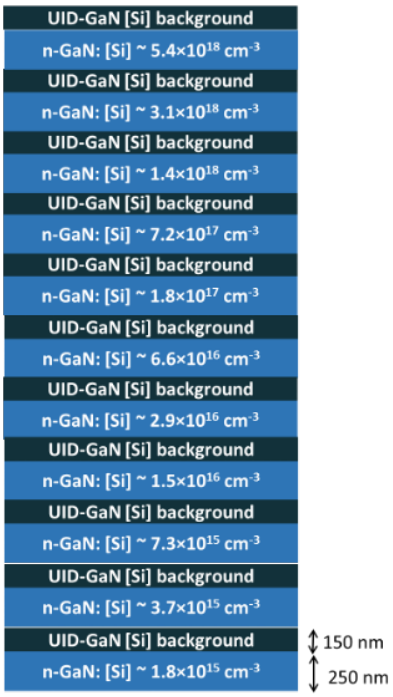

Figure 2.3. Schematic of *n*-type Si doping calibration sample with 11 regions with differing doping concentrations controlled by the flow rate of the Silane (SiH_3)

The concentration of impurities (Si, O, and C) of the calibration sample were analyzed by secondary ion mass spectroscopy (SIMS). The detection limits (sensitivity) and depth resolution are the same as previously stated at: $Si = 3\times 10^{15}\text{cm}^{-3}$, $O = 1\times 10^{16}\text{cm}^{-3}$, $C = 5\times 10^{15}\text{cm}^{-3}$and 12.5 Å, respectively. The depth profiles of the impurities within the calibration sample are presented in Figure 2.2.a. Distinct peaks corresponding to each individual layer of n-type doping are obtained for the impurity Si. The impurity levels of O and C are $4.2\times 10^{16}\text{cm}^{-3}$ and $2.8\times 10^{16}\text{cm}^{-3}$. Targeted and measured Si concentrations versus molar flow for the calibration sample are presented in Figure 2.4.b. Targeted Si concentrations are obtained by the ratio of SiH_3 molar flow and total molar flow of species within the MOCVD chamber during growth, and measured Si concentrations are the average of Si concentrations over the thickness of each doped layer obtained by SIMS.

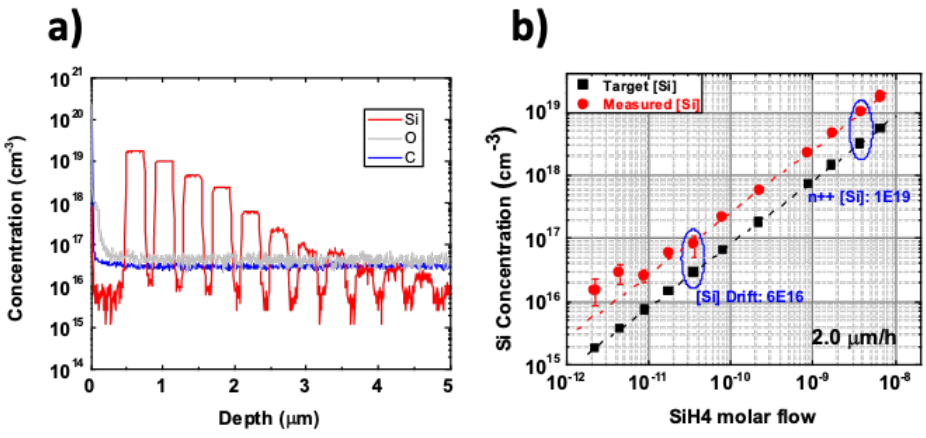

Figure 2.4.a) Secondary ion mass spectroscopy (SIMS) of calibration sample showing impurity concentrations of (Si, O, and C) versus a) depth, and b) Measured Si concentration and targeted Si concentration versus SiH_4 molar flow.

By inspection of the Si impurity profiles in figure 2.4.a, it may be observed that the regions corresponding with low molar flow ($< 3.5\times10^{-11}$) have a non-uniform Si profile. Additionally measured Si concentration follows a linear trend versus SiH_4 molar flow above 3.5×10^{-11}. Below this value of SiH_4 molar flow, the data deviates from the linear trend which indicated the minimum controllable Si doping concertation ([Si] = $6.0\times 10^{16}cm^{-3}$). It may also be noted, that targeted Si concentration values are slightly lower than measured Si concentration values. This is due to the calculation of Si concentration from the fractional molar flows of all growth species which does not take into account the growth kinematics (temp, binding energies, etc.) which influence each species' lattice incorporation. Nevertheless, the calculation yields a relative estimate of Si incorporation when increasing SiH_4 molar flow.

Therefore, we have determined the minimum controllable Si dopant level ([Si] = $6.0\times 10^{16}cm^{-3}$) for use in our study of vertical m-plane GaN *p-n* diodes. This limit is directly attributed to the tolerance of the mass-flow controllers used on the MOCVD reactor used during the duration of this work. Lower controllable limits may be obtained if more precise MFCs are implemented into the reactor system. Nevertheless, our lower limit for *n*-type doping will be used for the drift regions of the subsequent diodes presented.

2.3 Effects of growth interruption on interfacial impurities

The effects of interfacial impurities are now explored with respect to growth interruptions. Calibration samples with several growth interruptions were grown for *n*-type and *p*-type conditions without the use of intentional doping for each. The purpose of

these calibrations samples is to identify potential differences in impurity incorporation between the two growth conditions. Four growth interruptions were performed after ~ 750 nm of growth between each interruption, respectively.

The epitaxial growth structure of the n-type calibration sample is shown in Figure 2.5.a. The calibration sample was grown on free-standing *m*-plane GaN substrate. The calibration sample *n*-type growth condition consisted of: N_2 flow of 3710 sccm, NH_3 flow of 2100 sccm, pressure of 500 Torr, temperature of 970°C, and V/III ratio of 1710. As mentioned previously, no intentional doping was desired. Thus, SiH_4 was not flowed into the chamber. During the first interruption (1), the sample was kept in the MOCVD growth chamber for 10 minutes. During the second interruption (2), the sample was brought into the load-lock of the MOCVD chamber for 10 minutes. During the third interruption (3), the sample was brought outside the MOCVD chamber for 10 minutes. During the fourth interruption (4), the sample was kept outside the MOCVD chamber for one week in a nitrogen box.

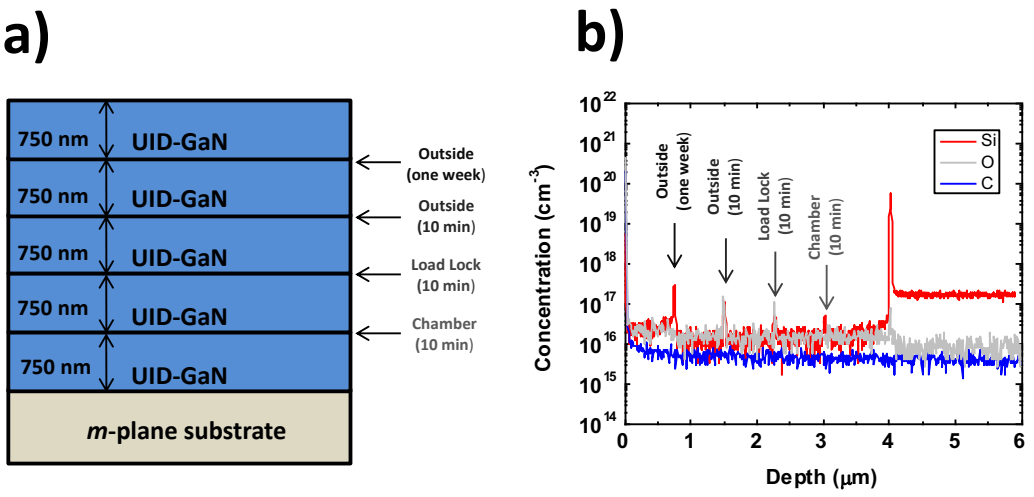

Figure 2.5.a) growth interruption impurity interface calibration sample (*n*-type condition) b) SIMS impurity profile of calibration sample (*n*-type condition)

Impurity concentrations of Si, O, and C versus depth were measured by SIMS of the growth interruption calibration sample using *n*-type growth conditions, and is shown in Figure 2.5.b. The detection limits and depth resolution of the SIMS profile is the same as that presented in previous sections. The effects of the growth interruptions can be observed from the SIMS profile, and distinct spikes in the impurity concentrations are observed for each interruption. Specifically, spikes in the Si and O impurity levels are observed at each interruption. The large spike observed at ~ 4 μm is due to the interface of the epitaxial layers and the free-standing *m*-plane substrate. Nevertheless, spikes in Si for interruptions (1) and (2) are nominally the same at ~5.1×10^{16}cm^{-3}. Spikes in Si for interruption (3) and (4) are observed to be 1.1×10^{17}cm^{-3} and 2.9×10^{17}cm^{-3}. Therefore, as increasing time within and outside the chamber yields elevated Si impurities at the epitaxial surface. The full-width half-maximum (FWHM) of the spikes are ~ 20-30 nm as well. The background Si concentration is also observed to be ~1.1×10^{16}cm^{-3} between interfaces with a slight increase to ~2.1×10^{16}cm^{-3} in the last layer. These differences may be attributed to an increased contamination of the MOCVD reactor due to sample loading. Spikes in O levels are also observed at growth interruption positions as observed in the SIMS profile. However, they are only present at interruption (2) and (3) with concentrations of ~1.0×10^{17}cm^{-3} and ~1.4×10^{17}cm^{-3} with FWHM of ~ 15-25 nm. The lack of a spike at interruption (1) and (4) indicates the sporadic nature of impurity incorporation during growth interruption. Further elaboration on this will be made when comparing interfacial impurities at regrown junctions in *p*-*n* diodes. The background O impurity level is ~1.5×10^{16}cm^{-3} with slight elevation to ~2.0×10^{16}cm^{-3} in the last layer. The C impurity level is fairly consistent throughout the growth interruptions with a

concentration of $\sim 4.5\times 10^{15}$cm^{-3}. Thus, we can conclude that growth interruptions have no effect on C incorporation.

The epitaxial growth structure of the p-type calibration sample is shown in Figure 2.6.a. The calibration sample was grown on free-standing *m*-plane GaN substrate. The calibration sample *p*-type growth condition consisted of: H_2 flow of 3500 sccm, NH_3 flow rate of 2000 sccm, pressure of 205 Torr, temperature of 835°C, and V/III ratio of 2560. Again, no *p*-type dopant (Bis(cyclopentadienyl)- magnesium (Cp_2Mg)) was flowed into the chamber. The exact same interruptions as previously described for the n-type growth condition calibration sample were performed on the p-type growth condition calibration sample.

Again, impurity concentrations of Si, O, and C versus depth was measured by SIMS of the growth interruption impurity interface calibration sample using *p*-type growth conditions and is shown in Figure 2.6.b.

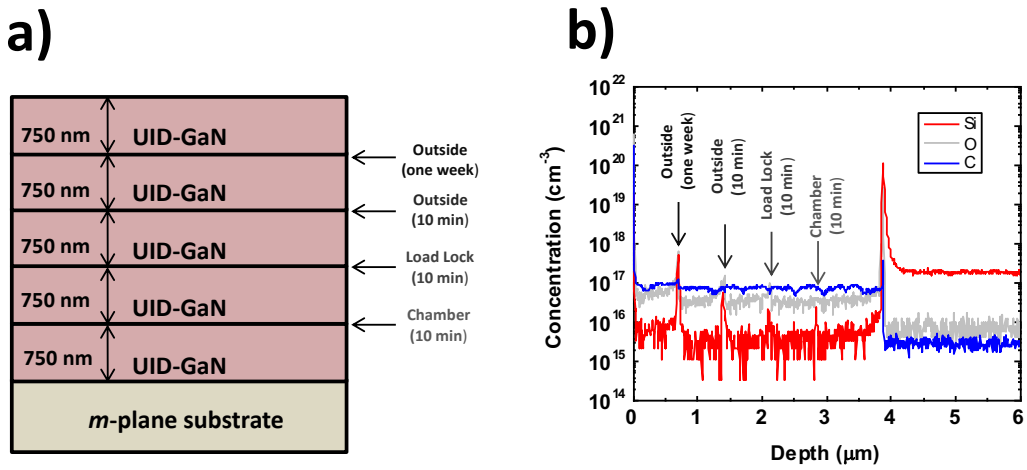

Figure 2.6.a) growth interruption impurity interface calibration sample (*p*-type condition) b) SIMS impurity profile of calibration sample (*p*-type condition)

Detection limits and depth resolution of the SIMS profiles are also the same as that presented in previous sections. Spikes in the Si and O impurity levels are also observed at each interruption. Spikes in Si for interruptions (1) and (2) are again nominally the same at ~2.3× 10^{16}cm^{-3}. Spikes in Si for interruption (3) and (4) are observed to be 5.6× 10^{16}cm^{-3} and 5.0× 10^{17}cm^{-3}. Therefore, as increasing time within and outside the chamber yields elevated Si impurities at the epitaxial surface. The full-width half-maximum (FWHM) of the spikes are ~ 20-30 nm as well. The background Si concentration is also observed to be ~3.1× 10^{15}cm^{-3} between interfaces with a slight increase to ~6.1× 10^{16}cm^{-3} in the last layer. Spikes in O levels are also observed at growth interruption positions except at interruption (1). The spike for interruption (2), (3), and (4) have concentrations of ~9.5× 10^{16}cm^{-3} , ~1.5× 10^{17}cm^{-3}, and ~6.4× 10^{17}cm^{-3} with FWHM of ~ 10-60 nm. It may be observed that the O spike isn't as 'sharp' with a slight tail into the subsequent layer observed. The background O impurity level is ~2.9× 10^{16}cm^{-3} with slight elevation to ~5.2× 10^{16}cm^{-3} in the last layer. The C impurity level is again not characterized with any sudden spikes at the growth interruption interfaces. However, slight dips in the C concentration are observed which don't correspond to growth interruption interface. However, the source of these dips could be due to subtle variations in the MOCVD parameters during growth. Nevertheless, the background C impurity is ~ 7.8× 10^{16}cm^{-3}, and we can conclude that growth interruptions have no effect on C incorporation.

The differences in *p*-GaN and *n*-GaN growth conditions can be compared as well. The presence of Si spikes corresponding to each growth interruption in both conditions

are observed with almost identical levels. An elevation on the background Si impurity level is observed in the n-type condition ($1.1\times 10^{16}cm^{-3}$) compared to the p-type condition ($3.1\times 10^{15}cm^{-3}$). Spikes in O are also nominally the same between the two conditions with similar levels. However, the background impurity O level is elevated in *p*-type condition ($2.9\times 10^{16}cm^{-3}$) compared to the *n*-type condition ($1.5\times 10^{16}cm^{-3}$). Carbon levels are mostly constant throughout both growth condition with no carbon spikes at each growth interruption. The *p*-type growth condition yielded higher background C level ($7.8\times 10^{16}cm^{-3}$) compared to the *n*-type growth condition ($4.5\times 10^{15}cm^{-3}$). The differences between the two growth conditions is directly attributed to the differences in MOCVD growth parameters used for each condition. Slight variations due to parameter fluctuation and sample handling is negligible for this experiment. Furthermore, impurity spikes induced during growth interruptions increase in severity as the sample is brought out of the growth chamber or held outside the chamber for longer periods of time. The Si impurity spikes shows that the Si impurities remain largely confined to the vicinity of the growth interruption without diffusing throughout the growth. However, O impurities spikes are narrow in the *n*-type growth condition sample, but they diffuse slightly in the *p*-type growth condition sample. Thus far, we have observed the effects of growth interruptions and the differences in impurity incorporation on MOCVD grown m-plane GaN in both *n*-type and *p*-type growth conditions. The interfacial impurity concentrations for all interruptions remained below 5×10^{17} cm^{-3} in, which is similar to previously published *c*-plane GaN studies [9]. The subsequent sections of this chapter will investigate the behavior of the impurities and their effects on

the electrical characteristics when placed at the metallurgical junction of *n*-GaN and *p*-GaN within *p*-*n* diode structures.

2.4 Growth of interrupted/treated vertical *m*-plane GaN *p*-*n* diodes

The effects of interfacial impurities on *m*-plane GaN *p*–*n* diodes is investigated in order to observe the impurity incorporation at regrown interfaces, and observe the effects they have on the device electrical characteristics. Thus, we will use what we have learned in the previous sections (2.1-2.3) along with our design considerations (1.6) to briefly describe the growth of the vertical *m*-plane GaN *p*–*n* diode structures for this purpose. Additional information on the subsequent studies may be found the previous publications [10–12].

The *p*-*n* diode epitaxial layers were grown using MOCVD on freestanding *m*-plane GaN substrates. A ~0.95º miscut toward the minus *c*-direction is used on the substrate from Mitsubishi Chemical Corporation (MCC). This miscut, along with growing in N_2 carrier gas, was shown to effectively mitigate the formation of pyramidal hillocks [13]. The *n*-type growth conditions consisted of: N_2 flow of 3710 sccm, NH_3 flow of 2100 sccm, pressure of 500 Torr, temperature of 950°C, and a growth rate of 2.0 μm/ hr. corresponding to a V/III ratio of 1710. First, a 2 μm-thick template layer ([Si] $=6\times 10^{17}cm^{-3}$) was grown as the base-line material to ensure proper morphology for the subsequent layers. An atomic force microscopy (AFM) was taken on a calibration sample with the same growth conditions which reveals ~1.0 nm root-mean-square (RMS) roughness. Subsequently, a 250 nm-thick n^{++} (([Si] $=5\times 10^{18}cm^{-3}$) layer which may constitute a top-side *n*-contact layer for purposes of lateral devices will be investigated in

Chapter 4. Next, the 5 µm-thick *n*-type drift region is grown using the minimum controllable *n*-type doping for the MOCVD system. A capacitance-voltage measurement on an additional calibration sample with these drift conditions revealed the carrier concentration of electrons to be $n_0 = 6\times 10^{16}\text{cm}^{-3}$. Now, the *n*-GaN part of the p-n diode structure is complete. The subsequent processes/treatments will intentionally attempt to introduce impurities at the top side interface of the aforementioned epitaxial layer. After this has been accomplished, the remaining *p*-GaN layers will be regrown. The regrowth/treated interfaces were placed directly at the metallurgical junctions between the n-GaN drift region and the p-GaN layers. Subsequent investigation of placement of the regrown interface away from the metallurgical junction will be presented in section 2.6. A schematic of the fabricated diodes with the placement of the regrowth interface and the 5 subsequent regrowth/treatments are shown in Figure 2.7.

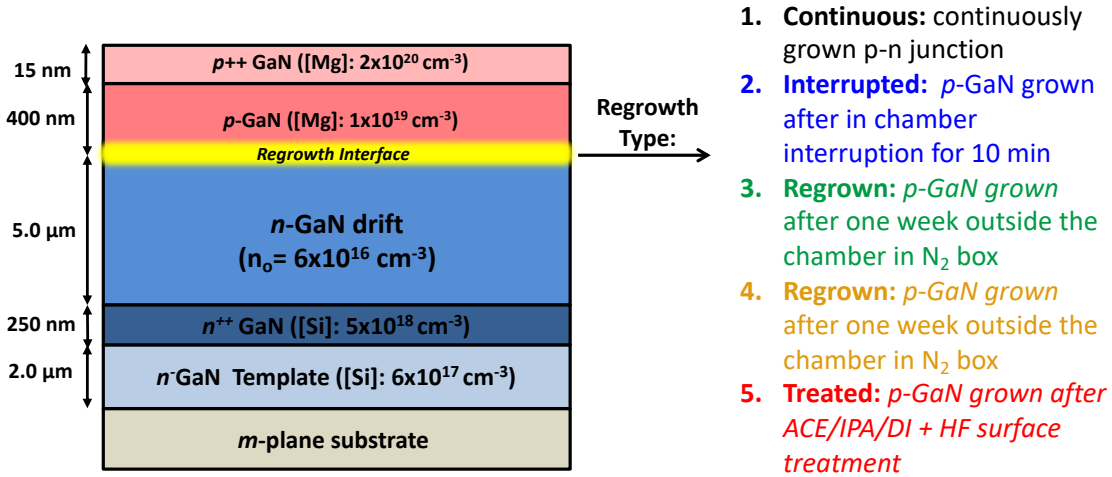

Figure 2.7: Epitaxial stack for regrown/treated vertical *m*-plane GaN *p-n* diodes showing the five different surface treatments done after *n*-GaN layers are grown

Five samples were grown: 1) continuously grown p–n diode; 2) regrown *p*-GaN grown after 1 week outside the chamber in N2 box; 3) regrown p-GaN grown after an in-chamber interruption for 10min; 4) regrown p-GaN grown after 1 week outside the chamber in N_2 box with N_2 blow; and 5) regrown p-GaN grown after the sample was exposed to acetone, isopropyl alcohol, and deionized (DI) water followed by hydroflouric acid (HF) and DI rinse. Sample 1 is used as the baseline for comparison between the subsequent treatments. The treatments in samples 2–4 were performed to replicate impurity incorporation at the regrown surface due to different exposure conditions. Sample 2 was intended to incorporate impurities from keeping the sample outside the chamber within a contained N2 purged box. Sample 3 was intended to incorporate impurities from within the chamber during a temperature cycle within the MOCVD. Sample 4 was intended to replicate incorporation due to keeping the sample outside the chamber within a contained N2 purged box along with a N2 blow that will bring impurities to the surface. The surface treatment for sample 5 was performed to observe if interfacial impurities associated with ACE/IPA/DI could be removed using HF.

Subsequent p-GaN layers are grown after the 5 previously mentioned interuptions/treatments. The *p*-type growth conditions consisted of: H_2 flow of 3500 sccm, NH_3 flow rate of 2000 sccm, pressure of 205 Torr, temperature of 835°C, and V/III ratio of 2560. The p-type dopant CP_2Mg is flowed along with H_2 in order to constitute the acceptor type doping. The layer constituting the *p*-GaN part of the *p*-*n* junction is grown with an intentional concentration of [Mg] =1×10^{19}cm^{-3} with a thickness of 400 nm. A highly doped p^{++}-type layer follows with an intentional concentration of [Mg] =1×10^{20}cm^{-3} which constitutes the *p*-contact layer of the diode. The sample is then annealed

at 700ºC for 15 min in order to activate the Mg atoms within the *p*-type layers. We will investigate the presence of the intentional interfacial impurities as a result of the interruption/treated regrowth process, and the effects they have on the electrical performance of the *p-n* diodes.

2.5 Fabrication of interrupted/treated vertical *m*-plane GaN *p-n* diodes

Descriptions of growth and interruptions/treatments for the 5 samples analyzed is discussed in the previous section (1.4). Further descriptions of the samples along with predominant impurity concentrations at the regrown junctions are given in Table 2.1 found in section 1.6. The 5 samples are fabricated into *p-n* diode device using standard photo-lithography, deposition, and dry-etching techniques. The samples were fabricated with circular Pd/Au (30/300 nm) metal layers deposited using electron-beam deposition to serve as *p*-contacts with a diameter of 350 μm. The diodes were isolated by circular mesas formed by an inductively coupled plasma (ICP) etcher with the following parameters: Cl2/Ar/BCl3 gas (20/5/10 sccm) at a pressure of 5 mTorr, radio frequency (RF) power of 25 W, and ICP power of 130 W. A backside large-area-contact of Ti/Al/Ni/Au (10/100/50/300 nm) was then deposited by electron-beam deposition to complete the process. Additional information regarding the sample fabrication and process is found in Appendix B. A schematic representation of the processed vertical *m*-plane GaN *p-n* diode is represented in Figure 2.8.

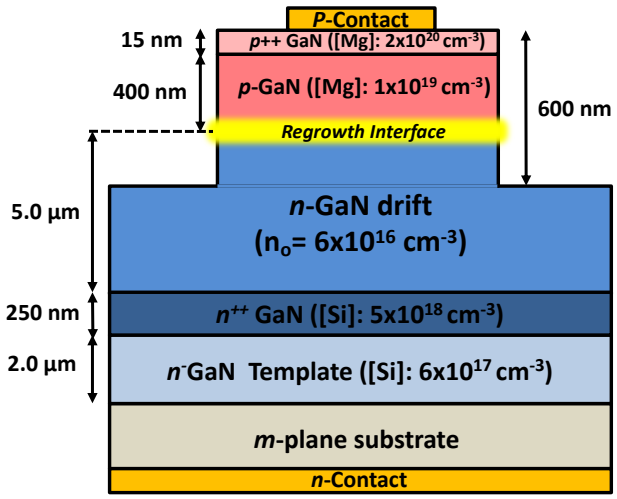

Figure 2.8: Cross-sectional schematic of the interrupted/treated vertical m-plane GaN p-n diode fabricated samples. Reprinted from [14], with the permission of WILEY-VCH Publishing.

2.6 Electrical Analysis of continuous and interrupted vertical *m*-plane GaN *p-n* diodes

An analysis of regrown nonpolar *m*-plane vertical *p-n* diodes will be presented which shows the benchmark devices which show the highest reverse blocking voltages obtained in this dissertation. Results, data, and images of this section are presented in the published work [11] . Forward and reverse current density-voltage (J-V) characteristics for continuously-grown (sample 1), interrupted (sample 2), and regrown (sample 3) *p-n* diodes are presented in Figure 2.9.a and b., respectively.

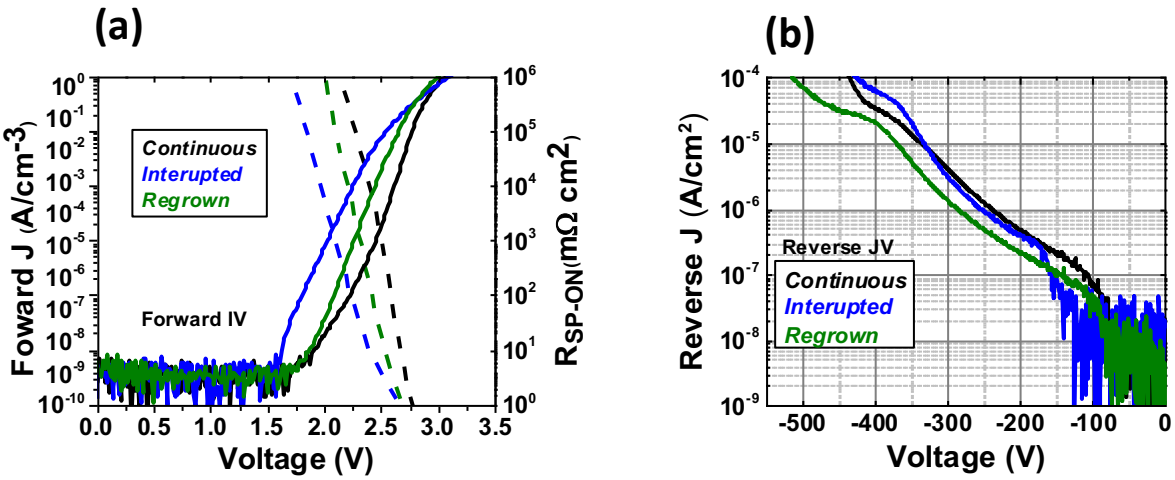

Figure 2.9: Current density-voltage curves of characteristics of selected GaN *p-n* diodes in a) Forward regime b) reverse regime.

Figure 2.9.a shows the forward *J-V* characteristics and specific on-resistances (R_{sp-on}) for continuously grown , interrupted, and regrown *p-n* diodes. The turn-on voltages are similar for each diode (~ 2.7-3.1 V). The specific on-resistance (R_{sp-on}) reaches 26-32 mΩ ·cm^2 at 5 A/cm^2 for all three diodes reduces, and reduces with increasing applied bias. At higher current density (J = 300 A/cm^2), the specific on-resistance reduces to ~ 1.7 mΩ.cm^2 (not shown in figure).

The Reverse *J-V* characteristics are show in Figure 2.9.b, with no direct indication of avalanche breakdown (no sharp increase in reverse leakage current) in any of the diodes. Reverse leakage is similar for all diodes below 200 V. Additionally, the breakdown voltages (Vb) are above 450 V, with Vb defined as the reverse voltage at 1 μA. The slight variations of reverse characteristics between the three samples can be related to variations in their drift layer properties. Specifically, V_b > 500 V was obtained for the regrown diode (sample 3). The effects of interfacial impurities on the electrical performance of these diodes will be presented in subsequent sections. Nevertheless, the

highest V_b = 540 V was obtained on the regrown diode (sample3). The corresponding maximum electric field was calculated to be E_{max} ~ 3.35 MV/cm at < 1 mA/cm^2 with the n-side depletion width of ~ 3.2 μm considering a one-sided junction approximation. Thus, a higher V_b can be enabled by a more lightly-doped and thicker drift region.

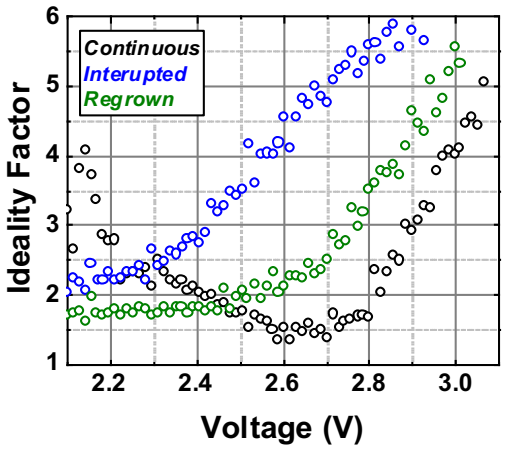

Figure 2.10: Ideality factor of selected GaN *p-n* diodes

The extracted ideality factor (n) is presented in Figure 2.10. The ideality factors are higher than 1 for all diodes which indicates non-ideal diode behavior due to Shockley-Read-Hall (SRH) dominant recombination currents in the space-charge region of the diodes [15]. The ideality factor n reduces with voltage (the ideal diffusion current starting to dominate the SRH current), with minimum values between 1.3-2.2 for the three diodes. At high biases, n increases due to series resistance [15]. The interrupted diode shows higher n, followed by the regrown and continuous diodes, indicating stronger SRH recombination current in the interrupted diode. At V < 1.5 V, the didoes show similar forward leakage current densities (< 10 nA/cm^2). However, the leakage current starts to deviate for the three diodes at higher voltages (> 1.5 V). The interrupted diodes show higher leakage current densities followed by the regrown and continuous

diodes. The interrupted diodes show over two orders of magnitude higher off-state leakage current density compared to the continuous and the regrown diodes. The forward characteristics contrast with the reverse bias characteristics where all the diodes show similar leakage current, suggesting that different mechanisms are responsible for forward and reverse leakage in these diodes. Additional investigation is needed to elucidate the sources of forward and reverse leakage in these diodes.

2.7 Interfacial impurities of interrupted/treated vertical *m*-plane GaN *p-n* diodes

Results, data, and images of this section are presented with the permission of WILEY-VCH and may found in the published work [14]. In order to understand the impacts of interfacial impurities (types and concentrations) on the diode performance, impurity levels using SIMS was conducted on all 5 of the previously mentioned samples. The detection limits (sensitivity) and depth resolution are the same as previously stated at: $Si = 3\times 10^{15}\text{cm}^{-3}$, $O = 1\times 10^{16}\text{cm}^{-3}$, $C = 5\times 10^{15}\text{cm}^{-3}$and 12.5 Å, respectively. Impurities between *n*-GaN and *p*-GaN may be easily resolved along with sharp spikes in impurities at the interface. The results of the SIMS impurity profiles of the 5 *p-n* diodes is presented in Figure 2.11 with the permission of WILEY-VCH Publishing from [14]. Each sample is placed next to each other for quick comparison with the same x-y axis dimensions, and the left-most position for each plot represents the topside surface of the *p-n* diode. Additionally, *p*-GaN and *n*-GaN regions are identified for each sample in each of the SIMS profiles.

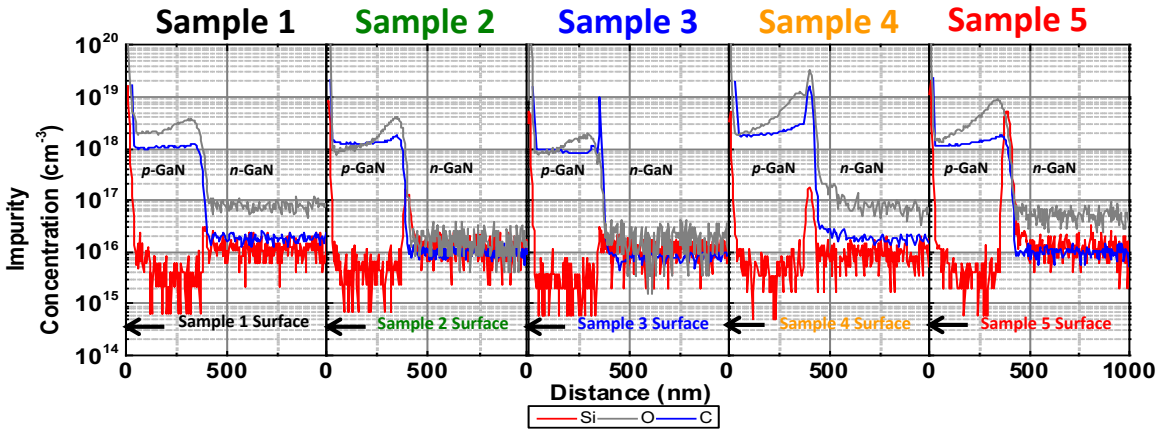

Figure 2.11: SIMS analysis of vertical m-plane GaN *p–n* diodes on 5 different samples with different interfacial impurity signatures. Reprinted from [14], with the permission of WILEY-VCH Publishing.

The impurity profile of Sample 1 (continuously grown sample) shows no significant spikes in Si, O, or C is at the within the sample. The background impurity concentration in the *n*-GaN region are: $Si \sim 1.0\times 10^{16}$cm^{-3}, $O \sim 7.4\times 10^{16}$cm^{-3}, $C \sim 1.8\times 10^{16}$cm^{-3}. A slight decrease is observed in the background Si concentration ($Si \sim 2.2\times 10^{15}$cm^{-3}) in the *p*-GaN region. We can identify the metallurgical junction at the position where the Si background profile drops from its nominal value in the n-type material to the p-type material at ~ 400 nm from the sample surface. A large increase near the sample surface is predominantly from ambient exposure. However, increases in background impurities O and C are observed in the *p*-GaN region with concentrations of $O\sim 1.9\times 10^{18}$cm^{-3} and $C \sim 9.5\times 10^{17}$cm^{-3}. This is expected from our investigation of *p*-type growth conditions in Section 1.3. The impurity O is observed to peak at a value of $O \sim 3.3\times 10^{18}$cm^{-3} at ~ 60 nm away from the metallurgical junction. A decreasing concentration attributed to diffusion is observed in the O profile away from this peak value. The length of this diffusion is observed to extend ~ 150 nm into the *p*-GaN region. However, the impurity concentrations of most significance are those exactly at the

metallurgical junction. Thus, the impurity concentrations for sample 1 at the metallurgical junction are identified: $Si \sim 2.9\times 10^{16}$cm^{-3}, $O \sim 6.9\times 10^{17}$cm^{-3}, and $C \sim 2.0\times 10^{17}$cm^{-3}.

The impurity profile of Sample 2 (regrown *p*-GaN grown after 1 week outside the chamber in N2 box) shows a significant spike in Si in the profile. The Si peak concentration is $Si \sim 1.6\times 10^{17}$cm^{-3} with a FWHM of ~ 25 nm. This spike indicates the location of the regrown interface and metallurgical junction of this sample at ~ 400 nm from the sample surface. The background impurity concentration in the *n*-GaN region are: $Si \sim 1.1\times 10^{16}$cm^{-3}, $O \sim 1.4\times 10^{16}$cm^{-3}, $C \sim 7.6\times 10^{15}$cm^{-3}. Again, a slight decrease is observed in the background Si concentration ($Si \sim 3.5\times 10^{15}$cm^{-3}) in the *p*-GaN region. Increases in background impurities O and C are also observed in the *p*-GaN region with concentrations of O~ 9.1×10^{17}cm^{-3} and $C \sim 1.2\times 10^{18}$cm^{-3}. Impurities O and C are observed to peak at a value of $O \sim 3.8\times 10^{18}$cm^{-3}and $O \sim 1.5\times 10^{18}$cm^{-3}at ~ 60 nm away from the regrown/metallurgical junction. Diffusion is observed in both O and C profiles away from their peak value. However, the effective diffusion length of the C (~75 nm) impurity is much less than that of O (~300 nm). Again, the impurity concentrations for sample 2 at the regrown/metallurgical junction are identified: $Si \sim 1.6\times 10^{17}$cm^{-3}, $O \sim 7.8\times 10^{17}$cm^{-3}, and $C \sim 3.9\times 10^{16}$cm^{-3}.

The impurity profile of Sample 3 (regrown p-GaN grown after an in-chamber interruption for 10min) shows a significant spike in the C profile. It may be noted that no Si spike is observed in this sample. The C peak concentration is $C \sim 9.9\times 10^{18}$cm^{-3} with a FWHM of ~ 6 nm. The C spike indicates the location of the regrown interface and

metallurgical junction of this sample at ~ 400 nm from the sample surface. The background impurity concentration in the *n*-GaN region are: $Si \sim 9.8\times 10^{15}$cm^{-3}, $O \sim 1.1\times 10^{16}$cm^{-3}, $C \sim 8.6\times 10^{15}$cm^{-3}. Again, a slight decrease is observed in the background Si concentration ($Si \sim 2.0\times 10^{15}$cm^{-3}) in the *p*-GaN region. Increases in background impurities O and C are also observed in the *p*-GaN region with concentrations of O~ 8.0×10^{17}cm^{-3} and $C \sim 8.4\times 10^{17}$cm^{-3}. The impurities O is observed to peak at a value of $O \sim 1.8\times 10^{18}$cm^{-3} at ~ 60 nm away from the regrown/metallurgical junction. A decreasing concentration attributed to diffusion is observed in the O profile away from this peak value which extends ~ 170 nm into the *p*-GaN region. The impurity concentrations for sample 3 at the regrown/metallurgical junction are identified: $Si \sim 2.9\times 10^{16}$cm^{-3}, $O \sim 6.2\times 10^{17}$cm^{-3}, and $C \sim 9.9\times 10^{18}$cm^{-3}.

Table 2.1. Description of interrupted/treated vertical m-plane GaN p-n diode samples.

Sample	Growth type	Treatment	Interfacial impurities [> 1×10^{18} cm^{-3}]
1	Continuous	N/A	N/A
2	Regrown	outside the chamber in N_2 box	N/A
3	Regrown	in chamber for 10 min	C
4	Regrown	outside the chamber in N_2 box + N_2 blow	C, O
5	Regrown	Ace/IPA/DI+ HF	C, Si, O

The impurity profile of Sample 4 (regrown p-GaN grown after 1 week outside the chamber in N_2 box) shows a significant spike in all impurity (Si, O, and C) profiles. The Si peak concentration is $Si \sim 1.7\times 10^{17}$cm^{-3} with a FWHM of ~ 33 nm. The O peak

concentration is $O \sim 3.2\times 10^{19}$cm^{-3} with a FWHM of ~ 45 nm. The C peak concentration is $C \sim 1.5\times 10^{19}$cm^{-3} with a FWHM of ~ 33 nm. The position of the spike indicates the location of the regrown interface and metallurgical junction of this sample at ~ 400 nm from the sample surface. The background impurity concentration in the *n*-GaN region are: $Si \sim 7.5\times 10^{15}$cm^{-3}, $O \sim 6.5\times 10^{16}$cm^{-3}, $C \sim 1.7\times 10^{16}$cm^{-3}. Again, a slight decrease is observed in the background Si concentration ($Si \sim 4.1\times 10^{15}$cm^{-3}) in the *p*-GaN region. Increases in background impurities O and C are also observed in the *p*-GaN region with concentrations of O~ 1.8×10^{18}cm^{-3} and $C \sim 1.7\times 10^{18}$cm^{-3}. Diffusion is observed in both O and C profiles away from their peak value. The effective diffusion length of the C (~160 nm) impurity is much less than that of O (~320 nm). The impurity concentrations for sample 4 at the regrown/metallurgical junction are identified: $Si \sim 1.7\times 10^{17}$cm^{-3}, $O \sim 3.2\times 10^{19}$cm^{-3}, and $C \sim 1.5\times 10^{19}$cm^{-3}.

The impurity profile of Sample 5 (regrown *p*-GaN) grown after the sample was exposed to acetone, isopropyl alcohol, and deionized (DI) water followed by hydroflouric acid (HF) and DI rinse) shows a significant spike in the Si profiles. The Si peak concentration is $Si \sim 5.2\times 10^{18}$cm^{-3} with a FWHM of ~ 29 nm. The position of the spike indicates the location of the regrown interface and metallurgical junction of this sample at ~ 400 nm from the sample surface. The background impurity concentration in the *n*-GaN region are: $Si \sim 1.1\times 10^{16}$cm^{-3}, $O \sim 5.1\times 10^{16}$cm^{-3}, $C \sim 9.4\times 10^{15}$cm^{-3}. Again, a slight decrease is observed in the background Si concentration ($Si \sim 2.8\times 10^{15}$cm^{-3}) in the *p*-GaN region. Increases in background impurities O and C are also observed in the *p*-GaN region with concentrations of O ~ 1.3×10^{18}cm^{-3} and $C \sim 1.1\times 10^{18}$cm^{-3}. The impurity O

is observed to peak at a value of $O \sim 8.6\times 10^{18}$cm^{-3} at ~ 50 nm away from the metallurgical junction. Diffusion is observed in both O and C profiles away from their peak value. The effective diffusion length of the C (~160 nm) impurity is much less than that of O (~280 nm). The impurity concentrations for sample 4 at the regrown/metallurgical junction are identified: $Si \sim 5.2\times 10^{18}$cm^{-3}, $O \sim 2.4\times 10^{18}$cm^{-3}, and $C \sim 1.0\times 10^{18}$cm^{-3}.

Now that the impurity profiles of the vertical *m*-plane GaN *p-n* diodes are analyzed, we will be able to understand the effects each have on the electrical performance of the devices. We will play close attention to the impurity concentrations at the regrown/metallurgical junction because at this point the internal electric field is highest during testing. Additional information on the impurity levels and profiles will be elaborated upon, as well. Nevertheless, we have observed the presence of impurities with the 5 test samples and have analyzed their profiles to identify the regrown/metallurgical junction and compared the differences in the background impurities levels between *n*-GaN and *p*-GaN.

2.8 Effects of interfacial impurities on the electrical performance of interrupted/treated vertical m-plane GaN p-n diodes

The effects of the interfacial impurities on the electrical performance of the 5 samples described in the previous sections will be investigated in this section. We will investigate the effects of impurity concentration and species on the forward and reverse operation regimes. Moderate levels of all species will be found to have a minimum effect on the diode performance in the forward and reverse. However, the performance of the diodes becomes compromised at higher interfacial impurity levels, and individual

impurities are concluded to have a different effect on the device performance in the forward and/or reverse regiemes.

The current density–voltage (*J–V*) characteristics of a single representative diode, out of approximately ten measured diodes on each sample, are shown in Figure 2.12. In the forward bias (Figure 2.12.a), all the samples showed very low off-state forward leakage (~1 nA/cm^2) below 1.5 V, except for sample 5. At higher voltages (>1.5 V) but still below turn-on, however, the off-state leakage currents differ for all the samples. All diodes showed similar turn-on voltages (~2.9 V). The extracted ideality factors (n) as a function of applied voltage for all diodes are shown in Figure 2.13. Nonideal diode behavior (n > 1) that often indicates Shockley–Read–Hall (SRH)- dominant recombination current within the depletion region of the diodes was observed [16].

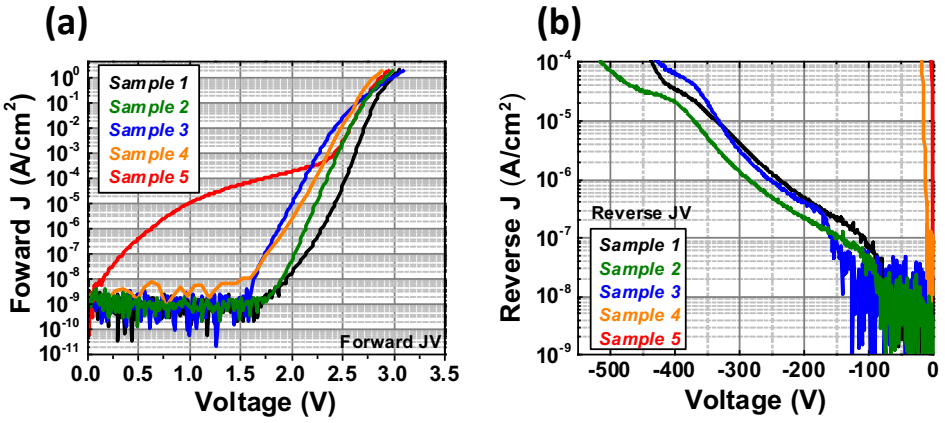

Figure 2.12: Current density-voltage curves of characteristics of selected interrupted/treated *m*-plane GaN *p-n* diodes in a) Forward regime b) reverse regime. Reprinted from [14], with the permission of WILEY-VCH Publishing.

At forward voltages below turn-on (~2.4 V), sample 5 may be strongly dominated by SRH (high n) leading to a higher forward leakage compared with the rest of the diodes. Below 1.5 V, the leakage was similar across all the diodes, except for sample 5. This may indicate an additional leakage mechanism attributed to the high Si spike

($Si \sim 5.2\times 10^{18}\text{cm}^{-3}$) in sample 5, which is not present in the other diodes. As the ideal diffusion current dominates the SRH current, n reduces to a minimum value (~1.5–2) for all diodes. However, at higher bias voltages (above turn-on), n is dominated by the diode series resistance and increases. Figure 2.12.b shows the reverse J–V characteristics of the samples. No direct indication of avalanche breakdown (i.e., sharp rise in current vs applied voltage) was observed for any of the samples. Significantly higher reverse leakage current densities for samples 4 and 5 compared with the other three samples are observed.

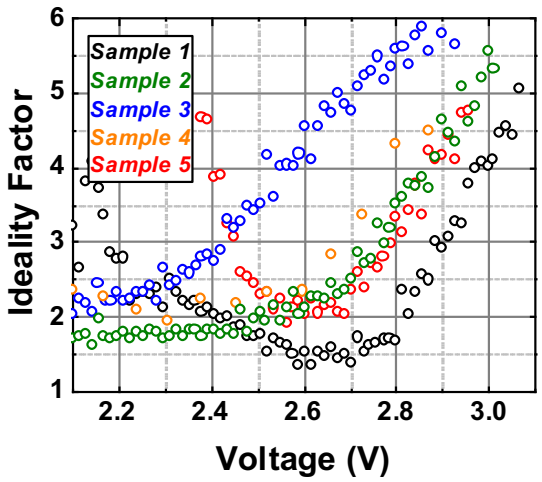

Figure 2.13: Ideality factor of selected interrupted/treated *m*-plane GaN *p-n* diodes. Reprinted from [14], with the permission of WILEY-VCH Publishing.

The *J–V* results are correlated with the impurity levels using the impurity profiles obtained from SIMS analysis to understand the impacts of interfacial impurities (types and concentrations) on the diode performance. The impurity profiles of the 5 samples were discussed in the previous section. Thus, the impurities between *n*-GaN and *p*-GaN may be resolved along with sharp spikes in impurities at the interface. The correlations between forward off-state leakage current (defined at forward current at 1.7 V), reverse blocking voltage (V_b) (defined as the reverse voltage at 1 μA/cm^2), and impurity

concentration at the interface are shown in Figure 2.14. The statistical (~ ten diodes per sample) forward off-state leakage current and reverse blocking voltage (V_b) are shown in Figure 2.14.a with error bars. The interfacial impurity concentration shown in Figure 2.14.b is defined as the peak of the impurity spikes observed at the regrowth interface in the SIMS data (Figure 2.11). The SIMS data was also separately analyzed by integrating over the spikes to obtain the total impurity concentration which produced similar trends.

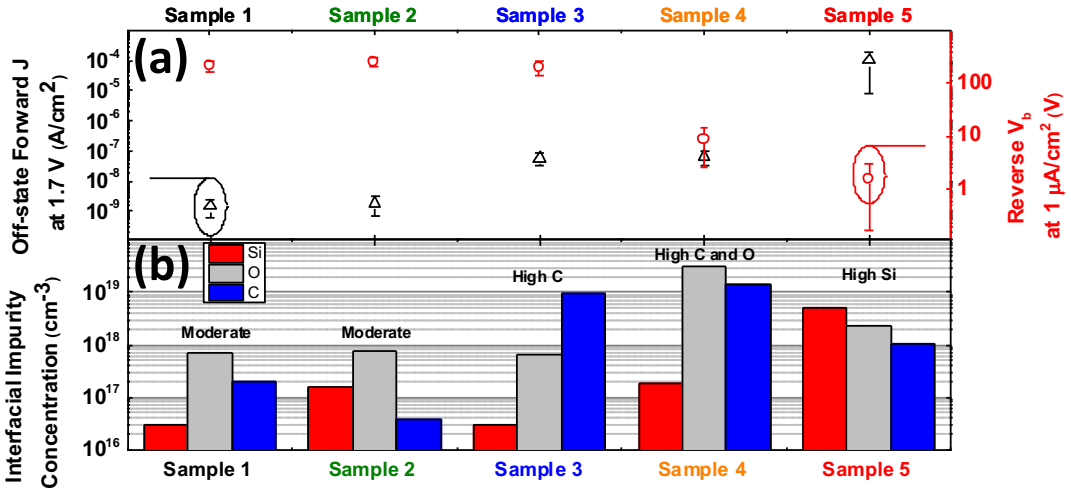

Figure 2.14. a) Vb and off-state forward current density at 1.7V, b) interfacial impurity concentrations (cm^{-3}) at the metallurgical junction.

The analysis reference samples 1 (continuously grown p–n diode) and 2 (regrown p-GaN grown after 1 week in N_2 box) showed that moderate levels of impurities (~ $5\times 10^{17} cm^{-3}$) at the junction yielded no significant degradation of the reverse (Vb > 200 V) and forward (<2 nA cm^2 off-state leakage at 1.7 V) characteristics. It is observed that the O levels within the drift region may differ by an order of 2.5 – 4 times. This difference was attributed to background impurity levels within the MOCVD at the time of growth. However, performance of the diodes was very similar which indicated that these differences in O within the *n*-GaN drift region did not degrade the device performance at

these O levels. Comparison of sample 3 (regrown p-GaN grown after an in-chamber interruption for 10 minutes and reference sample 1 (or sample 2) showed that high levels of carbon (~ $1\times 10^{19}cm^{-3}$) with moderate levels of silicon and oxygen (< $1\times 10^{18}cm^{-3}$) did not adversely affect the reverse blocking voltage (V_b > 200 V). However, the forward off-state leakage current was increased (from < 2 nA/cm^2 to ~ 60 nA/cm2 at 1.7V) compared with the reference sample 1. Sample 4 (regrown p-GaN grown after 1 week outside in N_2 box + N_2 blow) contained high levels of O and C, (~ $3\times 10^{19}cm^{-3}$ and ~ $1\times 10^{19}cm^{-3}$ respectively) with a moderate level of Si (~ $2\times 10^{17}cm^{-3}$). Comparison of sample 4 with the reference samples 1 and 3 indicated that the high level of oxygen (~ $3\times 10^{19}cm^{-3}$) or the combination of high oxygen and carbon was responsible for the degradation in the reverse performance, given that high levels of C impurities alone did not significantly alter the reverse characteristics. The reverse blocking voltage of sample 4 was reduced (V_b ~ 8.5 V) compared with the reference sample 1 (V_b > 200 V). The forward leakage (J = 60 nA/ cm^2 at 1.7 V) was similar to that of sample 3 with a similar C impurity level, but with a higher O level. Therefore, a high level of O was primarily responsible for a reduction in the reverse blocking voltage in sample 4. Sample 5 was characterized by a high level of Si (~ $5\times 10^{18}cm^{-3}$) with moderate levels of O and C (~ $2\times 10^{18}cm^{-3}$ and ~ $1\times 10^{18}cm^{-3}$, respectively). The blocking voltage of sample 5 was tremendously reduced (from Vb > 200 V to ~1.6 V) and the forward leakage was considerably increased (from <2 nA/cm^2 to ~100 $\mu A/cm^2$ at 1.7 V) compared with the reference sample 1.

Thus, we observed that large Si spikes strongly affect both forward and reverse characteristics of the diodes. Also, high carbon spikes at the junction affects primarily the

forward characteristics with high off-state leakage current in forward bias (~100x higher forward leakage current compared with a reference diode), whereas the reverse characteristics are not severely affected ($V_B > 200$ V at 1 μA/cm^2). High O spikes at the junction strongly affect the reverse blocking voltage ($V_b \sim 8.5$ V) compared with the reference sample 1 ($V_b > 200$ V) with nominal effect of the off-state forward current density. It is also shown that regrown diodes with impurity (Si, O, and C) levels below ($\sim 5\times 10^{17}$cm^{-3}) show comparable forward and reverse results with the reference continuously grown diodes. Thus, the effect interfacial impurities at the regrown junction of vertical m-plane GaN *p-n* diodes has been investigated with some key take-aways on impurity species incorporation and concentration.

2.9 Effects of regrown interface position on the electrical performance of interrupted/treated vertical m-plane GaN p-n diodes

The position of interfacial impurities with respect to the metallurgical junction on performance of vertical *m*-plane GaN *p-n* diodes is also investigated. The impurity interface is essentially 'buried' within the n^- GaN drift region prior to the growth of the metallurgical junction. By investigating this process, we seek to minimize the effect of interfacial impurities on the performance of the *p-n* diodes. In this section, three different vertical *m*-plane GaN *p-n* diode samples were grown on drift layers similar to those grown in the previous set (section 2.4). The epitaxial structure of the n-GaN layers is the exact same as that shown in Figure 2.8. However, the subsequent layers are as follows: i) p-GaN directly regrown on the drift layer; ii) 300nm n^- drift-GaN regrown prior to the p-GaN, and iii) 600 nm n^- drift-GaN prior to the p-GaN. The descriptions of the samples are shown in Table 2.2 and cross-sectional schematics of the epitaxial stacks are shown in

Figure 2.15. All the samples were treated with a consistent solvent cleaning of acetone, isopropyl alcohol, and a DI rinse prior to the regrowth to intentionally introduce impurities at the interface. Additionally, the fabrication process for these samples is the same as those in section 1.5.

Table 2.2. Description of vertical m-plane GaN *p-n* diode samples with metallurgical junction and regrowth interface separation.

Sample	Growth type	Junction And regrowth interface separation [nm]	Treatment	Interfacial impurities [$> 1\times10^{18}$ cm^{-3}]
i	Regrown	0	Ace/IPA/DI	Si
ii	Regrown	+ 300	Ace/IPA/DI	Si
iii	Regrown	+600	Ace/IPA/DI	Si

The SIMS impurity profiles of the three samples are presented in Figure 2.16. The positions of the regrowth interfaces with respect to the metallurgical junctions are identified by the sharp impurity spikes. Consistent Si spikes (~ $1\times 10^{18}cm^{-3}$) were observed at the regrown interfaces of all three samples. Other impurity levels (O and C) within the *n*-GaN drift region remained below $2\times 10^{17}cm^{-3}$ for all three samples. The O profile in the *p*-GaN layer of the direct p-GaN regrown diode (sample i) was consistent with all the previous diodes (samples 1–5) with the impurity interface at the metallurgical junction. Also, from the buried diodes (samples ii and iii), we observed an accompanying spike in O (~$1.4\times 10^{17}cm^{-3}$) along with the elevated Si spike at the regrown interface within the *n*-GaN. However, an increase in O within the p-GaN above 1×10^{18} cm^{-3} was not observed in the buried regrown diodes (samples ii and iii), but was observed in sample i. Therefore, samples i–iii were predominantly affected by Si due to consistent

higher concentration at the regrown junction (1×10^{18} cm^{-3}) along with O and C at the regrowth junction below levels (1×10^{18} cm^{-3}) previously shown not to affect diode performance (samples 1 and 2).

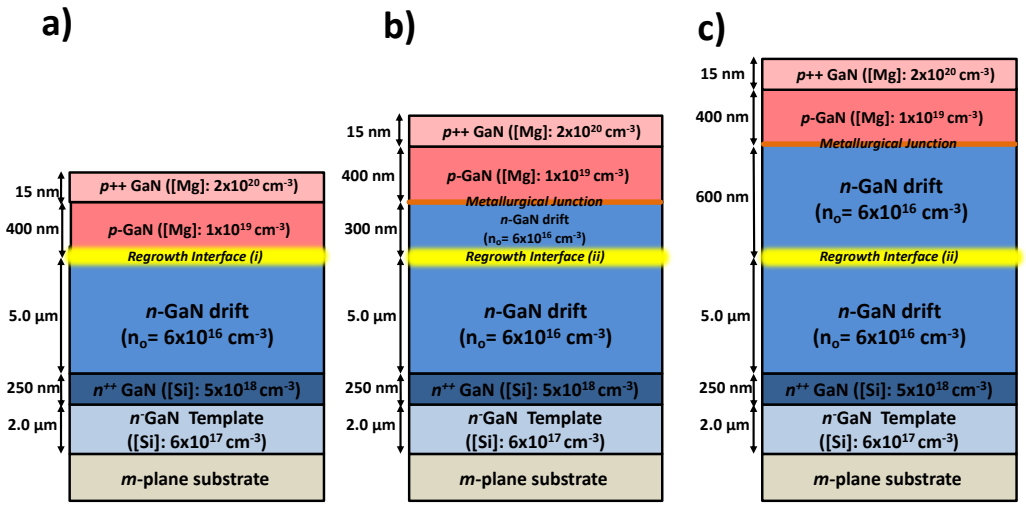

Figure 2.15. Cross-sectional schematic of vertical *p–n* diodes with metallurgical junction and regrowth interface separation of a) 0 nm) + 300 nm) + 600nm

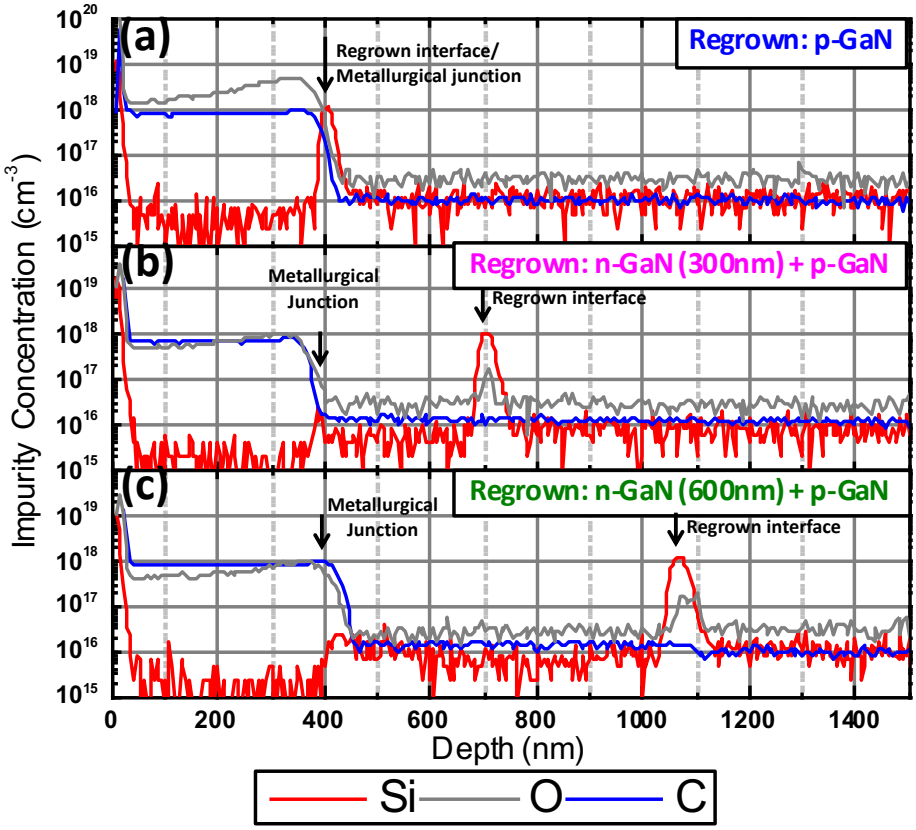

Figure 2.16. SIMS impurity profile of samples vertical *p–n* diodes with metallurgical junction and regrowth interface separation of a) 0 nm, b) + 300 nm, c) + 600nm

The forward and reverse electrical *J–V* characteristics of the three samples are shown in Figure 2.17, respectively. The *J–V* characteristics of the continuous diode (sample 1) from the previous section is also present in the plots for comparison. As expected, sample i shows significant forward leakage (~100 μA/cm^2 at 1.7 V) and a low Vb (<1 V). However, both samples ii and iii with impurity spikes buried below the junction show a significant reduction in the forward leakage (<2 nA/cm^2) compared with sample i, where the impurity spikes are located right at the junction. The behavior of the forward leakage of sample i was similar to that of sample 5 from the previous set (Figure 2.12.a) with a considerable leakage below turn-on, whereas samples ii and iii showed a similar forward leakage compared with the continuous sample 1 (Figure 2.12.a). The

forward leakage was mitigated because the depletion width on the *n*-side of the junction was less than 200 nm in forward bias, which was less than the thickness of the n^- GaN regrowth in both samples ii and iii. Therefore, the impurity spike was located outside the space charge region for samples ii and iii and did not have any adverse effect on forward J–V characteristics.

The ideality factors (n) as a function of applied voltage for the second set of samples are shown in Figure 2.18, indicating nonideal (n > 2) behavior with a minimum n ~ 1.8. Again, the similar trend in n versus voltage for samples ii and iii compared with the reference continuous sample 1 also supported the effectiveness of including n^- regrowth prior to *p*-GaN regrowth for forward characteristics. However, the ideality factor of sample i is severely affected by the increase leakage current below ~ 2.5V. Additional investigation of these types of leakage current will be presented in Chapter 4.

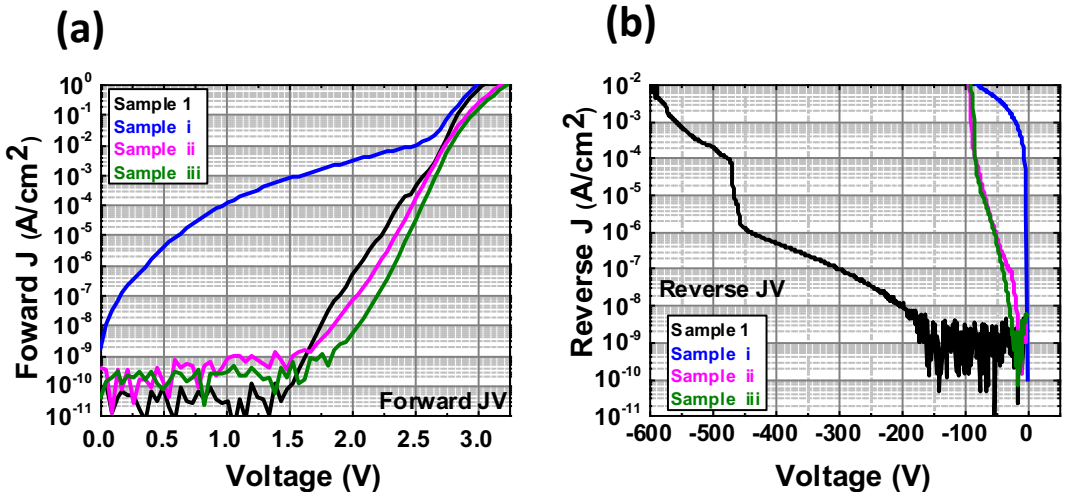

Figure 2.17. a) Forward J–V and b)reverse J–V characteristics samples vertical *p–n* diodes with metallurgical junction and regrowth interface separation.

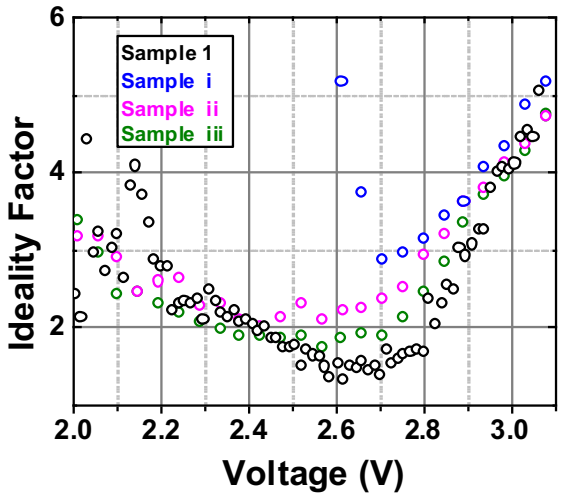

Figure 2.18. ideality factor as a function of forward voltages in vertical *p–n* diodes with metallurgical junction and regrowth interface separation.

In reverse bias, the behavior of the blocking voltage of sample i was also similar to that of sample 5 from the previous set (Figure 2.12.b) with a significantly reduced blocking voltage, whereas samples ii and iii showed a slightly improved blocking voltage compared with samples i and 5. The blocking voltage V_b was increased to 50 and 52 V for samples ii and iii, respectively. Although V_b was improved for samples ii and iii, it is still much lower than sample 1 (continuously grown sample) due to the presence of interfacial impurities. The effect of position of the junction with respect to the regrowth interface was more clearly observed if blocking voltage was probed at 10 nA/cm^2 instead of 1 μA/cm^2, where the n-side depletion width was approximately 750nm. The blocking voltages at 10 nA/cm^2 were approximately 1, 15, and 30 V for samples i, ii, and iii, respectively. Therefore, the high reverse leakage in regrown *p–n* diodes may also be mitigated by increasing the thickness of the regrown n-GaN region. However, typical selective-area-doped devices require only a few hundred nanometers of regrowth. Thus,

thicker n-GaN regrowth may not be practical as the depletion region quickly extends to several microns at large reverse voltages.

2.10 Effects of regrown interface position on the electric field of interrupted/treated vertical m-plane GaN p-n diodes

From the aforementioned discussion, interfacial impurity Si primarily led to degradation in regrown buried diode performance. Thus, electric field distributions over the depletion region of the three samples were calculated to understand the effects of Si on the critical breakdown field. It was previously observed that interfacial impurities at the interface of regrown junctions produced an increase in charged ionized donors, leading to an increased electric field at the junction of vertical regrown GaN diodes grown on the c-plane orientation [17]. The simulation considered the *p–n* doping profiles as seen in Figure 2.15 at a reverse bias voltage of 50V (approximate breakdown voltage of the regrown diodes). The results are shown in Figure 2.19. In this calculation, the Si spike (the primary impurity spike from the SIMS data in Figure 3) was inserted as a 20 nm delta-doped (1×10^{18} cm^{-3}) n-type GaN region at 0, 300, and 600 nm away from the metallurgical junction. A reference diode without a delta-doped region was also simulated to serve as a continuous diode without a Si impurity interface. The peak electric fields of the continuous diode and delta-doped diode at 0 nm away from the metallurgical junction were calculated to be ~1 and 1.3 MV/cm at 50 V reverse bias, respectively. Therefore, the presence of a doping spike associated with an interfacial Si impurity increased the peak electric field within the diode, but may not be directly

responsible for early breakdown because previously reported critical electric fields on regrown diodes were above 3.35 MV cm^{-1} [11].

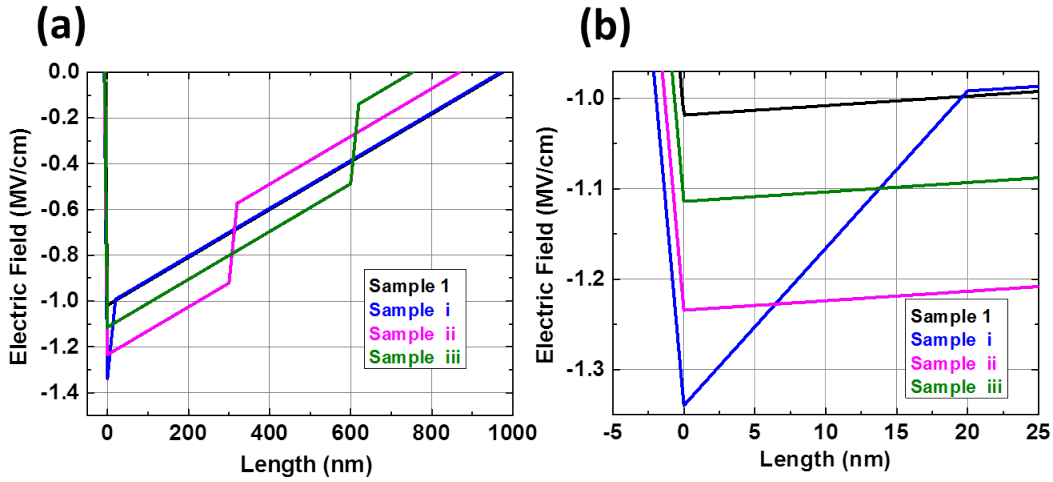

Figure 2.19. Calculated electric field distribution with a constant voltage of V_b = 50 V assuming delta Si doping (1× 10^{18} cm^{-3}) at 0, 300, and 600 nm away from the metallurgical junction a) expanded view (-50 nm to 1000 nm) b) zoomed view (-5 to 25 nm)

The peak electric field decreased when the delta-doped spike was buried further (+600 nm) in the *n*-drift GaN compared with the delta-doped diode at the metallurgical junction. The peak electric fields of the delta-doped diodes at 300 and 600 nm away from the metallurgical junction were calculated to be ~1.2 and 1.1 MV/cm at 50 V reverse bias. Thus, the peak electric field can be reduced in the presence of interfacial Si if it was considered completely ionized and the regrown interface was placed below the metallurgical junction. However, the assumption of complete interfacial Si ionization, which leads to larger peak electric fields, might not account entirely for the reverse leakage and early breakdown observed in our regrown diodes. For example, mid-gap C states may enhance the deep-level defect-assisted band-to-band tunneling [18], whereas shallow Si and O donors may contribute to carrier compensation [19]. Further

investigation in chapter 4 will elucidate the sources of forward and reverse leakage in these types of diodes.

2.11 Conclusion

In summary, we investigated impurities on growth-rate, intentional doping (impurity) control, interruptions, growth-type, and their presence at interfacial interfaces at and near the metallurgical junctions of vertical *m*-plane GaN *p–n* diodes. Our first consideration took into account the background impurity levels present at different growth rates. As the design architecture of vertical power electronics requires large drift regions, a quick growth-rate is necessary to insure reasonable throughput. An observed decrease in the incorporation of the impurity Si as growth rate increases is advantageous. However, increases in the impurities C and O are observed with increased growth rate. Therefore, a faster growth rate will introduce a trade-off between low Si impurity incorporation for marginal C and O incorporation. Thus, a growth rate of ~ 2.0 μm/ hr is chosen for epitaxial layers grown by MOCVD on *m*-plane GaN for the remaining studies.

The requirement for precise control of doping profiles was considered when implementing the low doped *n*-drift region which is critical to devices on GaN for power electronics. Thus, the minimum controllable carrier concentration achievable by the MOCVD used was found to be $n_0 = 1\times10^{16}cm^{-3}$. Doping profiles for *n*-type drift GaN below this value were observed to be sporadic and do not follow a linear trend with the SiH_4 flow rates introduced within the MOCVD

Interfacial impurities were explored with respect to growth types and growth interruptions. Calibration samples with several growth interruptions were grown for *n*-type and *p*-type conditions without the use of intentional doping for each. The background Si, O, and C concentration is also observed to be ~1.1×10^{16}cm^{-3} , ~1.5×10^{16}cm^{-3} , and 4.5×10^{15}cm^{-3} for *n*-type growth conditions. Spikes in Si and O are observed at positions corresponding to growth interruptions with an increase in concentration for interruptions for longer periods of time. For p-type growth conditions, the background Si, O, and C concentration is also observed to be ~3.1×10^{15}cm^{-3} , 2.9×10^{16}cm^{-3} , and ~ 7.8×10^{16}cm^{-3}, respectively. Spikes in Si and O are also observed at some positions corresponding to growth interruptions. However, the sporadic nature of the interfacial impurities is shown, as some of the positions don't possess a corresponding impurity spike.

Additionally, the effects of impurity species and concentrations on the forward/reverse electrical characteristics, including reverse blocking voltage, ideality factor, and off-state forward leakage current, reveals the impact of impurities on the diode performance. For example, a high C spike at the junction correlates with high off-state leakage current in the forward bias (~ 100× higher forward leakage current compared with the reference diode), whereas the reverse bias is not severely affected (V_b > 200 V). Also, high Si and O spikes at the junction strongly affect the reverse leakage currents (V_b ~ 1–10 V). Furthermore, the effect of the regrown interface position relative to the metallurgical junction on the diode performance was investigated. The adverse effects of induced impurities may be mitigated by repositioning the impurity spikes with respect to the depletion width as a function of applied voltage.

A significant reduction of the forward leakage (from J ~ 100 μA/cm^2 to J < 2 nA /cm^2 at 1.7 V) and an increase in the reverse blocking voltage (from V_b ~1V to Vb ~30V at 10nA/cm^2) is observed by separating the diode junction from the metallurgical junction. However, the reverse performance of the diodes with buried impurities was not comparable to that of the continuous diodes (V_b ~ 200 V at 10 nA /cm^2) due to the presence of interfacial impurities. The results contribute to understanding the effects of impurities on regrown diodes and provide design/epitaxial solutions to the interfacial impurity challenges in high-voltage selective-area- doped vertical p–n diodes.

Thus, a better understanding of impurities for several critical aspects of vertical power electronics on GaN has been investigated. The introduction of interfacial impurities on regrown junctions possesses a continuing challenge for the implementation of selectively-doped regions in GaN power electronics. By investigating this challenge, we are introduced to the challenges of increased leakage current and the reduction in blocking voltages on vertical m-plane GaN *p-n* diodes. The subsequent chapters will investigate other difficult challenges which are associated with the dry-etched enhanced damage on GaN.

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Chapter 3 Dry-etched enhanced damage: effects on planar *m*-plane diodes.

This chapter will cover the effect of dry-etched enhanced damage on planar vertical *m*-plane GaN diodes. A brief introduction to dry-etched enhanced damage was covered in section 1.4 and will be presented again here to gain some context before exploring deeper. The motivation of this body of work is to understand the challenges of implementing vertical selective-doped power electronics devices in GaN. An essential aspect of selective-doping , specifically, selective-area doping is to remove material from

a desired footprint in order to regrow within that region. The primary candidate to achieve this process is dry-etching. There are two primary means of removing material in dry-etching, namely sputtering and chemical processes. While these processes remove material, the leave behind a damaged surface. Since active removal of macro-amounts of material is occurring using an etch with significant physical component, it may be expected that the process yields some sort of damage to the resulting crystalline lattice. As will be presented subsequently, damage is present at the surface of the crystalline lattice and, below the surface, which leads to non-ideal surface for regrowth and propagation into the subsequently regrown material. Furthermore, crystalline defects can manifest into deep-level traps within the band gap of GaN. Spectroscopy will be used to identify these levels and their concentration, and their effects on the electrical performance will be presented.

An investigation of regrown and etched-and-regrown *m*-plane GaN vertical Schottky diodes by steady-state photocapacitance (SSPC) by comparing changes in the defect concentration relative to a continuously grown film, will be presented in the following sections. Material and data in this section is referenced from [1] with the permission of AIP publishing. It will be shown that elevated defect concentrations are localized at regrowth interfaces even without a plasma etch. Also, regrowth on dry-etched surfaces produced even higher peak defect concentrations near the regrowth interface, and elevated defectivity propagated into the regrown region. Post-etch surface treatment using AZ400K, prior to regrowth, reduced the defect concentration at the regrown interface. We also introduced a photoelectrochemical (PEC) wet etch treatment to remove dry-etch enhanced damage at the regrowth interface of the etched-and-regrown diodes.

The effectiveness of the PEC etch treatment in reducing the dry-etch enhanced damage near the regrowth interface was also investigated and compared with AZ400K. Furthermore, the concentration of a near-mid-bandgap defect level trended with reverse leakage, suggesting that this defect is a major contributor to diode leakage.

Additionally, etched-and-regrown *m*-plane GaN verical *p-n* diodes will be compared to the results of the deep level defects observed in the corresponding Shottky diodes mentioned above. The electrical characteristics will be comparted to the deep-level concentration in order to correlate their effects on forward leakage current and reverse blocking voltage. It will be observed that dry-etching significantly degrades these electrical properties. However, post-dry etch treatments will be shown to slightly mitigate these effects with a corresponding reduction in deep-level concentrations.

3.1 *m*-plane GaN vertical Schottky diodes for deep-level optical spectroscopy analysis

Thus far, we have investigated vertical m-plane GaN p-n diode structures for interfacial impurities at regrown junctions. However, the implementation of Schottky diodes in this section enables a more precise control over the depletion depth as a function of applied voltage. This will allow for precise depth resolution when conducting spatially varying optical spectroscopy, which will be elaborated in the following sections. Additionally, benefits of the Schottky diode arise due to the device unipolar device operation, which allows for detailed analysis of the majority carriers only.

GaN Schottky diode structures were grown through MOCVD on freestanding *m*-plane GaN substrate with a −0.95° miscut toward the minus *c*-direction from MCC with

n-type Si doping ($n_0 = 1 \times 10^{17}$ cm^{-3}). The small crystal off-angle minimizes the roughness of the overgrown GaN epilayer by mitigating pyramidal hillocks [2]. The epitaxial layers were grown at a pressure of 500 Torr using trimethylgallium (TMGa) and ammonia (NH_3) as precursors for elemental Ga and N, respectively. The n-type dopant is introduced using SiH4 diluted in nitrogen. The n-GaN layers are grown at a substrate temperature of ~960 °C measured by a pyrometer. The epitaxial growth consists of a 2-µm-thick *n*-type GaN buffer layer ([Si]: 6×10^{17} cm−3) followed by a 250-nm-thick n^+-GaN ([Si]: $\sim 5 \times 10^{18}$ cm^{-3}) and a subsequent 5-µm-thick lightly doped *n*-type GaN (with $N_D - N_A$: $\sim 6 \times 10^{16}$ cm^{-3}) to serve as a drift region. The net doping concentration ($N_D - N_A$) of the lightly doped n-GaN drift layer was found using a capacitance–voltage (*C–V*) evaluation on a separate calibration sample. Schematics of the Schottky diode structures are shown in Figure 3.1.

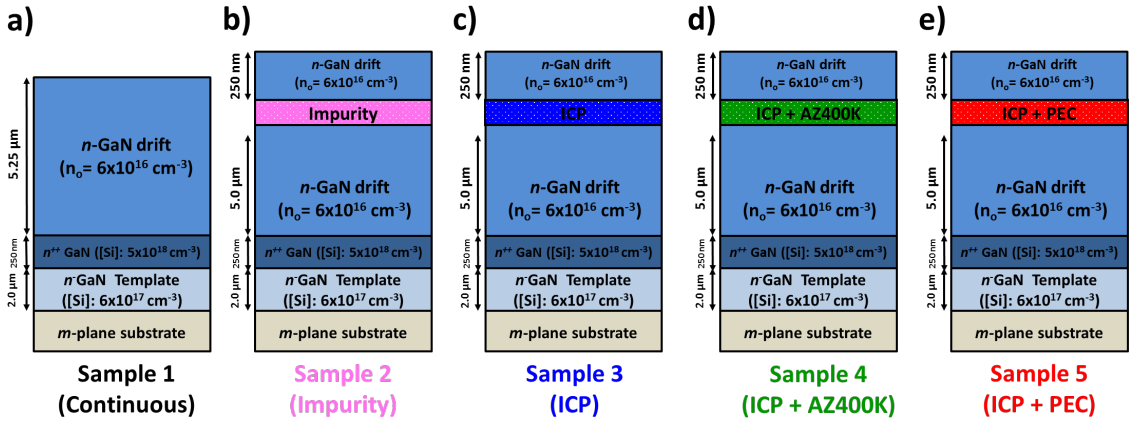

Figure 3.1. Schematic of vertical m-plane GaN Schottky didoes with the following surface treatment: a) continuously grown, b) impurity interface, c) ICP interface, d) ICP + AZ400K interface, e) ICP + PEC interface

A total of five samples with various treatments at the regrowth interface were studied. Sample 1 (reference sample) was continuously grown without any interruption,

etching, or surface treatment to serve as a reference baseline as-grown material for comparison. Sample 2 contained a regrowth interface without etching but with a solvent cleaning acetone/isopropanol/de-ionized water (Ace/IPA/DI) to intentionally introduce impurities at the regrowth interface. It may be mentioned that interfacial impurities such as Si, O, and C are known to affect the reverse and off-state forward leakage current (Chapter 2) as well as reverse blocking voltage of vertical p–n diodes [3]. Sample 3 was regrown after 400 nm of dry etching using a PlasmaTherm Apex SLR inductively coupled plasma (ICP) etcher, in which $Cl/Ar/BCl_3$ at a chamber pressure of 5 mTorr with an ICP power of 130W and a RF power of 30W were used. Additional information on ICP etching calibration is presented in Appendix B. Sample 4 was ICP etched using the same conditions as those for sample 3 but with a subsequent AZ400K treatment at 80 °C for 10 min prior to the regrowth. Sample 5 was also ICP etched (using the same conditions as those for samples 3 and 4) followed by a subsequent photoelectrochemical (PEC) etch (with an etch depth of 200 nm) in a 0.01M KOH in DI at room temperature with a mercury arc lamp positioned to have a surface flux of 100 mW/cm2. Additional information on PEC etching calibration is also presented in Appendix B. The samples in this study were not exposed to any acid treatments as we have observed that doing so has yielded higher impurity incorporation (Chapter 2) with an increase in Si (∼5 × 1018 cm−3), O (∼2 × 1018 cm−3), and C (∼2 × 1018 cm−3) at the regrown interface [3].

Atomic force microscopy (AFM) root-mean-square (RMS) surface roughness scans (20 × 20 μm^2) are shown in Figure 3.2.a–d of similarly grown m-plane GaN epilayers after the surface treatments. Above 1 nm, surface roughness is attributed to

~7.25 µm of GaN constituting the underlying n-type GaN buffer, n++-GaN layer, and n-type GaN drift regions.

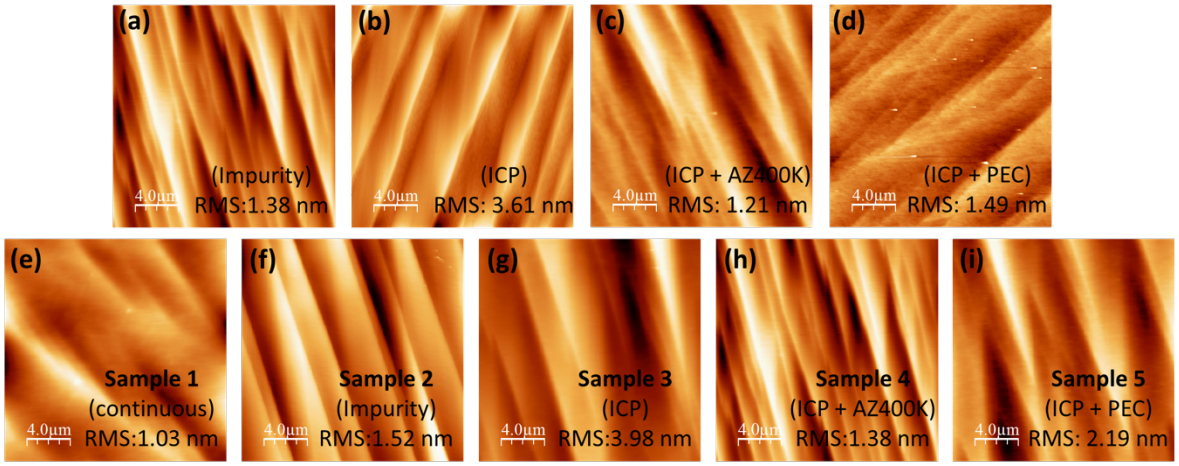

Figure 3.2 AFM images of the m-plane GaN surface after 7.25 µm of growth and subsequent a) impurity treatment, b) ICP etch, c) ICP etch and AZ400K treatment, d) ICP etch and PEC etch. AFM images before processing of: e) sample 1 continuous growth, f) sample 2 impurity + regrowth, g) sample 3 ICP etch + regrowth, h) sample 4 ICP etch + AZ400K treatment + regrowth, and i) sample 5 ICP etch + PEC etch + regrowth.

Variations in roughness are ascribed to differing treatments. A 250–500 nm *n*-type GaN ($n \sim 6 \times 10^{16}$ cm^{-3}) layer was regrown on samples 2–5 following the surface treatments. AFM surface roughness scans (20×20 μm^2) of all samples are shown in Figs. 3.2.e–i after regrowth. The morphologies are similar to the previous surfaces before regrowth with a slight increase in roughness due to regrowth.

3.2 Fabrication of vertical *m*-plane GaN Schottky diodes

Descriptions of growth and interruptions/treatments for the 5 samples analyzed were discussed in the above section (1.1). Further descriptions of the samples along with predominant deep level defect concentrations are given in Table 3.1 found in Section 3.11. The 5 samples are fabricated into Schottky diodes for steady-state photocapacitance

(SSPC) measurements using standard photolithography, and deposition techniques which have been discussed in Section 2.6. The samples were fabricated with semi-transparent Ni contacts with 9 nm thickness deposited by electron-beam deposition on the top side of the samples to serve as the Schottky contacts with a diameter of 350 µm. A backside large-area ohmic contact of Ti/Al/Ni/Au (10/100/50/300 nm) was then deposited by electron-beam deposition to complete the process. Additional information of sample fabrication and process is found in Appendix B, and a schematic representation of the processed vertical *m*-plane GaN Schottky diode is represented in Figure 3.3.

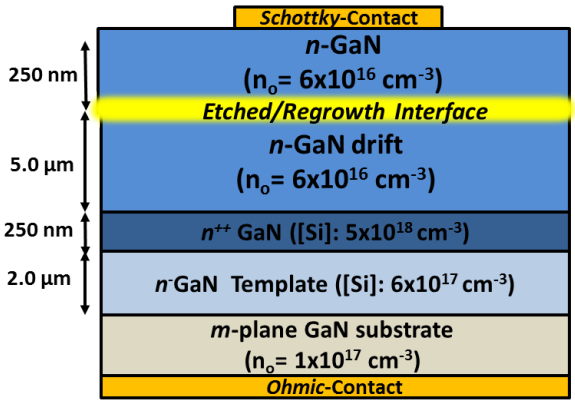

Figure 3.3: Cross-sectional schematic of fabricated etched-and-regrown vertical m-plane GaN Schottky diode. Reprinted from [1], with the permission of AIP Publishing.

3.3 Electrical characterization of vertical *m*-plane GaN Schottky diodes

The current density–voltage (*J–V*) characteristics of a single representative diode out of ~10 measured vertical m-plane GaN Shottky diodes on each wafer are shown in Figure 3.4.a. Statistical mean and standard deviation of ~10 measured diodes on each sample are shown in Figure 3.4.b at specific reverse and forward voltages of interest. According to the J–V results, the continuous reference sample (sample 1) shows the

lowest reverse leakage current of ~4 × 10^{-5} A/cm^2 at −10 V among all the samples tested and a turn-on voltage of 0.7 V. A comparison of *J–V* data between the continuously grown (sample 1) and the regrown (sample 2) diodes indicates the influence of a regrowth process (without an etch) on current leakage. Sample 2 shows an ~100× larger reverse J compared to that of the reference (sample 1) (~3 × 10^{-3} A/cm^2 compared to ~4 × 10^{-5} A/cm^2 at −10 V). A comparison of sample 3 shows the highest reverse leakage of ~3 × 10^{-2} A/cm^2 at −10 V of all samples with ~1000× increase in the reverse leakage compared to the reference (sample 1). The forward turn-on voltage of sample 3, however, is similar to that of the reference (sample 1) (0.7 V), indicating that dry-etch enhanced damage has a more prominent effect on the reverse characteristics than on the forward characteristics of the Schottky diodes. An additional testing of AZ400K wet-treated ICP etched and regrown diodes (sample 4) shows a reduction in the reverse J (~1 × 10^{-3} A/cm^2) compared to the ICP etched and regrown diodes (sample 3).

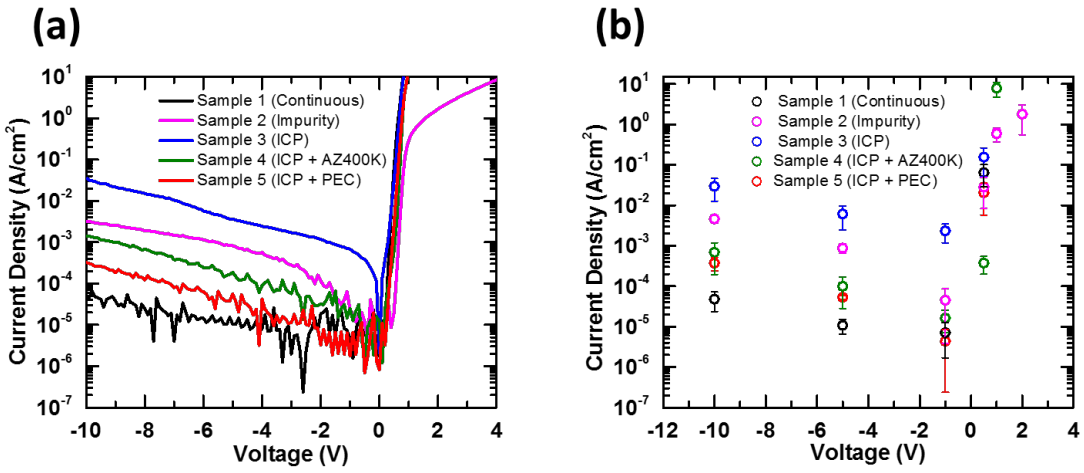

Figure 3.4: a) *J-V* characteristics of selected representative Schottky diodes from each sample. (b) *J–V* mean and standard deviation of statistical data. Reprinted from [1], with the permission of AIP Publishing.

Thus, the removal of ICP etched damage regions using AZ400K shows a slight improvement in the reverse blocking voltage. Further comparison of an ICP etched (sample 3) and subsequent PEC etched (sample 5) diode shows further reduction of the reverse J ($\sim 3 \times 10{-}4$ A/cm^2). The decrease in the reverse leakage current of sample 5 is attributed to the removal of the dry-etch enhanced damage using PEC and shows that PEC was more effective at reducing the reverse leakage current than by AZ400K. The forward turn-on voltage is similar (0.7–0.8 V) for all samples. However, sample 2 exhibits a higher R_{on} than the rest of the samples. From our previous work, we expect the highest concentration of interfacial impurities ($>1 \times 10^{18}$ cm^{-3}) at the regrown interface [3] . Complete ionization has not been confirmed, but the higher R_{on} may be attributed to impurity compensation which may affect R_{on}. The elevation in deep levels may also indicate other phenomenon such as increased recombination or trapping at the regrown junction which may also lead to higher R_{on}.

It may be observed that dry-etching and post-etch treatments have an effect on the *J-V* performance of the Schottky diodes. Therefore, we will identify the deep levels present within each sample using a steady-state photocapacitance (SSPC) analysis in the subsequent section. With this analysis along with the spatial distribution of the deep-levels we will be able to identify more precisely the effects of dry-etched and/or regrown interfaces on the electrical characteristics of these diodes, thus expanding our understanding of the leakage mechanisms at etched-and-regrown interfaces which play an integral part in selectively-doped power electronic devices.

3.4 Deep-level optical spectroscopy and steady-state photocapacitance

Steady-state photocapacitance [4] (SSPC) was used to examine the type of deep level defects and lighted capacitance–voltage (LCV) [4] was used to measure the depth profile of defect concentrations in the regrown diodes. All SSPC and LCV measurements were taken by our colleagues at Sandia National Laboratories, but the analysis is developed within this dissertation. SSPC uses monochromatic sub-bandgap-energy light to stimulate photoemission of carriers trapped at defect states in the depletion region of a diode. Upon photoemission, the carrier is swept out of the junction, and the remnant excess space-charge causes the depletion region to contract. The additional depletion capacitance is measured as a photocapacitance ΔC. When the energy of the mono-chromatic light becomes large enough to resonate with a deep level, thresholds appear in the SSPC spectrum at approximately $E_o–d_{FC}$, where E_o is the optical energy of the defect and d_{FC} is the Franck–Condon energy. The photon energy at which these thresholds occur is a hallmark of a defect. The saturation of the SSPC signal occurs at the bandgap energy. For the case of uniform doping, SSPC can quantify the deep level defect concentration (N_t). However, it was found in this study that the regrowth interface often was accompanied by a large spike in the doping. This rapidly varying doping concentration made conventional SSPC near the regrowth interfaces difficult from the standpoint of establishing N_t. Therefore, SSPC data are shown in as $\Delta C/C_0$ to focus only on defect energy thresholds.

Defect concentration was measured using LCV which measures the depth profile of a defect's concentration by measuring the increase in the apparent doping concentration when the deep level defect is photo-ionized by continuous wave (CW)

monochromatic illumination. A photon energy is chosen to cause photoemission of the defect with the lowest E_o, and the increase in the space-charge profile relative to that in the dark with all deep levels filled gives the N_t depth profile of that defect state. The extent of the measured depth profiles of capacitance–voltage (*C-V*) and lighted capacitance–voltage (*LCV*) were determined largely by the existence of (or lack of) a UID doping spike at the regrown interface. For the regrown samples without PEC etch, the large UID doping spike at the regrowth interface restricted the depletion region and, therefore, CV and LCV sensitivity to near the regrowth interface. For the regrown sample with the PEC etch, the UID doping spike was not evident, and this allowed the depletion region to move much deeper into the sample. For the case of multiple defect states, the measurement is repeated with successively larger photon energies chosen to optically excite defects one at a time.

SSPC and LCV measurements were performed at room temperature using a X_e arc lamp source filtered through a ¼ meter monochromator with mode-sorting filters to achieve monochromatic illumination from 1.20 to 3.50 eV at a photon flux of 5×10^{16} cm^{-2} s^{-1}. A collimating lens and a focusing lens were used to image the beam on the diode's semi-transparent Schottky contact. For SSPC, a measurement and fill pulse bias of 0 and +0.5V were used, respectively. LCV and SSPC measurements were taken at 1MHz. More information on SSPC and LCV can be found in Appendix C.

3.5 Deep level spectroscopy of continuous Schottky diodes

The SSPC spectrum of the continuously grown diode (sample 1) is presented in Figure. 3.5.a and is very similar to that of *c*-plane *n*-GaN grown on free-standing GaN [5]. Similar E_o values to those of [5] are adopted in this study; E_o = 1.9 eV, 2.9 eV,

and 3.3 eV were determined for the deep level signature between 1.20 and 2.60 eV, 2.60 and 3.20 eV, and 3.30 and 3.45 eV, respectively. The origin of the E_c – 1.90 eV deep level is likely related to a native defect caused by atomic displacement during growth [6]. Defect levels near E_c – 2.9 eV in n-GaN are associated with either C [7] or Ga vacancy, [8] and it is likely that both defect sources are present in the film. The E_c – 3.3 eV defect state is likely the same as a level at E_c – 3.28eV that is often ascribed to C impurities [9]. Previous reports on m-plane n-type GaN show a level at E_c – 3.31 eV, which was also attributed to C [10].

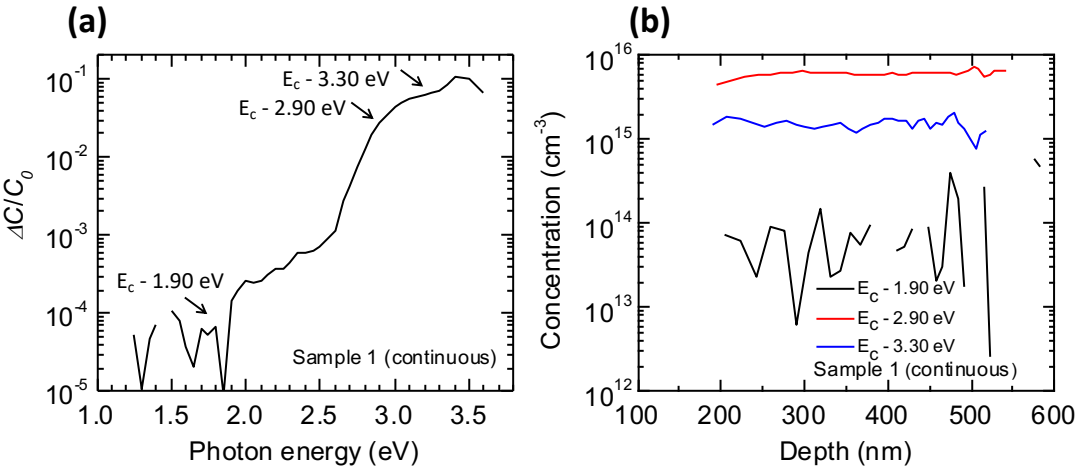

Figure 3.5 (a) SSPC spectrum and (b) depth profile of the continuously grown Schottky diode (sample 1). Reprinted from [1], with the permission of AIP Publishing.

The depth profiling of the deep levels for sample 1 using the LCV method is presented in Figure 3.5.b. Spatially uniform defect concentrations were observed for the as-grown *n*-type *m*-plane GaN, which is expected for a continuously grown film. The defect concentrations of the deep levels are similar to continuously grown *c*-plane oriented *n*-GaN on free-standing GaN substrates, [5] indicating that the concentration of point defects, and especially impurity-related defects, can be well controlled for epitaxial growth of *m*-plane GaN. The low defect density observed in the continuously grown

sample corresponds well with the observed lowest reverse leakage characteristic in the J–V results (~4×10^{-5} A/cm^2 at −10 V) among all the samples tested in this study [Fig. 3.4.a].

3.6 Deep level spectroscopy of regrown Schottky diodes

Spectroscopy of a regrown Schottky diode (sample 2) was also studied to investigate the role of interfacial impurities and regrowth without any dry etching on defect levels in GaN. The SSPC spectrum is shown in Figure 3.6.a with the net doping profile measured by *C–V* and the defect concentration profile measured by LCV in Figure 3.6.b. The SSPC spectrum in Figure 3.6.a was measured with a reverse voltage, $V_r = 0$ V, corresponding to a depletion region from 0 to 200 nm below the surface, i.e., 75 nm above the regrowth interface. The fill pulse (+0.5 V) was sufficient to reset the diode capacitance to near its dark value. The SSPC spectrum of the regrown diode (Figure 3.6.a) is qualitatively similar to that of the continuously grown diode (Figure 3.5.a), implying that the same type of deep level defects exist in both samples. However, the profile of these defect states in the regrown sample shows a strong depth dependence that is closely correlated to the regrowth interface. The doping profile shows a large spike at the depth of ~275 nm from the sample surface (Figure 3.6.b), corresponding to the regrowth interface. The spike in the doping profile of the regrown sample was previously correlated with Si and/or O impurity spikes buried at the regrowth interface [3]. The peak N_t for all observed deep levels exceeds 10^{17} cm^{-3} just above the regrowth interface (Figure 3.6.b.). However, only ~25 nm above the interface, N_t for the $E_c - 2.9$ and $E_c -$

3.30 eV defect levels reach those of the as-grown continuously grown diode (Figure 3.5.b.).

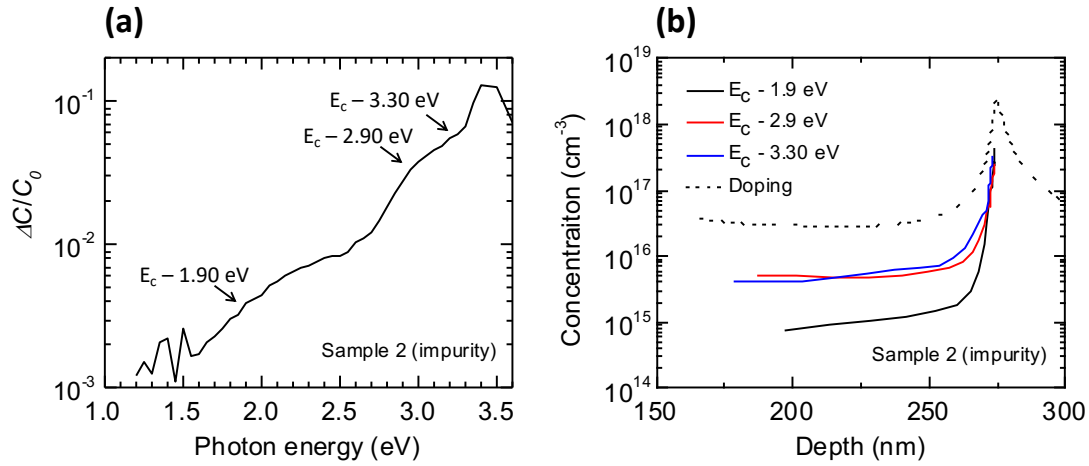

Figure 3.6 (a) SSPC spectrum and (b) depth profile of the regrown impurity Schottky diode (sample 2). Reprinted from [1], with the permission of AIP Publishing.

Considering prior impurity investigation of regrown m-plane GaN diodes indicating sharply peaked C concentration profiles at the regrowth interface, the observed trend here is also consistent with C related defects being the origin of the E_c – 2.9 eV and E_c – 3.3 eV levels [3]. The large-density of the E_c – 1.9eV level (relative to the continuously grown sample) persists even over 75 nm above the regrowth interface, suggesting that elevated concentration of this defect level propagates to the upper layers during the regrowth process. A possible scenario is that the thermal desorption during the substrate ramp up (prior to initiating the epitaxial regrowth) generates point defects at the regrowth interface, which may then diffuse to the upper layers.

A comparison of J–V data (Fig. 3.4.a) between the continuously grown (sample 1) and the regrown (sample 2) diodes shows an ~100× larger reverse J compared to that of the reference (sample 1), which is likely due to the increased concentration of the E_c – 1.9 eV deep levels. The E_c – 1.9 eV state is energetically located near midgap, which may

give rise to efficient band-to-band tunneling and increase both forward and reverse leakage [3,11]. Furthermore, the gradually "saturated" forward current from sample 2 after 0.5 V may also be attributed to the increased interfacial impurities. One possible mechanism for such a behavior is an increased recombination at the regrowth junction. Additional investigation of this leakage mechanism will be covered in Chapter 4. As the impurity spikes are highly localized to the regrowth interface, it may adversely affect the performance of regrown *p–n* diodes, especially if the regrowth interface is located right at the metallurgic junction, where the electric field is the highest [3].

3.7 Deep level spectroscopy of ICP etched-and-regrown diodes

The SSPC and LCV results of the baseline etched-and-regrown diode (sample 3) are presented in Figure 3.7. Similar to the regrown diode (sample 2), the etched-and-regrown diode (sample 3) also showed a spike in the doping at the regrowth interface. The depletion width was pinned at the regrowth interface, indicating an increase in $N_D - N_A$ near the regrown interface. The Si doping level was the same for all the structures ($\sim 6 \times 10^{16}$ cm^{-3}), which suggests that the deep level defect concentration exceeds that of Si throughout the regrown region. Thus, ICP etching appeared to greatly increase the defect levels for the etched-and-regrown sample (sample 3) compared to just regrowth without ICP etching (sample 2). The SSPC spectrum for the ICP etched-and-regrown diode shows the same deep-level defect signatures as the continuously grown and regrown (without etch) diodes. However, the LCV data reveal a significantly increased level of defect density near the etched-and-regrown interface of sample 3 compared to the reference and regrown only samples (samples 1 and 2). Thus, defects associated with

features from dry etching depend strongly on the depth away from the regrowth interface, which is also reported previously [12–14]. The peak concentrations of the E_c – 1.9 eV and E_c – 3.30 eV levels exceed 10^{18} cm^{-3} compared to ~10^{17} cm^{-3} for the regrown diode.

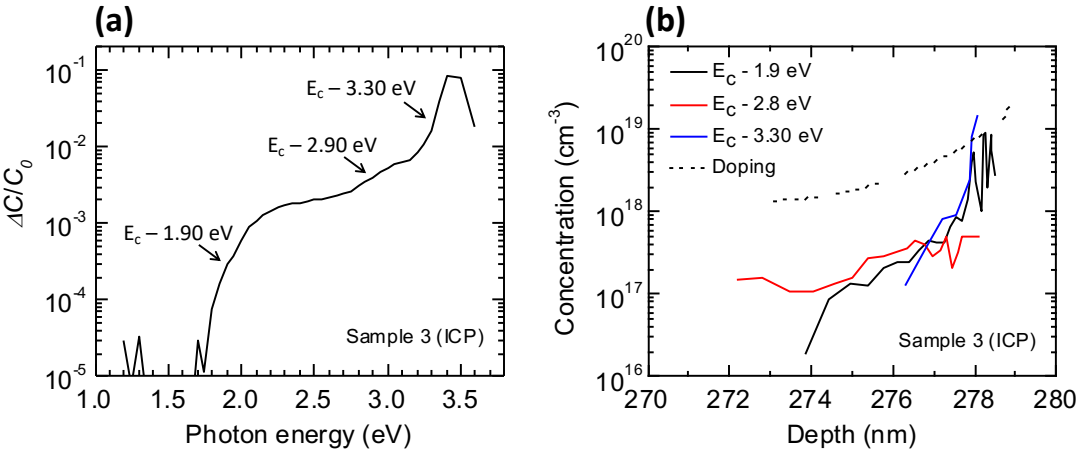

Figure 3.7 (a) SPPC spectrum and (b) depth profile of the ICP etched-and- regrown Schottky-diode (sample 3). Reprinted from [1], with the permission of AIP Publishing.

The defect concentration near the regrown surface could not be probed by LCV due to the fully depleted regrown drift region. However, the results from the regrown diode imply that the high concentration of the E_c – 1.9 eV relative to the nominal Si doping level persists well into the region above the regrowth interface. Dry etch subsurface damage has been previously shown to extend several hundred angstroms (500–600 Å) below the surface, which is attributed to the creation of nitrogen vacancy-related shallow donors [15–17]. However, due to the increased charge interface at the regrown interface, the depletion region was not able to extend into the sub-surface region below the regrown interface for analysis.

Electrical testing of sample 3 shows the highest reverse leakage of all samples. The interpretation of high defect density propagating to the surface is accompanied with

∼1000× increase in reverse leakage of sample 3 compared to the reference (sample 1) (Fig. 3.4.a).

3.8 Origins of ICP etched-and-regrown enhanced deep levels

The effects of dry-etch and regrowth on the electrical performance of diodes have also been reported on c-plane GaN [18–20]. Increased leakage current in *p–n* diodes grown on the c-plane in both the forward and reverse bias has been correlated with dry etch enhanced defects (E_c – 1.9 eV) [21]. The origin of the E_c – 1.9 eV level is likely to be an intrinsic point defect, considering that it exists at a low concentration in a continuously grown material, has elevated concentration at a non-plasma etched regrowth interface (where thermal desorption may occur), and an even larger concentration at a plasma-etched regrowth interface, given that atomic displacement from ion bombardment is likely to occur during any plasma-based dry-etching.

The gallium interstitial (Ga_i) has been suggested as the source for the E_c – 1.9eV deep level [5], as its density increase coincides with the emergence of point defect clustering during proton irradiation of *c*-plane *n*-GaN. Also, due to the relatively high mobility of Ga_i at room temperature [22], the point defect clustering may occur with a high probability considering Ga_i as the point defect.

3.9 Deep level spectroscopy of ICP etched-and-treated (AZ400K) diodes

The effect of a 10 min AZ400K at 80 °C treatment of the dry etched GaN material (sample 4) was also investigated to see whether the elevated defect levels could be mitigated near the regrowth interface. AZ400K is a KOH based solution that etches GaN

very slowly [23], but it could be sufficient to remove some surface defects. The results of SSPC (Figure 3.8.a) and LCV (Figure 3.8.b) of the ICP etched +AZ400K are shown. The same three defect levels as those for the other samples were observed in the SSPC spectrum. The peak N_t for all deep levels were drastically reduced for the ICP + AZ400K diode (sample 4) compared to the ICP baseline etched-and-regrown diode (sample 3) and were comparable to those for the regrown diode without ICP. The tail of the elevated defects from the regrowth interface into the bulk (Figure 3.8.b) was much longer for the ICP + AZ400K compared to the regrown without an etch sample. However, N_t for all deep levels reached the values observed in the reference continuously grown diode (sample 1). This is especially notable for the E_c – 1.9 eV deep level with a high N_t for the regrown sample (sample 2) compared to the reference (sample 1). This reduction in N_t for the E_c – 1.9 eV level explains the reduced reverse leakage for the ICP + AZ400K diode (sample 4) compared to the regrown diode without an etch (sample 2) (Figure 3.4.a).

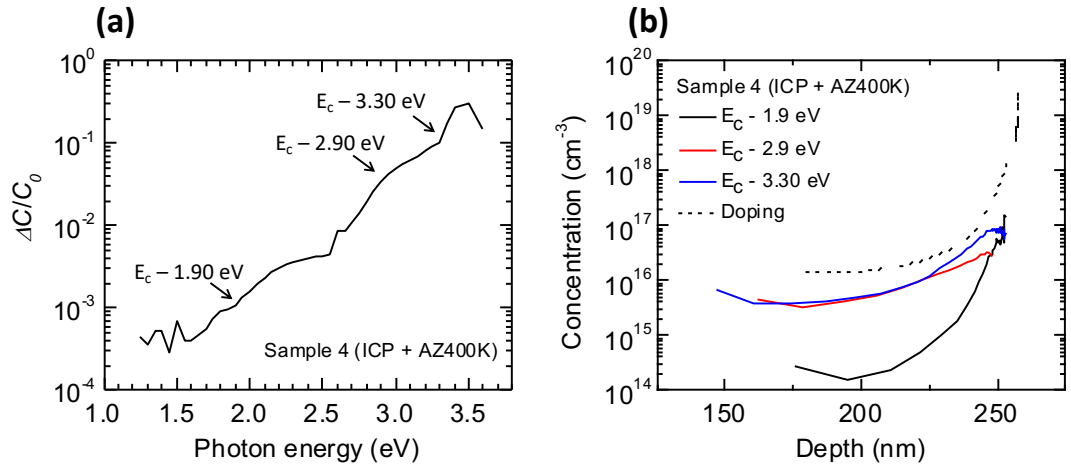

Figure 3.8. a) SSPC spectrum and (b) depth profile of the ICP + AZ400K etched-and regrown (sample 4). Schottky-diode. Reprinted from [1], with the permission of AIP Publishing.

3.10 Deep level spectroscopy of ICP + PEC etched diodes

As we have observed, ICP etching is likely to generate sub-surface damage via ion bombardment which may not be readily removed with etchants with slow etch rates, such as AZ400K. While our results show that AZ400K is marginally effective in reducing defect levels associated with regrowth, additional methods for removing dry etch enhanced damage should be investigated to reduce the defects further. PEC etching has previously been used to etch significant depths into GaN [24–27]. Therefore, it may be a suitable candidate for etching away damaged material caused by a dry etching process. For this purpose, the PEC etch rate was calibrated to approximately 2 nm/ min of n-GaN (6×10^{16} cm^{-3}) using 0.01M KOH in de-ionized (DI) water at room temperature with a surface flux of 100 mW/cm^2. More information on PEC etching and calibrations can be found in Appendix B.

The SSPC spectrum and depth profile of the ICP etched (200 nm deep) plus a subsequent PEC etching (400 nm deep) diode (sample 5) are presented in Fig. 7. The RMS roughness was measured after 400 nm of PEC etching using atomic force microscopy (AFM) to be ∼1.5 nm (Figure 3.2.d), which shows reduced roughness compared to an ICP etched only sample (Figure 3.2.b). The same group of deep levels was observed in the ICP + PEC sample as in the other samples in this study (Figure 3.9. .a). No doping spike at the regrowth interface (∼500 nm depth) was observed (Figure 3.9. .b) in the ICP + PEC sample (sample 5) using CV. However, the presence of Si (∼5 × 10^{17} cm−3) and O (∼6 × 1017 cm−3) “spikes” with a full width half max (FWHM) of ∼33 nm and ∼37 nm, respectively, is observed by secondary ion mass spectrometry (SIMS) in figure 3.10.

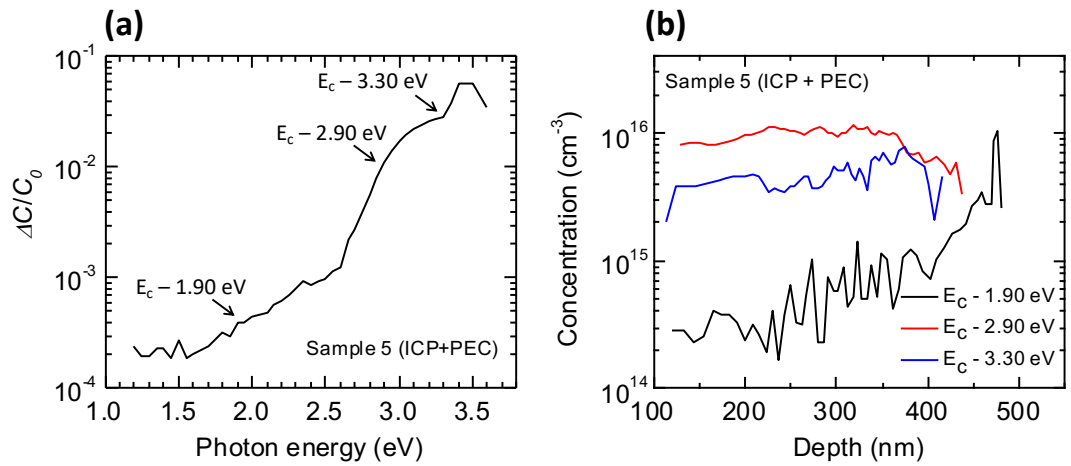

Figure 3.9. (a) SSPC spectrum and (b) depth profile of the ICP + PEC etched-and-regrown Schottky diode (sample 5). The depth profile in (b) is taken near the regrowth interface. Reprinted from [1], with the permission of AIP Publishing.

The detection limits (sensitivity) of the analysis are Si = 3 × 10^{15} cm^{-3}, O = 1 × 10^{16} cm^{-3} with a depth resolution of 12.5 Å. It is unclear whether the lack of a doping spike in *C-V* at the regrowth interface is a result of the PEC treatment or simply due to the sporadic nature of surface contamination by ambient exposure [3,11]. Interfacial impurities are likely to increase with ambient exposure and surface treatments. However, a lack of a doping spike (i.e., charge) does not necessarily indicate a lack of interfacial impurities as seen from the comparison of SIMS and *C-V*. Therefore, the interfacial impurities are not completely ionized. A defect profile comparison of the ICP + AZ400K (Figure 3.8.b) and ICP + PEC (Figure 3.9.b) shows that the latter has a slightly lower N_t for the E_c – 1.9 eV level in the bulk but much lower (~10^{16} cm^{-3}) N_t near the regrowth interface.

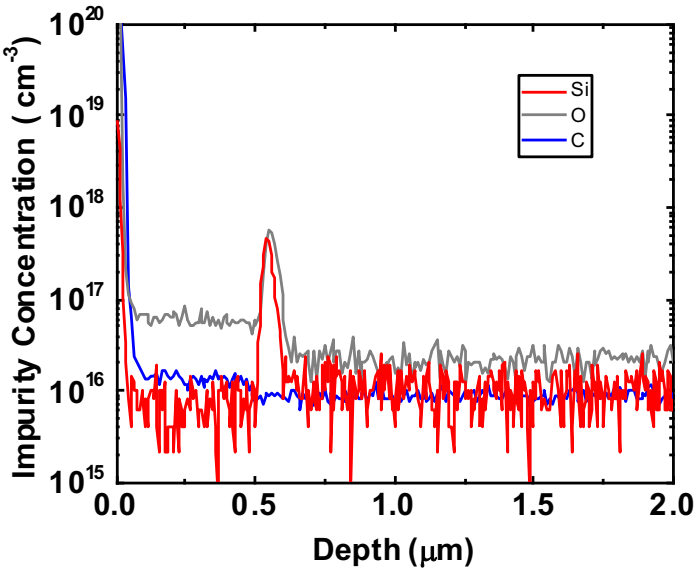

Figure 3.10. SIMS depth profile showing impurities Si, O, and C of the ICP + PEC etched-and-regrown Schottky diode (sample 5).

The decrease in the reverse leakage current of sample 5 (3×10^{-4} A/cm^2) as compared to the ICP etched only (sample 3)(3×10^{-2} A/cm^2) is attributed to the removal of the dry-etch enhanced damage based on the reduction of all deep levels in sample 6 compared to sample 3. Also, the E_c – 2.9 eV deep level is the highest N_t in the ICP + PEC diodes. Thus, the effect of this level is unlikely to contribute to the reverse leakage, as the ICP + PEC diodes coincide with the lowest reverse J compared to all other regrown samples (samples 2–4). This result is consistent with our previous report of a high-C interfacial layer which corresponds to the E_c – 2.9 eV deep level showing little effect on reverse leakage [3].

3.11 Summary of Deep level spectroscopy of Schottky diodes

A summary of the deep-level defect densities for all the samples investigated is presented in this section. Table 3.1 summarizes the deep-level defect densities for all the samples in this study near the regrown interface (close to the peak defect densities in the depth profile) and away from the interface in the bulk region, where the defect density spectrum is flat away from the tail regions of the interface. The regrown sample (sample 2) did not show significant enhancement in any of the three deep levels (namely, Ec – 1.9 eV, Ec – 2.9 eV, and Ec – 3.3 eV) in the bulk region, while a localized enhancement in the deep levels near the regrowth interface was observed. The ICP etched-and-regrown sample, on the other hand, shows a significant enhancement of all the three deep levels in the bulk and near the regrowth interface. AZ400K (sample 4) and PEC (sample 5) treatments both significantly reduce the deep-level defect densities away from the regrown interface down to the levels close to those for the reference continuously grown sample (sample 1). The main difference between samples 4 and 5 is that localized defects near the regrowth interface were largely eliminated in the PEC treated sample (sample 5).

Table 3.1 Summarized deep-level defect density results for all the samples investigated. Reprinted from [1], with the permission of AIP Publishing.

Sample #	Surface Treatment	Above Regrown Interface			Near Regrown Interface		
		E_c - 1.9 eV ($\times 10^{14}$ cm^{-3})	(E_c – 2.9 eV) ($\times 10^{14}$ cm^{-3})	(E_c – 3.3 eV) ($\times 10^{14}$ cm^{-3})	(E_c - 1.9 eV) ($\times 10^{14}$ cm^{-3})	(E_c – 2.9 eV) ($\times 10^{14}$ cm^{-3})	(E_c – 3.3 eV) ($\times 10^{14}$ cm^{-3})
1	N/A	1	30	70	N/A	N/A	N/A
2	Ace/IPA/DI	2	20	30	2,000	1,600	3,300
3	ICP (400 nm)	10	200	1,000	85,600	5,030	81,600
4	ICP (400 nm) + AZ400K	1	30	30	300	300	800
5	ICP (400 nm) + PEC (200 nm)	4	90	30	30	50	70

In addition, the ICP + PEC (sample 5) and the regrown without an etch (sample 2) samples have similar N_t for the E_c – 1.9 eV level in the regrown bulk, while the latter shows > 10× higher leakage. Hence, the large spike in E_c –1.9 eV defect N_t (> 10^{17} cm^{-3}) for the regrown diode (and missing for the ICP + PEC sample), is likely to be the main contributor to leakage rather than background levels $N_t \sim 10^{15}$ cm^{-3} in the regrown bulk. The ICP + PEC sample also shows a lower N_t for the E_c – 1.9 eV level near the regrown interface even when compared to the regrown sample without a plasma etch, which may imply that the PEC not only removes dry-etch enhanced damage, but also may provide an epitaxial surface that is less susceptible to the formation of defects during the regrowth process. PEC may also be considered to replace the dry-etch process to define the selective-area regrown region as it introduces significantly reduced levels as compared to ICP etching. However, PEC etching is not able to fully eliminate dry-etch enhanced defect levels. Also, the concentration of the E_c – 2.9 eV level in the bulk is a bit higher, while the E_c – 3.3 eV concentration is almost the same in sample 5 compared to other samples. The wet treatment methods suggested in this work (both AZ400K and PEC) enable reduced damage, while maintaining smooth epitaxial-ready surfaces.

In summary, SSPC was performed on etched-and-regrown *m*-plane *n*-type Schottky diodes. As-grown levels were identified at E_c – 1.9 eV, E_c – 2.9 eV, and E_c – 3.3 eV with concentrations below $N_t \sim 10^{16}$ cm−3. The origin of the E_c – 1.9 eV level is likely to be an intrinsic point defect introduced during growth where thermal desorption may occur. Defect levels near E_c – 2.9 eV are associated with either C or Ga vacancies, and the E_c – 3.3 eV defect state is likely ascribed to carbon impurities. In addition, localized levels associated with impurities and regrowth were observed for regrowth

without an etch. However, by introducing an ICP etch process before regrowth a ∼100, 000× increase in the E_c – 1.9 eV level with an emergent E_c – 3.3 eV level as compared to as-grown materials is observed near the regrowth surface. Thus, atomic displacement from ion bombardment is likely to occur during any plasma-based dry etching resulting in an even larger defect concentration at a plasma-etched regrowth interface. Depth profiling shows that the effect of these plasma enhanced defects are not localized and may propagate several hundred nanometers away from the etched interface. This is indicated by an observed tail for all defect levels. Further, JV testing confirms the effect of these elevated levels as leakage current was ∼1000× higher as compared to the as-grown material. Therefore, wet treatments were investigated to mitigate the elevated defect levels enhanced by dry etching. An AZ400K dip was introduced after ICP etching due to its ability to slowly etch GaN. The deep levels were significantly reduced near the regrown interface along with an ∼100× reduction in reverse leakage current compared to the ICP-etched only sample. An observed tail of the elevated defects from the regrowth interface into the bulk was again observed indicating only a partial mitigation of the dry-etch enhanced damage. Thus, a PEC wet-etch treatment after ICP-etching was investigated due to its ability to etch GaN at a higher rate than AZ400K. It was observed that the subsequent PEC treatment reduced the E_c – 1.9 eV level. Reverse leakage was also reduced by ∼1000× compared to the ICP-etched only sample. No observable tail in the depth profiling indicated that the deep levels enhanced by ICP etching did not propagate away from the regrowth interface in the ICP + PEC sample. Therefore, the wet treatment methods suggested in this work (both AZ400K and PEC) enable mitigation of ICP dry-etch enhanced damage on n-type m-plane GaN, while maintaining smooth

epitaxial-ready surfaces. Similar wet-etching methods have been implemented on the c-plane and are part of on-going investigation on etched-and-regrown *c*-plane diodes. By providing solutions to dry-etched enhanced damage using wet-treatments, the next generation of selective-doped high-power vertical electronics devices on GaN may be realized.

3.12 Etched-and-regrown *m*-plane GaN vertical *p-n* diodes

Thus far, we have investigated vertical *m*-plane GaN Schottky diode structures for investigation of dry-etched enhanced damage at, below, and above the regrowth junction. From the analysis of *J-V* and SSPC, we have attributed current leakage to deep level traps located within the ICP-etched and regrown Schottky diodes. We have also seen the reduction of deep levels through surface treatment AZ400K and subsequent PEC etching with associated reduction in current leakage. Therefore, the implementation of these treatments/etches will be investigated on vertical *m*-plane GaN *p-n* diodes. The results will indicate similar benefits from the transition of the processes in terms of *J-V* performance. However, complete reduction of leakage current is not achieved in comparison to continuously grown *p-n* diodes. Challenges associated with complete damage mitigation and the removal of interfacial impurities continue to persist and is the object of further investigation. Nevertheless, the results of etched-and-regrown *m*-plane GaN vertical *p-n* diodes is presented in this section.

GaN *p-n* diode structures were grown through MOCVD on freestanding *m*-plane GaN substrate with a −0.95° miscut toward the minus *c*-direction from MCC with *n*-type Si doping ($n_0 = 1 \times 10^{17}$ cm^{-3}). The epitaxial layers were grown at a pressure of 500 Torr

using trimethylgallium (TMGa) and ammonia (NH_3) as precursors for elemental Ga and N, respectively. The n-type dopant is introduced using SiH_4 diluted in nitrogen. The n-GaN layers are grown at a substrate temperature of ~960 °C measured by a pyrometer. The epitaxial growth consists of a 2-µm-thick *n*-type GaN buffer layer ([Si]: 6×10^{17} cm−3) followed by a 250-nm-thick n^+-GaN ([Si]: ~5×10^{18} cm^{-3}), and a subsequent 5-µm-thick lightly doped *n*-type GaN (with N_D-N_A: ~6×10^{16} cm^{-3}) to serve as a drift region. The net doping concentration (N_D-N_A) of the lightly doped *n*-GaN drift layer was found using a capacitance–voltage (*C–V*) evaluation on a separate calibration sample. Schematics of the *p-n* diode structures are shown in Figure 3.11.

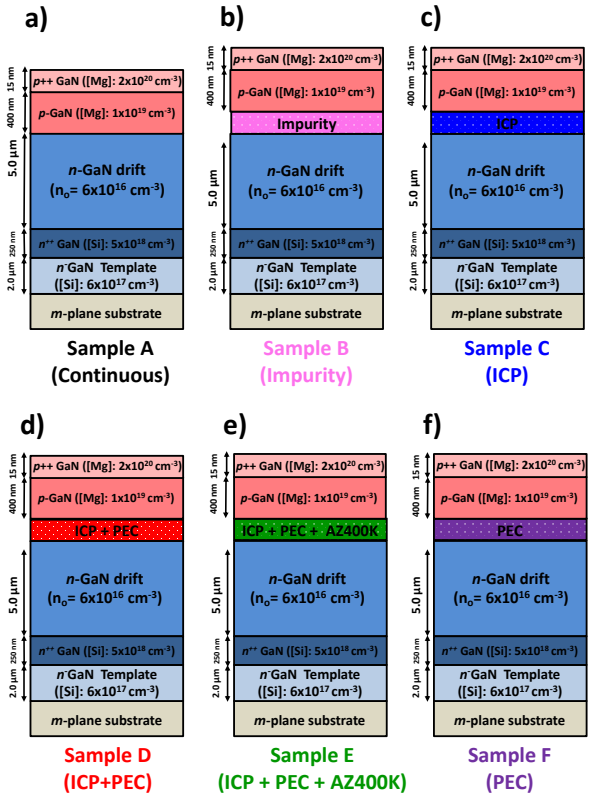

Figure 3.11. Schematic of vertical m-plane GaN *p-n* didoes with the following surface treatment: a) continuously grown, b) impurity interface c) ICP interface, d) ICP + PEC interface, e) ICP + PEC AZ400K interface, f) PEC interface

A total of 6 samples with various treatments at the regrowth interface were studied. Sample A (reference sample) was continuously grown without any interruption, etching, or surface treatment to serve as a reference baseline as-grown material for comparison. Sample B is the same as (sample 5) from section 2.4 of the previous chapter. It was regrown after the sample was exposed to acetone, isopropyl alcohol, and deionized (DI) water followed by hydroflouric acid (HF) and DI rinse, and constitutes the baseline impurity sample. Sample C was regrown after 200 nm of dry etching using a PlasmaTherm Apex SLR inductively coupled plasma (ICP) etcher, in which Cl/Ar/BCl3 at a chamber pressure of 5 mTorr with an ICP power of 130W and a RF power of 30W were used. A subsequent hydrofluoric acid (HF) dip was performed for 1 min followed by DI rinsing. Sample D was ICP etched using the same conditions as those for sample C followed by a photoelectrochemical (PEC) etch (with an etch depth of 500 nm) in 0.01M KOH in DI at room temperature with a mercury arc lamp positioned to have a surface flux of 100 mW/cm^2 along with a subsequent HF + DI dip is performed as well. Sample E was also ICP + PEC etched (using the same conditions as those for samples C and D) followed by an AZ400K treatment at 80 °C for 10 min with a subsequent HF + DI dip prior to the regrowth. Sample F was regrown after 200 nm of PEC etching only with a subsequent HF + DI dip prior to the regrowth.

The *p*-GaN layers are grown after the 5 previously mentioned etches/treatments. The *p*-type growth conditions consisted of: H_2 flow of 3500 sccm, NH_3 flow rate of 2000 sccm, pressure of 205 Torr, temperature of 835°C, and V/III ratio of 7020. The p-type dopant Cp_2Mg is flowed along with H_2 in order to constitute the acceptor type doping. The layer constituting the *p*-GaN part of the *p*-*n* junction is grown with an intentional

concentration of [Mg] =1× 10^{19}cm^{-3} with a thickness of 400 nm. A highly doped p^{++}-type layer follows with an intentional concentration of [Mg] =1× 10^{20}cm^{-3} which constitutes the *p*-contact layer of the diode. The sample is then annealed at 700ºC for 15 min in order to activate the Mg atoms within the *p*-type layers. Atomic force microscopy (AFM) root-mean-square (RMS) surface roughness scans (20 × 20 μm^2) are shown in Figure 3.12 of the top-side m-plane *p*-GaN.

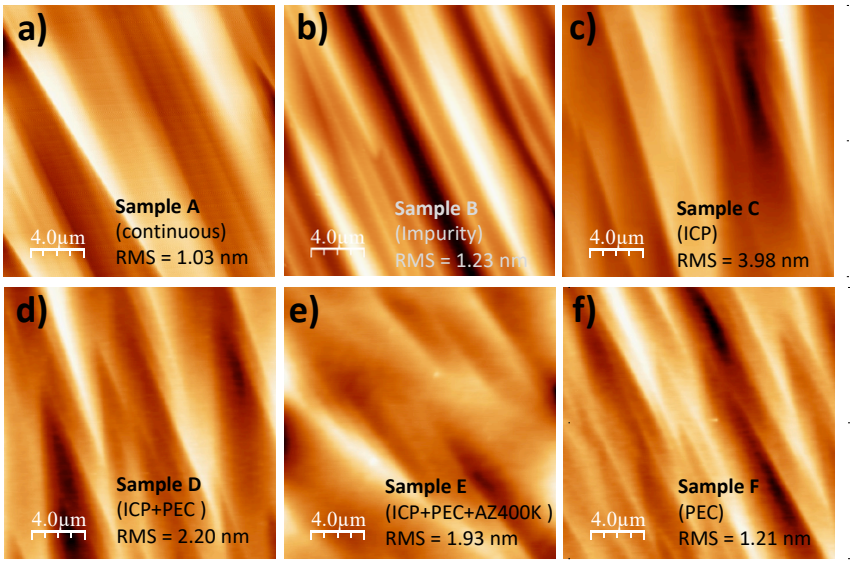

Figure 3.12 AFM images of the m-plane GaN surface after 7.25 μm of growth and subsequent a) continuously grown, b) impurity interface c) ICP interface, d) ICP + PEC interface, e) ICP + PEC AZ400K interface, f) PEC interface

Above 1.0 nm, surface roughness is attributed to ~7.25 μm of GaN constituting the underlying n-GaN regions and the ~ 500 nm of *p*-GaN which typically roughens due to the presence of H_2 flow. The variations in roughness are ascribed to the differing treatments (IMP, ICP, ICP +PEC, ICP+PEC+AZ400K, and PEC). The roughness of the ICP-etched-and-regrown (Sample C) shows the highest surface roughness at 3.98 nm. The ICP+PEC (Sample D) and ICP+ PEC+AZ400K (Sample E) show that the

etching/treatments effectively smooth the surface with 2.20 nm and 1.93 nm, respectively. The PEC etched only and regrown (Sample F) has an observed roughness of 1.21nm which is only marginally higher than the continuously grown (Sample A) at 1.03 nm and the impurity interface (Sample B) at 1.23 nm. Nevertheless, the morphologies follow similar trends as the previous surfaces observed on the m-plane GaN Schottky diodes after regrowth.

3.13 Fabrication of vertical *m*-plane GaN *p-n* diodes

The 6 samples are fabricated into *p-n* diode devices using standard photo-lithography, deposition, and dry-etching techniques as in section 2.5. The samples were fabricated with circular Pd/Au (30/300 nm) metal layers deposited using electron-beam deposition to serve as *p*-contacts with a diameter of 450 μm. The diodes were isolated by circular mesas formed by an inductively coupled plasma (ICP) etcher with the following parameters: Cl2/Ar/BCl3 gas (20/5/10 sccm) at a pressure of 5 mTorr, radio frequency (RF) power of 25 W, and ICP power of 130 W. A backside large-area-contact of Ti/Al/Ni/Au (10/100/50/300 nm) was then deposited by electron-beam deposition to complete the process. Additional information of sample fabrication and process is found in Appendix B. A schematic representation of the processed vertical *m*-plane GaN *p-n* diode is represented in Figure 3.13.

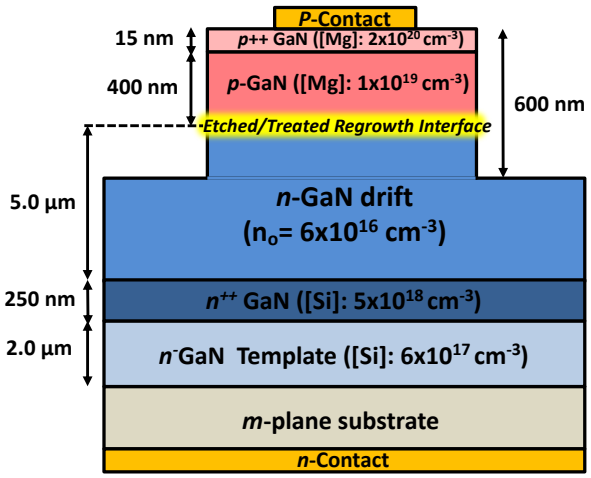

Figure 3.13: Cross-sectional schematic of fabricated etched-and-regrown vertical *m*-plane GaN *p-n* diode.

3.14 Electrical characterization of vertical *m*-plane GaN *p-n* diodes

The current density–voltage (*J–V*) characteristics of single representative diode out of approximately five measured *p-n* diodes on each sample are shown in Figure 3.14. In the forward bias (Figure 3.14.a), all the samples showed very low off-state forward leakage (< 1 µA/cm^2) below 1.5 V, except for sample B (IMP) and C (ICP) showing significant forward leakage (~58 µA/cm^2) and (~ 5 mA/cm^2), respectively. At higher voltages (>1.5 V) but still below turn-on, however, the off-state leakage currents are similar in samples A (continuous), E (ICP + PEC + AZ400K), and F (PEC). All diodes showed similar turn-on voltages (~2.5 V). The extracted ideality factors (n) as a function of applied voltage for all diodes are shown in Figure 2.15. As with the interrupted/treated *p-n* diodes (Chapter 2) nonideal diode behavior (n > 1) is ascribed to Shockley–Read–Hall (SRH)- dominant recombination current within the depletion region [28].

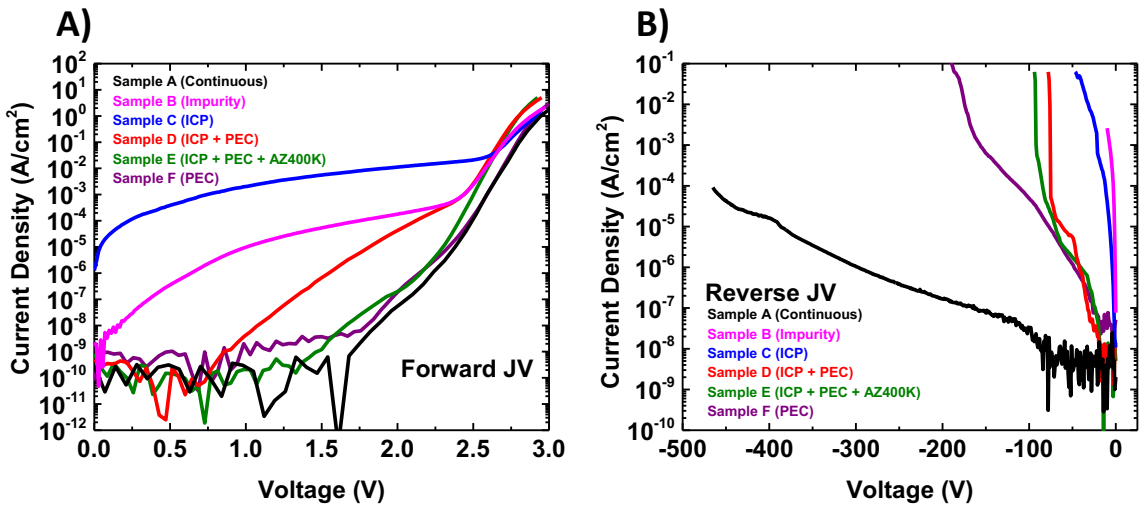

Figure 3.14. a) Forward *J-V* characteristics, b) Reverse *J-V* characteristics of selected representative etched-and-regrown *p-n* diodes from each sample

At forward voltages below turn-on (~2.4 V), sample B (IMP) and sample C (ICP) may be strongly dominated by SRH (high n) leading to a higher forward leakage compared with the rest of the diodes. Below 1 V, the leakage was similar across all the diodes, except for samples B and C. This indicates a leakage mechanism which may be attributed to the high concentration of interfacial impurities in sample B and high concentration of deep level states in sample C. Large ideality factors are observed in sample B below 2.4 V and sample C below 2.7 V which correlate with the observed forward leakage in these samples. Ideality factors are similar for samples A, E, and F throughout the voltage range. However, ideality factors for sample D increase below 2.5 V as compared to samples A, E, and F which is attributed to the higher forward leakage current than those samples. However, the ideality factor of sample D is lower than sample C below 2.7 V which indicates the mitigation of etched damage with the addition of the PEC etch on the ICP etched surface. Sample E further shows the mitigation of ICP etch damage with the addition of the subsequent AZ400K treatment after PEC etching in

reducing the ideality factors to nominally the same as the continuous sample A. Sample F also indicates a similar trend as a PEC etched-and regrown only *p-n* diode does not elevate the ideality factor, i.e. leakage current, as compared to the ICP etched-and-regrown sample B. As the ideal diffusion current dominates the SRH current, n reduces to a minimum value (~1.5–2) for all samples except sample C. Again, at higher bias voltages (above turn-on), n is dominated by the diode series resistance and increases.

Figure 3.14.b shows the reverse *J–V* characteristics of the samples. Significantly lower reverse blocking voltages (V_B) are observed in samples B–F as compared to the sample A (continuous) with $V_b \sim 300V$ at 1 $\mu A/cm^2$.

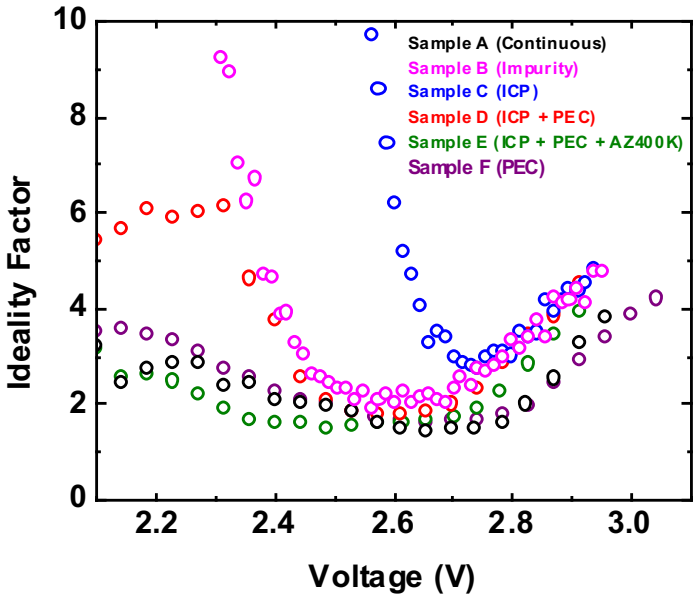

Figure 3.15: Ideality factor of selected etched-and-regrown *m*-plane GaN *p-n* diodes.

The analysis of sample A also shows no observable sharp increase in off-state reverse leakage current which indicates no avalanche breakdown mechanism in this sample up to reverse voltage of ~ 500V. Sample B (IMP) shows the lowest blocking voltage of all samples tested at $V_b \sim 1V$ at 1 $\mu A/cm^2$. Sample C also shows a low blocking voltage at

$V_b \sim 5V$ at 1 $\mu A/cm^2$. Thus, the effects of the impurity-regrown and ICP etched-and-regrown interface both show severally degraded reverse blocking voltages within the *p-n* diodes tested. Sharp increases in off-state reverse leakage current is observed in both these diodes (Sample B and C). However, the leakage mechanism may not be directly attributed to avalanche breakdown as the leakage current rises almost linearly from V = 0 V in both samples. Sample D shows a slight increase in blocking voltage at 1 $\mu A/cm^2$ with $V_b \sim 42V$. This slight increase in blocking voltage is again attributed to the subsequent PEC etch treatment after ICP etching. Samples E and F also show similar blocking voltage at 1 $\mu A/cm^2$ with $V_b \sim 40V$ and $V_b \sim 48V$, respectively. The off-state reverse current in samples D, E, and F however do not increase as linearly as sample B and C. Thus, a better comparison of the effects of the regrowth/treatments on the reverse blocking voltage (V_B) is made at 100 $\mu A/cm^2$.

As expected, sample A has the lowest reverse blocking voltages (V_B) of all samples with $V_b \sim 460V$ at 100 $\mu A/cm^2$. Sample B shows the lowest blocking voltage (V_b ~3V) of all samples tested at 100 $\mu A/cm^2$. Sample C also show a low blocking voltage (V_b ~12V) at 100 $\mu A/cm^2$. Sample D shows a slight increase in blocking voltage at 100 $\mu A/cm^2$ with $V_b \sim 75V$ compared to sample C. Sample E has an increased blocking ($V_b \sim$ 85 V) at 100 $\mu A/cm^2$ as compared to sample B, C, and D with. Samples F has a further increased blocking voltage ($V_b \sim$ 115 V) at 100 $\mu A/cm^2$ as compared to sample B, C, D, and E. Thus, the effects of the etched-treated-and-regrown processes on the reverse blocking voltages are observable. It may seem that the PEC and PEC+AZ400K processes increase the reverse blocking voltage as compared to ICP etched only sample. However, the increase in blocking voltage is only marginal, as they are far below that of the

continuously grown sample. Furthermore, the resulting blocking voltages of a PEC etched only sample also fall short of the continuously grown diode. Nevertheless, we will compare the electrical characteristics of the *p-n* diodes to the deep level concentrations measured from the Shottky diodes (Section 3.11) in the previous section.

3.15 Comparison of vertical *m*-plane GaN *p-n* diodes and Schottky diodes

The forward leakage current at 1.7 V and off-state blocking voltages at 100 $\mu A/cm^2$ of the *p-n* diodes are presented in Figure 3.16.a. The corresponding deep-level concentration of the associated Schottky diodes near and above the regrown interface are presented in Figure 3.16.b and c, respectively. From our previous assessment of the *J-V* characteristics from the *p-n* diodes (samples A-F), we observe that sample A has the highest blocking voltage (V_B ~ 460 V at 100 $\mu A/cm^2$) and lowest off-stage forward leakage (1 nA/cm^2 at 1.7 V). A comparison of the deep levels observed in the Schottky diode sample 1 (continuous) show the lowest concentration of E_c–1.9 eV, E_c – 2.9 eV , and E_c – 3.3 eV levels (~ $1\times 10^{14}cm^{-3}$, $3\times 10^{15}cm^{-3}$, $7\times 10^{15}cm^{-3}$, respectively) when comparing the rest of the sample near their regrown interfaces (Figure 3.16.b). Only the E_c – 3.3 eV level in samples 2, 4, and 7 is lower when observing above from the regrown interface, but is of the same order of magnitude as sample 1.

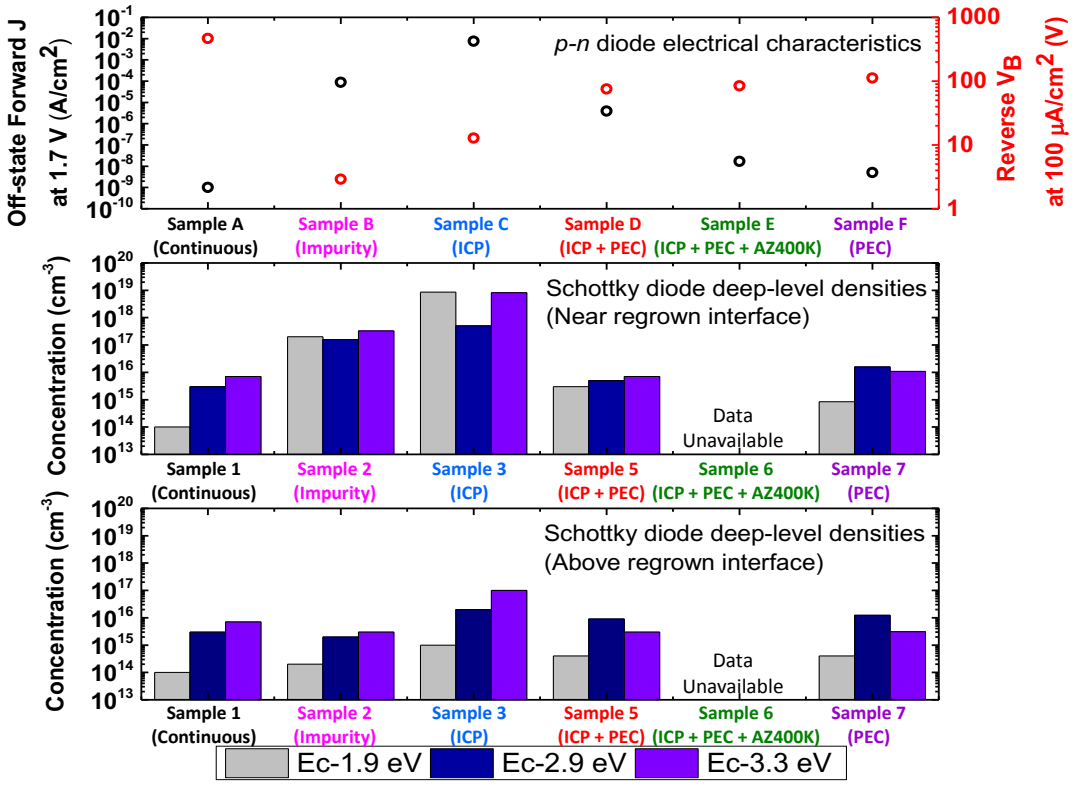

Figure 3.16. a) Off-state forward current density (at 1.7 V) and reverse blocking voltage (at 100 µA/cm2) of *p-n* diodes b) Deep-level densities near regrown interface of associated Schottky diodes, and c) Deep-level densities above regrown interface of associated Schottky diodes

It may be noted that the addition of samples 6 and 7 are presented in figures 3.16.b-and-c. These are the corresponding Schottky diodes to the *p-n* diode samples under current discussion. Data for sample 6 are not presented as a Schottky diode with similar ICP etched and a subsequent PEC+ AZ400K etch/treatment was not grown or fabricated. However, a PEC etched only Schottky diode was grown and fabricated which constitutes sample 7, here. This diode was not presented in the previous section as some ambiguity arose during testing which pinned the depletion region away from the regrown surface. These ambiguities will be discussed when comparing sample F to sample 7 in the following discussion.

The *p-n* diode sample B may be compared to it corresponding Schottky diode (sample 2). It is noted that sample B had the lowest blocking voltage (V_B ~ 2.9 V at 100 μA/cm^2) and the second highest forward leakage current (J ~ 88 μA/cm^2 at 1.7 V) of all *p-n* diodes tested. The deep-level densities away from the regrown interface of the corresponding sample 2 showed similar levels (E_c–1.9 eV ~ 2× 10^{14}cm^{-3}, E_c – 2.9 eV 2× 10^{15}cm^{-3} , and E_c – 3.3 eV ~7× 10^{15}cm^{-3}) as the continuous diode (sample 1). However, the deep-level densities near the regrown interface of sample 2 are the second highest of all samples tested with E_c–1.9 eV ~ 2× 10^{17}cm^{-3}, E_c – 2.9 eV ~2× 10^{17}cm^{-3} , and E_c – 3.3 eV ~3.3× 10^{17}cm^{-3}. These levels are only exceeded by the ICP-etchted-and-regrown sample 3. Thus, we can see the effects of the elevated deep levels near the regrown junction in the impurity interface *p-n* diode (sample B). It may be noted that the incorporation of interfacial impurities of sample B were previously unknown regarding their electronic states withing the energy-band of the diode. Thus, we can more closely identify the effects of the concentrations of interfacial impurities (Si, O, and C) on the electronic states. However, exact correlation of the interfacial impurities on the exact deep-level state is unable to be directly identified. Additionally, interfacial impurities may also incorporate as shallow donors or acceptors which are not as easily identifiable through the SSPC methods presented previously.

A comparison of the ICP-etched-and-regrown *p-n* diode (sample C) will be compared to its corresponding Schottky diode (sample 3). Sample C was observed to have the highest forward leakage current (J ~ 7.5 mA/cm^2 at 1.7 V) and the second lowest blocking voltage (V_B ~ 12.8 V at 100 μA/cm^2). The deep-level densities of the corresponding sample 3 showed the highest levels (E_c–1.9 eV ~ 1× 10^{15}cm^{-3}, E_c – 2.9 eV

~2× 10^{16}cm^{-3} , and E_c – 3.3 eV ~1× 10^{17}cm^{-3}) away from the impurity interface. Furthermore, the deep-level densities of sample 3 are the highest away from the regrown interface of all samples tested with E_c–1.9 eV ~ 8.6× 10^{18}cm^{-3}, E_c – 2.9 eV ~5.0× 10^{17}cm^{-3} , and E_c – 3.3 eV ~8.2× 10^{18}cm^{-3}. It appears that these elevated deep-level concentrations affect the forward leakage current. In comparison of the impurity interface sample B the deep level densities corresponding to sample C are significantly higher near the regrown junction with ~800× increase in leakage current. However, the reverse blocking voltage of sample C is only marginally higher, ~4× higher, than sample B. However, since sample 2 shows lower deep-level densities than sample 3 it may be expected that sample B would have a larger blocking voltage than sample C. But, as stated before, the effects of the interfacial impurities may not only effect deep-level concentrations, as additional mechanisms may be affecting the blocking voltage of sample B. Regardless, both samples B and C have significantly raised deep-level densities near the regrown interface which reduce the blocking voltages and increase the forward leakage currents.

Comparing the ICP + PEC etched-and-regrown *p-n* diode (sample D) and its corresponding Schottky diode (sample 5) shows improvement in blocking voltage and forward leakage current. Blocking voltage is increased (V_B ~ 76 V at 100 μA/cm^2) and forward leakage current is reduced (J ~ 3.9 μA/cm^2 at 1.7 V) as compared to the ICP etched-and-regrown p-n diode (sample C). The deep-level densities of the corresponding sample 5 showed nominally low levels away from the impurity interface (E_c–1.9 eV ~ 4× 10^{14}cm^{-3}, E_c – 2.9 eV ~9× 10^{15}cm^{-3} , and E_c – 3.3 eV ~3× 10^{15}cm^{-3}). The deep-level densities of sample 5 are significantly reduced compared to the ICP etched-and regrown

sample 3 near the regrown interface with E_c–1.9 eV ~ 3.0× 10^{15}cm^{-3}, E_c – 2.9 eV ~5.0× 10^{15}cm^{-3} , and E_c – 3.3 eV ~7.0× 10^{15}cm^{-3}. However, unlike the impurity interface p-n diode (sample 2), the reduced levels seem to effect both the reverse blocking voltage and forward leakage current. The reverse blocking voltage of sample D is increased ~6× compared to sample C, and the forward leakage is reduced ~190× compared to sample C. However, the nominally low deep-level densities of sample D are not sufficient to achieve similar blocking voltages and forward leakage currents as that of the continuously grown *p-n* diodes (sample A). In comparison sample 5 has only slightly elevated deep level densities away from the regrown junction as compared to the continuous diose (sample 1). When comparing sample 1 and 5 near the regrown interface we observe the greatest increase (~30×) in the E_c–1.9 eV level. This may indicate that this level could be the predominant level which effects forward leakage current and reverse blocking voltage. However, further investigation will be needed to confirm this.

A comparison of the ICP + PEC + AZ400K etched-and-regrown *p-n* diode (sample E) and its corresponding Schottky diode (sample 6) is unable to be made due to a lack of such a Schottky diode for analysis. However, it may be observed that the blocking voltage is increased (V_B ~ 85 V at 100 μA/cm^2) and forward leakage current is reduced (J ~ 16.8 nA/cm^2 at 1.7 V) when compared to the ICP + PEC etched-and-regrown *p-n* diode (sample D). As the data are unavailable, we are left only to interpolate what the deep level defect densities should be, considering the previous sample investigated. It may be assumed that the deep level densities would be lower in sample 6 vs. sample 5, based on improved electrical characteristics. Primarily, a reduction in the E_c–1.9 eV level may be attributed to the reduced leakage current based on our

comparison of sample D and A in the previous section. Nevertheless, an observable benefit of the AZ400K treatment on the electrical performance in sample E is observed in comparison to sample D.

The SSPC spectrum of the PEC etched-and-regrown Schottky diode (sample 6) is presented in Figure. 3.17.a. The depth profiling of the deep levels for sample 6 using the LCV method is also presented in Figure 3.17.b. Similar deep-levels at E_c–1.9 eV, E_c – 2.9 eV, and E_c – 3.3 eV are observed as in the rest of the samples measured previously. The deep level concentrations are presented in Figure 3.16.b and c for comparison. It may be noted that the deep-level densities are taken at approximately the region where the densities have a drastic increase in the curves of figure 3.17.b.

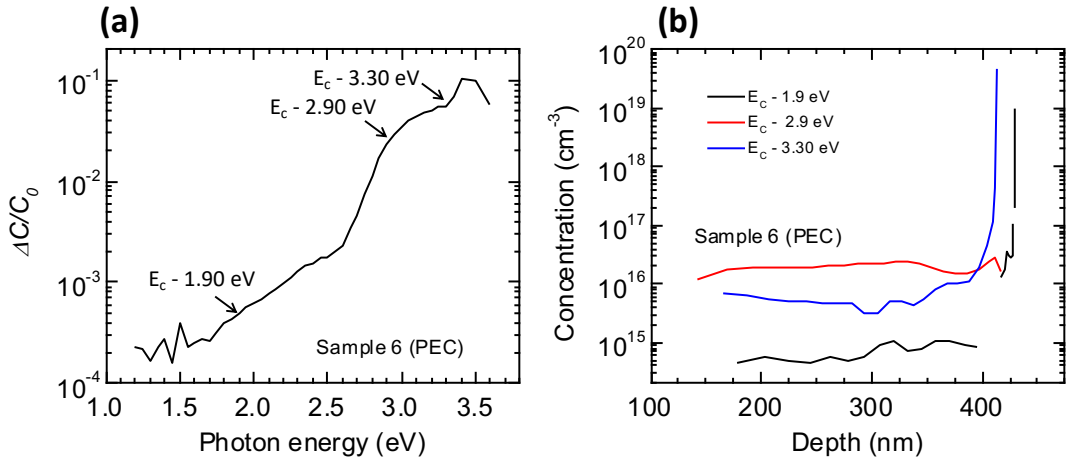

Figure 3.17. (a) SSPC spectrum and (b) depth profile of the PEC etched-and-regrown Schottky diode (sample 7)

Sample F is observed to have the second highest blocking voltage (V_B ~ 112 V at 100 μA/cm^2) and the second least forward leakage current (J ~ 5.0 nA/cm^2 at 1.7 V) of all diodes tested (sample A being the best). The deep-level densities of the corresponding sample 7 showed nominally low levels away from the impurity interface (E_c–1.9 eV ~

$4\times 10^{14}cm^{-3}$, $E_c - 2.9$ eV $\sim 1.23\times 10^{16}cm^{-3}$, and $E_c - 3.3$ eV $\sim 3.1\times 10^{15}cm^{-3}$). The deep-level densities of sample 7 away from the interface are similar to the ICP+PEC etched and regrown sample 5. The deep-level densities of sample 7, when compared to the ICP+PEC etched-and regrown sample 5 near the regrown interface, show an ~28× reduction in the $E_c - 1.9$ eV ($\sim 4.0\times 10^{14}cm^{-3}$) - an ~3× increase in the $E_c - 2.9$ eV level ($\sim 1.6\times 10^{16}cm^{-3}$) , and nominally the same (~1.5×) $E_c - 3.3$ eV level ($\sim 1.1\times 10^{16}cm^{-3}$. The blocking voltage is not significantly increased (~1.3×) in sample F when compared to sample D either. However, the forward leakage current of sample F is reduced ~780× when comparted to sample D. The only significant difference is the reduction of the $E_c - 1.9$ eV level ($\sim 4.0\times 10^{14}cm^{-3}$) in sample 7 compared to sample 5. Thus, we see additional evidence that the $E_c - 1.9$ eV level contributed more significantly to the electrical performance of the diodes than the other levels. Another comparison to make is from sample F and sample C. We have seen that ICP etching is a fundamental requirement for selective-area doping form power electronic applications. However, we can see that PEC etching may also be used in order to develop selective-area doping region for the same purpose. As usual, many challenges would arise with this implementation. However, we can see that this switch may benefit since much better electrical performance is observed from the PEC etched-and-regrown *p-n* diodes we have investigated here.

We have thus made comparisons of the electrical performance of regrown *p-n* diodes with the deep-levels observed in Schottky diodes. The effects of ICP etching on the regrown junctions of *p-n* diodes are shown to severely degrade the electrical performance as we compare to the elevated deep levels within the corresponding

Schottky diodes. The addition of PEC etching and AZ400K treatments shows a reduction of the deep level densities along with corresponding increase in electrical performance. However, one thing to mention is validity of the comparison of the *p*-*n* diode to the Schottky diodes. In the case of the *p*-*n* diode there is the addition of regrown p-GaN, but in the Schottky diodes the regrown layers are *n*-type GaN. It may not be entirely accurate to assume that the deep levels present in regrown *n*-GaN are similar to regrown *p*-GaN, considering the differences in growth conditions as seen in sections 1.1 and 1.12, respectively. Additionally, the regrown junctions are not entirely within *p*-GaN, but at the metallurgical junction between *n*-GaN and *p*-GaN layers. Therefore, contributions to the deep-level defects may be present in both types. Nevertheless, a comparison is made in order to at least identify contributions made from the n-GaN layers, considering they constitute the drift layer and are the material that is exposed to the dry-etching processes.

3.16 Summary of dry-etched enhanced damage: effects on planar *m*-plane diodes

A summary of Chapter 3 details the investigation of dry-etched enhanced damage on planar vertical *m*-plane GaN diodes. Dry etching is investigated due to its implementation for selectively-doped regrowth for vertical GaN power electronics. Thus, planar Schottky diodes were grown/regrown in order to measure the damage as a result of crystalline defects which manifest as deep-level traps within the band-gap of GaN.

Steady-state photocapacitance (SSPC) was used to examine the deep level defect concentration along with lighted capacitance–voltage (LCV) measurements to obtain the depth profile of the defect concentrations in the regrown diodes. Comparison of changes in the defect concentration relative to a continuously grown film is presented which shows the elevation of E_c–1.9 eV, E_c – 2.9 eV, and E_c – 3.3 eV levels within ICP etched-

and-regrown GaN. Elevated defect concentrations are shown to be localized at regrowth interfaces in the presence of an impurity interface even without a plasma etch. Elevated defectively is also shown to propagate away from the regrown region within dry-etched-and-regrown samples. Surface treatments (AZ400K) and post wet etch treatments (PEC) are shown to reduce the defect concentration at the regrown interface. Furthermore, the concentration of the near-mid bandgap defect levels is compared to forward and reverse leakage, suggesting that these defects are major contributors to diode leakage.

Additionally, comparisons of the electrical performance of regrown *p-n* diodes with the deep-levels observed in Schottky diodes are included. The effects of ICP etching on the regrown junctions of *p-n* diodes are shown to increase the forward leakage current and reduce the reverse blocking voltage as compare to continuously grown *p-n* diodes. These adverse effects on the electrical performance are correlated with the elevated deep-level densities of the corresponding Schottky diodes to the regrown *p-n* diodes. Furthermore, subsequent surface treatments on ICP etched-and-regrown *p-n* diodes are observed to mitigate the degradation in electrical performance by reducing forward leakage current and increase reverse blocking voltage. It is also observed that the corresponding deep-level defect concentrations reduce with these treatments. However, complete mitigation of these concentrations and complete restoration of the electrical performance of the p-n diodes utilizing these treatments is not realized. Thus, additional investigation of these techniques is required to completely solve these issues while simultaneously reducing the effects of interfacial impurities discussed in chapter 2. Therefore, Chapter 4 of this disseration will be dedicated to investigating the leakage mechanisms that arise from dry-etch enhanced damage. A motivation for this is to better

understand leakage mechanisms for the purpose of developing more systematically reliable processes to identify and mitigate them.

3.17 References

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Chapter 4 Leakage mechanisms in planar *m*-plane *p-n* diodes.

This chapter will investigate leakage mechanisms in dry-etched enhanced damage on planar vertical *m*-plane GaN *p-n* diodes. We have thus far observed the degradation of p-n diode performance due to interfacial impurities (chapter 2) and from dry-etching (Chapter 3). A novel radio-frequency (RF) technique will be presented in order to ascertain the origin of the increased leakage. Thus, a small-signal RF analysis was conducted to evaluate the effects of etching and regrowth on differential resistance, carrier lifetime, series resistance, and capacitance in etched-and-regrown nonpolar *m*-plane *p-n* diodes. Rate equations considering carrier diffusion and recombination are used to derive an equivalent electrical small-circuit model of fabricated PN diodes. Expressions for the input impedance response are fit to experimental data obtained and used to extract carrier dynamic parameters. Differences in differential resistance, carrier lifetime, capacitance, and series resistance between etched-and-regrown devices are compared to continuously grown devices in order to investigate the effects of dry-etched enhanced damage on carrier dynamics. The method presented is relevant to the understanding of leakage current at etched-and-regrown junctions for high-power electronic devices in GaN.

As mentioned, the two primary challenges facing etched-and-regrown interfaces on GaN are the presence of interfacial impurities (Si, O, and C) and an elevation of deep level defects below, at, and above the regrown interface [1], [2]. The concentration and type of interfacial impurities have shown to degrade the forward leakage and reverse blocking voltages. Furthermore, elevation of the deep level defects at E_C - 1.9 eV, E_C - 2.9 eV, and E_C - 3.3 eV after dry-etching has been observed to influence the electrical characteristics

of Schottky diodes with an increase in forward and reverse leakage as compared to as-grown diodes [2]. Corresponding *p-n* diodes with similar dry-etching have also shown increases in forward leakage and reverse blocking voltage. Therefore, additional understanding of carrier dynamics in the presence of elevated impurities and deep level defects is necessary to further understand the challenges of etch-and-regrown devices. By extracting differential resistance, carrier lifetime, series resistance, and capacitance, the effects of dry-etched enhanced damage on devices on GaN may be better understood. However, carrier dynamic parameters such as lifetime and capacitance are not as easily measured in typical *J-V* (current density-voltage) measurements. Thus, a method to test for these parameters during in-situ electrical operation is developed.

We investigate etched-and-regrown *m*-plane GaN *p-n* diodes using a small-signal RF method. A small-signal electrical equivalent circuit is derived from rate-equations expressing the carrier dynamics of a *p-n* diode. The real and imaginary parts of input impedance of the equivalent circuit are simultaneously fit to experimentally measured input impedance of the *p-n* diode to extract carrier dynamic parameters such as differential resistance, carrier lifetime, series resistance, and capacitance. A comparison of etch-and-regrown and continuously grown devices is made to understand the effects of the regrown junction on the electrical performance of the device. The effects of the carrier dynamics are analyzed to explain the observed increase in leakage of the etched-and-regrown devices compared to continuously grown devices.

4.1 *m*-plane GaN vertical *p-n* diodes for small-signal electrical RF analysis

GaN *p-n* diode structures were grown using a Veeco metal-organic chemical vapor deposition (MOCVD) system on a freestanding *m*-plane GaN substrate with a -0.95° mis-cut towards the minus *c*-direction from Mitsubishi Chemical Corporation (MCC). The substrate is *n*-type Si doped ($n_0 = 1\times10^{17}$ cm^{-3}). The small crystal off-angle minimizes the roughness of the overgrown GaN epilayer by mitigating pyramidal hillocks.[3] The epitaxial layers were grown at a pressure of 500 Torr using trimethylgallium (TMGa) and ammonia (NH_3) as precursors for elemental Ga and N respectively. The *n*-type dopant is introduced using SiH_4 diluted in nitrogen. The *n*-GaN layers are grown at a substrate temperature of ~ 960°C measured by a pyrometer. *P*-type GaN was grown by supplying Cp_2Mg at a growth temperature of 835^{0}C, reactor pressure of 205 Torr, and a V/III ratio of 2630 under H_2 ambient. The epitaxial growth consists of a 2-µm-thick *n*-type GaN buffer layer ([Si]: 6×10^{17} cm^{-3}) followed by a 250-nm-thick n^+-GaN ([Si]: ~ 5×10^{18} cm^{-3}), and a subsequent 1-µm-thick lightly doped *n*-type GaN (with N_D-N_A: ~ 1×10^{17} cm^{-3}) to serve as a drift region. The net doping concentration (N_D-N_A) of the lightly doped *n*-GaN drift layer was found using a capacitance-voltage (*C-V*) evaluation on a separate calibration sample. An inductively coupled plasma technique was then applied on pieces of the drift layer to introduce damage to the sample surface prior to the p-GaN regrowth. Subsequent 200 nm *p*-type GaN ([Mg]: 1×10^{19} cm^{-3}) was grown followed by 15 nm p^+-type GaN ([Mg]: 1×10^{19} cm^{-3}). Samples were annealed at 700^{0}C to activate the Mg acceptor doping. A schematic of the *p-n* diode structure is shown in Figure 1(a).

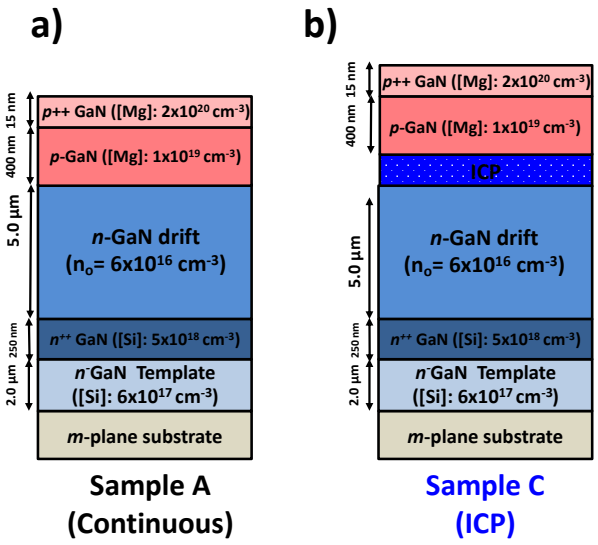

Figure 4.1. Schematic of vertical m-plane GaN Schottky didoes with the following surface treatment: a) continuously grown, b) ICP interface

A total of two samples with various treatments at the regrowth interface were studied. Sample 1 (reference sample) was continuously grown without any interruption, etching, or surface treatment to serve as a reference baseline as-grown material for comparison. Sample 2 was regrown after 400 nm of dry etching using a PlasmaTherm Apex SLR inductively coupled plasma (ICP) etcher, in which $Cl_2/Ar/BCl_3$ at a chamber pressure of 5 mTorr with an ICP power of 130W and a RF power of 30W were used.

The *p*-GaN layers were grown after the 5 previously mentioned etches/treatments. The *p*-type growth conditions consisted of: H_2 flow of 3500 sccm, NH_3 flow rate of 2000 sccm, pressure of 205 Torr, temperature of 835°C, and V/III ratio of 7020. The p-type dopant Cp_2Mg is flowed along with H_2 in order to constitute the acceptor type doping. The layer constituting the *p*-GaN part of the *p*-*n* junction was grown with an intentional concentration of [Mg] =1× 10^{19}cm^{-3} with a thickness of 400 nm. A highly doped p^{++}-type layer follows with an intentional concentration of [Mg] =1× 10^{20}cm^{-3} which

constitutes the *p*-contact layer of the diode. The sample was then annealed at 700ºC for 15 min in order to activate the Mg atoms within the *p*-type layers.

4.2 Fabrication of vertical *m*-plane GaN *p-n* diodes for small-signal electrical RF analysis

The two samples were fabricated into *p-n* diodes for small-signal RF measurements using standard photolithography, and deposition techniques. The samples were fabricated with circular Pd/Au (30/300 nm) metal layers deposited using electron-beam deposition to serve as *p*-contacts with a diameter of 450 µm. The diodes were isolated by circular mesas formed by an inductively coupled plasma (ICP) etcher with the following parameters: $Cl_2/Ar/BCl_3$ gas (20/5/10 sccm) at a pressure of 5 mTorr, radio frequency (RF) power of 25 W, and ICP power of 130 W. Top-side contacts of Ti/Al/Ni/Au (10/100/50/300 nm) were then deposited by electron-beam deposition to utilize the co-planer ground-signal (GS) probe tip for RF measurement. Additional information of sample fabrication and process is found in Appendix B. A schematic representation of the processed vertical *m*-plane GaN *p-n* diode is represented in Figure 3.13.

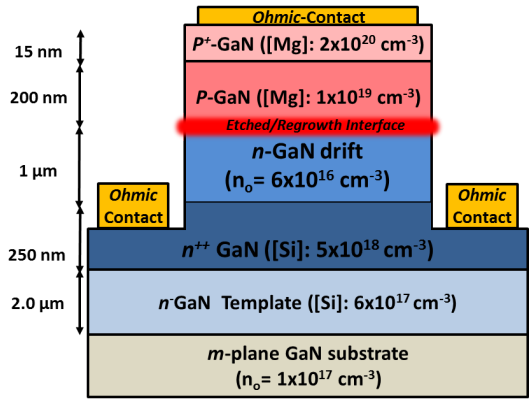

Figure 4.2: Cross-sectional schematic of fabricated etched-and-regrown vertical m-plane GaN Schottky diode.

4.3 Electrical characterization of vertical *m*-plane GaN Schottky diodes for small-signal electrical RF analysis

The current density-voltage (*J-V*) characteristics of a single representative diode out of ~ 5 measured diodes on each wafer are shown in Figure 1(b). According to the *J-V* results of Figure 1(b), sample 1 shows the lowest reverse leakage current of ~ 1×10^{-7} A/cm^2 at -10 V and a turn-on voltage of ~ 2.0 V. Comparison of *J-V* data between the continuously-grown (sample 1) and the etched-and-regrown (sample 2) diodes indicates the influence of the dry-etch process on current leakage. Sample 2 shows a ~ $1x10^9$ larger reverse *J* compared to that of the reference (sample 1) (~ 1×10^{-7} A/cm^2 compared to ~ 10 A/cm^2 at -10 V). The forward turn-on voltage of sample 2 is similar (2.0 V) for all samples. However, sample 2 exhibits a higher leakage current than sample 1 below turn-on (~ 2 A/cm^2 compared to ~1×10^{-7} A/cm^2) at 1.8V.

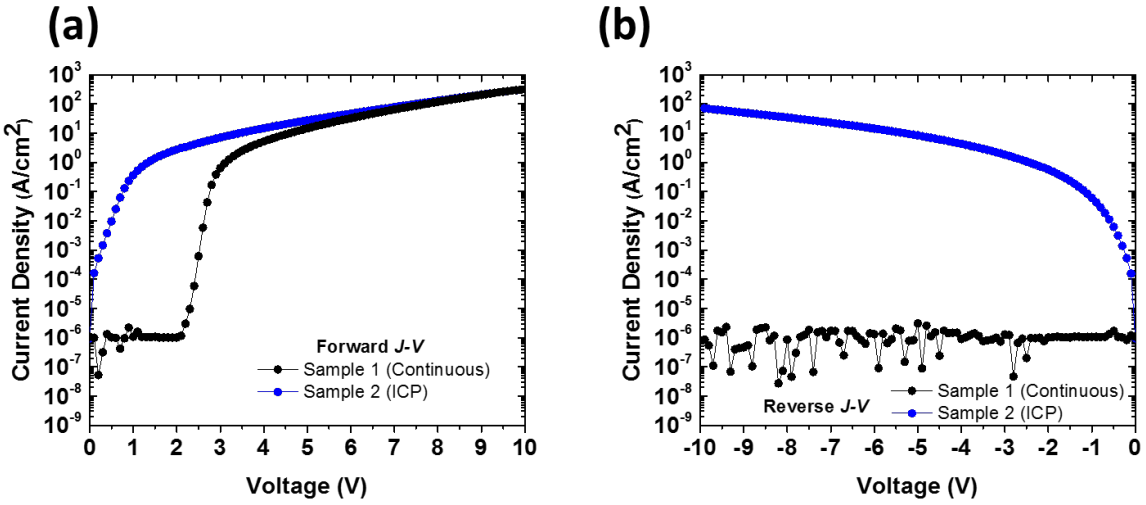

Figure 4.3: *J-V* characteristics of selected representative *p-n* diodes from each sample. a) forward, and b) reverse regime

4.4 Small-signal equivalent circuit of vertical *m*-plane GaN *p-n* diode

A small-signal equivalent circuit is derived from a rate equation for a *p-n* diode in order to extract the quantities of the associated circuit elements from an experimental RF measurement technique. The energy-band diagram of a *p-n* diode structure showing the dominant carrier mechanisms under forward bias in this model is shown in Figure 4.4.a. The injected carrier number toward the depletion region is denoted as (N). The quasi-fermi-level separation outside the depletion region is denoted as (V), and (I) is the injected current into the depletion region. The current required to charge the space-charge capacitance (C_{sc}) is ($C_{sc}\frac{dV}{dt}$). The minority carrier lifetime (τ) is the delay that minority carriers (N) experience before they recombine. The electron charge is denoted as (q). We considered a single-particle rate equation assuming the carrier dynamics is dominated by electrons due to the heavy mass of holes. A similar model has shown previously to accurately describe electrical characteristics of LEDs [4]. The following single-particle rate equation governing the mechanisms in the *p-n* diode is written:

$$\frac{dN}{dt} = \frac{I}{q} - \frac{C_{sc}}{q}\frac{dV}{dt} - \frac{N}{\tau} \tag{4.1}$$

The small-signal form of Equation 4.1 can be written in Equation 4.2 by assuming a small-signal value in addition to the steady state for all variables (e.g., $x = x_0 e^{j\omega t}$ where x is the small-signal parameter, x_0 is the amplitude of the signal, ω is the RF angular frequency, and t is time.). The differential form is used to derive the small-signal electrical circuit for the *p-n* diode, shown in Figure. 4.4.b.

$$j\omega n = \frac{i}{q} - \frac{C_{sc}}{q} j\omega v - \frac{n}{\tau_\Delta} \tag{4.2}$$

The substitute Δ denotes differential value. We used a similar approach to that in Ref. [5] to relate the small-signal carrier number to the applied small-signal voltage by the capacitance associated with the carriers (C).

$$n = \frac{Cv}{q} \tag{4.3}$$

Inserting Eq. (3) into Eq. (2) yields Eq. (4):

$$\left(j\omega(C + C_{sc}) + \frac{C}{\tau_\Delta}\right) v = \ i \tag{4.4}$$

The resistance associated with carries may be defined in Equation 4.5 as:

$$\frac{C}{\tau_\Delta} \ = \frac{1}{R} \tag{4.5}$$

By inserting Equation 4.5 into Equation 4.4, and rearranging for admittance (Y) we obtain Equation 4.6:

$$Y = j\omega(C + C_{sc}) + \frac{1}{R} \tag{4.6}$$

The admittance equation in (4.6) yields the small-signal equivalent circuit of the *p-n* diode shown in Figure 4.4.b with the series resistance (R_s) manually added. The series

resistance is comprised of the contact resistance and the resistance of the semiconducting layers.

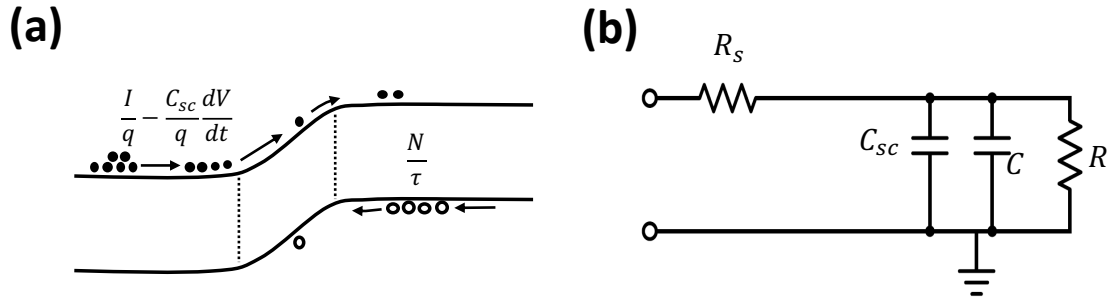

Figure 4.4: (a) Dominant carrier processes in *p-n* diode, (b) small-signal equivalent electrical circuit of the *p-n* diode

4.5 Small-signal RF testing of vertical *m*-plane GaN *p-n* diodes

The input impedance of the p-n diodes was measured using a network analyzer (Keysight e5061b) by combining a time-dependent small-signal voltage provided by port 1 of the network analyzer (NA) with a peak-to-peak amplitude of ~20 mV (-30dBm) to the DC bias (-10V to 10V) of the *p-n* diodes. The *p-n* diodes were probed using a micro-RF ground-signal-ground probe (ACP40-GSG-150, Cascade Microtech, Inc.). Additional information on the RF setup is presented in Appendix C.

To determine the carrier dynamic parameters, the parameters of the circuit in Figure 4.4.b were extracted by fitting the input impedance of the circuit to the measured input impedance of the p-n diode for a frequency range of 500 kHz to 2 GHz. The real and imaginary parts of the impedance were extracted from the measured reflection coefficient (S11). The measurements were carried out for devices with circular diameters of 450 μm for current densities ranging from 1×10^{-7} A/cm^2 to 300 A/cm^2 (-10V to 10V)

for the continuously grown p-n diode (Sample 1) and 30 A/cm^2 to 300 A/cm^2 (-10V to 10V) for the etched-and regrown p-n diode (sample 2).

The simultaneous fit of the input impedance of the circuit in Figure 4.4.b to the measured input impedance of the continuous (sample 1) and etched-and-regrown diode (sample 2) in the reverse regime at a reverse voltage of -10 V, and in the forward regime at current densities of ~ 1 A/cm^2 and ~ 100 A/cm^2 are shown in figure 4.5a and b, respectively.

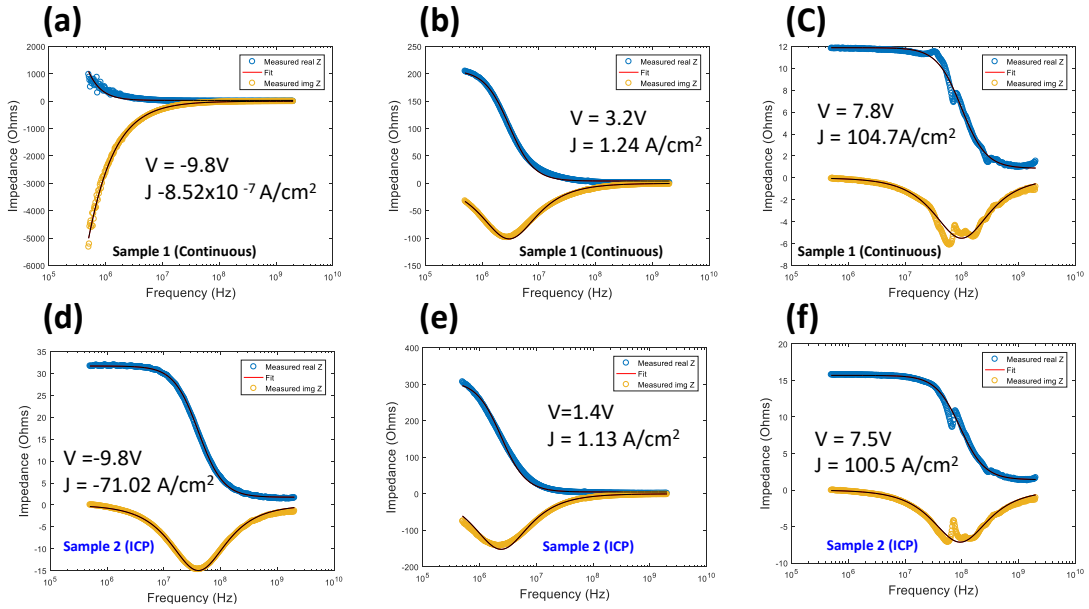

Figure 4.5 simultaneous fit of the input impedance of the circuit in Fig.2(b) to the measured input impedance of: a-c) continuous diode (sample 1), and d-f) etched-and-regrown diode (sample 2) in the reverse and forward regime

The fits of the complex impedance for both samples (1 and 2) show high R-squared values above 95% in the reverse regime (-10V) and at low current densities (~ 10 A/cm^2). However, at high current densities (> 100 A/cm^2) a resonance occurs around 50 MHz (Figure 4.5.c and f) which leads to degradation in the fitting. This resonance may be

attributed to parasitic capacitances and inductances which only influence the *p-n* diodes at high current densities. Nevertheless, the regime of most interest is in the forward off-state (below and around turn-on) at current densities from 0 - 50 A/cm^2 for the samples tested. Therefore, the proceeding analysis may be confidently made considering the fittings with high R-squared values at these current densities.

4.6 Analysis of small-signal RF testing of vertical *m*-plane GaN *p-n* diodes

The results of the extracted small signal equivalent circuit are presented in Figure 4.6. The results are presented versus applied DC voltage due to the differences in current densities between diodes. Typically, RF equivalent circuit analysis on p-n diodes is compared to current density. However, due to the leakage current present in sample 2, the independent variable to observed differences in the circuit parameters is the applied voltage.

The parasitic series resistance (R_s) of sample 1 and 2 are shown in Figure 4.6.a. Dynamic behavior is not expected from this circuit element. However, the association of the series resistance and differential resistance is constituted by the conservation of current in the circuit. The slight dependence vs increasing voltage may also be associated with reduced resistances due to current crowding at higher current densities of non-ohmic contacts [6]. Nevertheless, dynamic behavior is observed. The series resistance for sample 1 is observed to linearly decrease from reverse bias (-10 V) towards turn-on (~ 2.5 V) with increasing bias (~ 13 Ω at -10 V and ~ 13 Ω at 2.5 V). Thus, the current density for sample 1 does not increase (J ~ 1x10^{-7} A/cm^2 at < 2.5 V), which indicates no addition of carries from the contacts to contribute to current with increasing reverse

biases. Above turn-on, the series resistance drops sharply (~ 4 Ω at -10 V) and slightly reduces with increase forward bias. The differential resistance of sample 2, however, is observably different. The maximum series resistance (~ 15 Ω) is observed at V = 0V. However, the series resistance begins to decrease with increasing forward bias. In this sample, significant reverse leakage is observed the reverse regime (Figure 4.3.b). Therefore, the contacts must inject carriers to accommodate the increased leakage current. Thus, the series resistance is effectively reduced due to the increase in inject carriers from the contacts. Above V = 0 V, the differential resistance of sample 2 reduces for the same reason due to current leakage. After ~ 1.5 V the series resistance achieves its nominal value (~2 Ω) as forward bias increased. It must be noted, the magnitudes of the parasitic series resistances (R_s ~ 1-30 Ω) are much less than the differential resistances (R~ 300 Ω – 25 kΩ) of the two sample below turn-on. Thus, the predominant circuit elements in this regime of interest are the differential resistance (R) and capacitance (C). These two elements are the driving factors for the electrical characteristics we will be discussing.

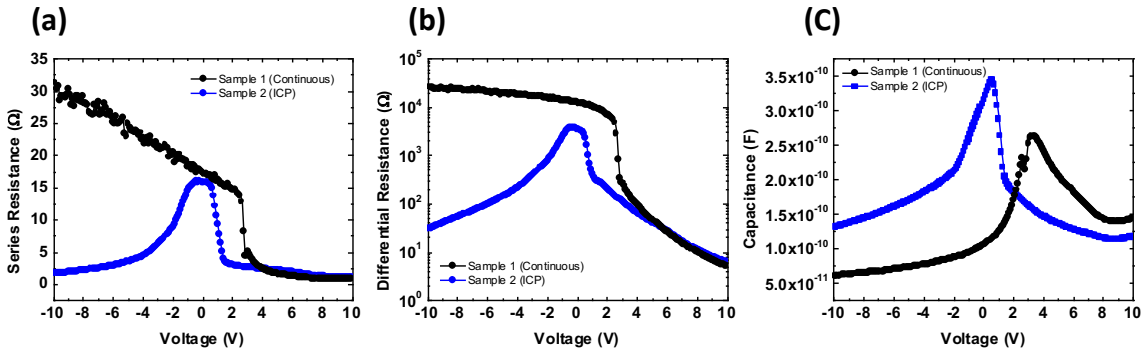

Figure 4.6: a) Series resistance, b) Differential resistance, and c) Capacitance vs. voltage of continuously-grown and etched-and-regrown *p-n* diodes.

Figure 4.6.b shows the differential resistance (R) of the small-signal equivalent. circuit of the continuously grown (Sample 1) and etched-and-regrown (sample 2) *p-n* diodes. It may be noted, the differential resistance is typically inversely proportional to the injected current (number of carriers) in a similar equivalent circuit for LEDs [5]. Comparing to voltage, we see that sample 1 has a slightly increasing differential resistance (R) at higher reverse voltages (~13 kΩ @ 0 V and ~25 kΩ @ -10 V). Sample 2 shows the opposite behavior, with a decreasing differential resistance (R) at higher reverse voltages (~3 kΩ @ 0V and ~31Ω @ -10 V). The behavior of sample 1 is expected as the depletion region extent is increased by a power of 2 versus applied reverse voltage ($W \sim V^2$). Thus, a reduction of injected current is expected due to the increasing potential barrier to which free carriers must overcome. As observed in the *J-V* curve (Figure 4.3.b) the reverse leakage of sample 1 does not increase with applied bias. Additionally, the reverse leakage of the etched-and-regrown (sample 2) shows a steadily increasing leakage current with increasing applied bias. Thus, injected current increases as a result of increased free carries in the reverse regime. In the forward regime the differential resistance begins to decrease as the diode approaches turn-on (~ 2.5 V). Above turn-on the differential resistance of sample 1 drops drastically to ~ 300 Ω at 2.7V. Thus, an increase in injected current is observed due to the reduced barrier height which allows free carriers to cross the reduced depletion region. The differential resistance of sample 2 also drops with applied forward bias, however the onset of leakage current is immediate with $J \sim 1$ A/cm^2 at ~1.4V. At this voltage the differential resistance begins to decrease less sharply with an observed kink in the curve above this point. This point will indicate a position where recombination and diffusion current begin to compete significantly, which

we will discuss later. Above ~ 6 V (far above flat-band) the differential resistance between the two samples is nominally the same, indicating a nominal effect on the carriers at high current density.

The total capacitance versus voltage of the diodes is shown in Figure 4.6.c. It may be noted that the space-charge capacitance (C_{sc}) and diode capacitance (C) are in parallel in the small-signal equivalent circuit (Figure 4.4.b). Thus, the fitting of the circuit model parameters to the complex impedance measurements is unable to discriminate between the two capacitances due to their configuration. Total capacitance must be analyzed to extract each term based on the regime of operation where each is dominant. Therefore, the total capacitance can be expressed as:

$$\mathbf{C_{tot} = C + C_{sc}} \qquad (\mathbf{4.7})$$

The space-charge capacitance (C_{sc}) originates from the separation of charge in the depletion region, thus with an applied reverse bias $V_R + dV_R$ an additional capacitance is associated from $C_{sc} = dQ/dV_R$. For a one-sided junction we obtain an expression for the space charge-capacitance as:

$$\mathbf{C_{sc}} \approx \sqrt{\frac{\mathbf{e\varepsilon_s N_d}}{\mathbf{2(V_{bi} + V_R)}}} \qquad (\mathbf{4.8})$$

However, the space-charge capacitance is only dominant in the reverse regime and low forward bias regime as the depletion region begins to shrink at higher forward biased toward turn-on. The diode capacitance alternatively is predominantly affected by the small-signal attenuation of voltage in the forward bias regime which is affected by the diffusion of injected minority carriers. By a complex analysis of the minority carries

considering a small-signal perturbation the diode capacitance of a one-sided p-n junction can be expressed as:

$$\mathbf{C} = \left(\frac{\mathbf{1}}{\mathbf{2}\boldsymbol{V_t}}\right)\left(\boldsymbol{I_{p0}}\boldsymbol{\tau_{p0}}\right) \qquad (\mathbf{4.9})$$

As can be seen, the diode capacitance is a function of the thermal voltage (V_t), injected hole current ($\boldsymbol{I_{p0}}$), and the minority hole lifetime ($\boldsymbol{\tau_{p0}}$). However, the minority carrier lifetime is dynamic itself, which leads to a dynamic behavior of C as well. Nevertheless, above turn-on, the diode capacitance dominates the total capacitance as current increases and the junction capacitance decreases with forward applied biases. Thus, at low current densities, the dominant capacitance is the junction capacitance.

The total capacitance of sample 1 and 2 are shown to peak at 260 nF at V ~ 3.3 V and 340 nF at ~ 0.5 V, respectively. Comparing both samples, the peak position of sample 2 is lower than sample 1 with a consistently higher value below turn-on compared to sample 1. In the reverse regime and below turn-on, the capacitance decays as expected since the space-charge capacitance $C_{sc} \sim V^{-1/2}$ in both samples. Since capacitance is a measurement of differential charge over differential voltage, the increase in sample 2 may be attributed to an increase in differential charge. This increase in charge is observed due to the increased carriers from leakage current in sample 2. Thus, we expect sample 2 to achieve its peak total capacitance at a lower voltage since the diode capacitance will dominate the total capacitance at a faster rate due to leakage current as compared to sample 1. As the diode approaches flat band, the space-charge capacitance becomes negligible as minority charge begins to flow across the space-charge region, leading to a

reduction in charge accumulation outside the space-charge region. As the diode capacitance begins to dominate, it is not observed to increase with above-flat-band voltage. This effective "negative" capacitance is a direct result of the dynamic diode capacitance due to the dynamic minority carrier lifetime in equation 4.9. As we will see in the following section the minority carrier lifetime will reduce at higher forward biases.

4.7 Differential minority carrier lifetime in vertical *m*-plane GaN *p-n* diodes

The differential minority carrier lifetime may be determined by the RC time constant of the equivalent circuit (Figure 4.4.b). This can simply be represented as follows:

$$\tau = \mathrm{R} \times \mathrm{C} \tag{4.10}$$

It may be noted that the terms in equation 4.10 are the differential resistance (R) and the total capacitance (C). We have discussed the total capacitance and the relevant components in the forward and reverse regimes of a one-sided *p-n* diode while operated in the reverse bias. Figure 4.7 shows the extracted minority carrier lifetime vs. voltage of the tested samples. The carrier lifetime of sample 1 (continuous-grown) is nominally constant at $\tau \sim 1.4\times10^{-6}$ s for reverse voltages and voltages below turn-on (~2.5V). As the voltage in increased above turn (> 2.5 V), the lifetime dips sharply ($\tau \sim 7.3\times10^{-8}$ s at V = 2.7 V) due to an increase in free carrier current. At higher forward-on voltage the carrier lifetime begins to decrease due to the steadily reducing differential resistance and slightly reducing capacitance.

The differential carrier lifetime observed in sample 2 is quite different, as expected. The peak in carrier lifetime ($\tau \sim 1.4\times10^{-6}$ s) is observed at V = 0V which is nominally the same as sample 1 at the same voltage and at increasing reverse bias. However, the carrier lifetime of sample 2 decreases with increasing reverse biases ($\tau \sim 4.1\times10^{-9}$ s at -10 V). This is expected due to the increased leakage in the reverse regime which is manifested in the reduced differential diode resistance. A similar reduction is observed in the forward off-state as well with a reduced carrier lifetime of sample 2 as compared to sample 1 due to the increased leakage. The observed decrease in carrier lifetime is attributed to the increase in leakage current. As seen previously, the differential diode resistance is lower in sample 2 as compared to sample 1 in this regime. However, the capacitance of sample 2 is larger as compared to sample 1 in the same regime.

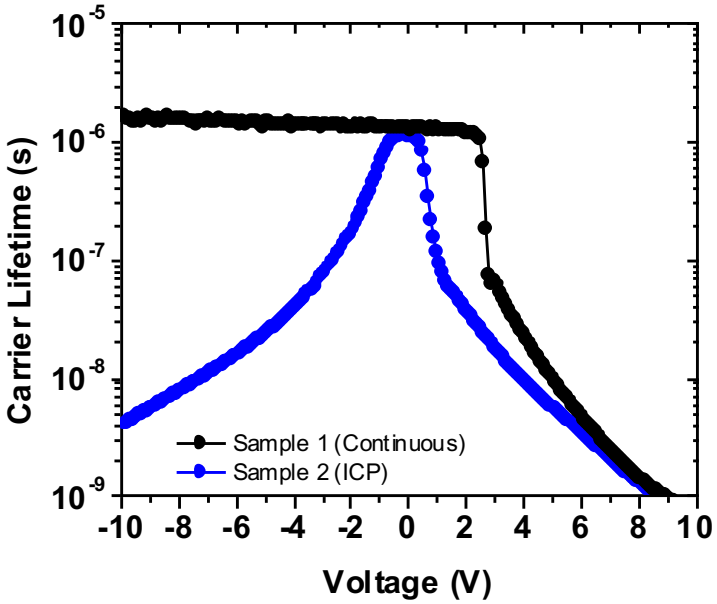

Figure 4.7: Carrier lifetime of continuously-grown and etched-and-regrown *p-n* diodes.

Thus, the effect of the lower differential resistance dominates as the carrier lifetime is lower in sample 2 than sample 1. This implies a mechanism for which carrier current is increased which is measurable by carrier lifetime. The subsequent section will elaborate on this mechanism to give a better understanding of the increased leakage in etched-and-regrown diodes. As forward voltage increases (> 6V), the carrier lifetime reaches nominally the same value as sample 1. As with sample 1, there is a distinct bend in the carrier lifetime at ~1.2 V which we will elaborate on in the next section. This point will be argued where diffusion current begins to dominate recombination current in this sample.

4.8 Origin of forward leakage in etched-and- regrown *m*-plane GaN *p-n* diodes

We have thus calculated the differential minority carrier lifetime as a function of voltage. A decrease in carrier lifetime is observed with increasing current (carriers) density due to the increase in the recombination rate with carrier density. This behavior is in good agreement with an ABC recombination model describing carrier loss mechanisms in GaN devices.[7] Thus, for an increase for A to occur, the lower carrier lifetime in sample 2 (etched-and-regrown) compared to sample 1 (continuous) at low voltages is likely due to trapped carriers at deep level states. Therefore, the recombination rate (R) with units $cm^{-3}s^{-1}$ can be written as:

$$R = C_{n,p} N_t \delta_{n,p} \equiv \frac{\delta_{n,p}}{\tau_{n,p0}} \tag{4.11}$$

The recombination rate is a function of the capture rate or electrons or holes ($C_{n,p}$), the trap density (N_t) and the excess electron or hole concentration $\delta_{n,p}$. By definition the carrier lifetime can be obtained by rearranging equation (4.11) so that:

$$\tau_{n,p0} = \frac{1}{C_{n,p} N_t} \tag{4.12}$$

Deep levels have been observed to significantly increase in etched-and-regrown GaN at $Ec - 1.9$ eV, $Ec - 2.9$ eV, and $Ec - 3.3$ eV [2]. With the elevated deep levels, carriers have a higher probability of being trapped. Thus, a reduction in observed carrier lifetime is expected in the presence of elevated deep-level traps [8], [9].

Now we will investigate the effect of a reduced minority carrier lifetime due to an increased trap density on the currents within a p-n diode. The first current we will analyze is the diffusion current (J_D) which is constituted by minority carriers that diffuse and recombine within the neutral regions and thus induce a current to accommodate this loss of majority carriers. The diffusion current may be written as:

$$J_D = J_s exp\left(\frac{eV_a}{kT}\right) \tag{4.13}$$

The diffusion current is comprised of the total saturation current density (J_s) and the exponential dependency of the applied voltage (V_a). The total saturation current density (J_s) may be expressed as:

$$J_s = \frac{eD_n n_{p0}}{L_n} + \frac{eD_p p_{n0}}{L_p} \tag{4.14}$$

The saturation current denisty (J_s) is comprised of the thermal equilibrium minority carrier electron and hole concentrations (n_{p0} and p_{n0}) , the minority carrier electron and

minority hole diffusion coefficients (D_n and D_p), the minority carrier electron and hole diffusion lengths (L_n and L_p), and the elemental charge (e). Using the relationship $L_{n,p}^2 = D_{n,p}\tau_{n,p0}$ and $n_i^2 = N_d p_{n0}$ and $n_i^2 = N_a n_{p0}$, equation 4.13 can be written as:

$$J_s = en_i^2\left(\frac{1}{N_a}\sqrt{\frac{D_n}{\tau_{n0}}} + \frac{1}{N_d}\sqrt{\frac{D_p}{\tau_{p0}}}\right) \tag{4.15}$$

Thus, we can see that the diffusion current is a function of several parameters including the minority carrier lifetime. As will be shown later, this will be a critical aspect when comparing the leakage currents of the continuous and etched-and-regrown diodes.

The second current present in the forward bias is the recombination current. As electrons and holes diffuse in the sample and drift across the space-charge region the probability exists that some of these carriers will recombined and not become part of the minority carrier distribution. Therefore, the recombination current density may be calculated as:

$$J_{rec} = \int_0^W eR\,dx \tag{4.16}$$

Using Shockley-Read-Hall recombination theory, the recombination rate (R) can be expressed as:

$$R = \frac{np - n_i^2}{\tau_{p0}(n + n') + \tau_{n0}(p + p')} \tag{4.17}$$

It may be noted that the inclusion of the trap density (N_t) is folded into the minority carrier lifetimes (τ_{p0} and τ_{n0}) and the constants related to the trap energy (n' and p'). In order to make the analysis easier, the trap energies may be considered at mid-gap and that

$\tau_{p0} = \tau_{n0} = \tau_0$ so that we may define the recombination current at the maximum recombination rate of electrons and holes as:

$$J_{rec} = \frac{eWn_i}{2\tau_0} exp\left(\frac{eV_a}{2kT}\right) = J_{r0} exp\left(\frac{eV_a}{2kT}\right) \quad (4.18)$$

Again, we see that the recombination current is a function of the minority carrier lifetime. Some assumptions about the trap energies were made to make the analysis easier. However, we will now attempt to identify the dominant current components of the *p-n* diodes using the extracted minority carrier lifetimes.

The diffusion and recombination models are fitted using the extracted minority carrier lifetimes along with extracted values of N_d and W and typical values of D_n and n_i of the continuous (sample 1) and etched-and-regrown (sample 2). The diffusion and recombination current density components are plotted along with the total (sum of the components) and experimentally measured current densities in Figure 4.8. We will first begin by looking at the diffusion current model of equation 4.13 and 14. From the model we observed that we have most of the components except the diffusion coefficients (D_n and D_p), Therefore, the *J-V* curves of each sample will be used to extract these terms. As we have seen, the lifetime behaves dynamically, thus the diffusion coefficients will also be dynamic. Therefore, the diffusion current for both samples is computed and presented in Figure 4.8. It may be noted that the diffusion current is dominant at nominal voltages around the turn-on of the diodes. We can observe that the diffusion current of sample 1 fits relatively well with the measured current density at the diode turn-on. It may be observed that the diffusion current increases "linearly" above ~ 2.5 volts. This behavior is attributed to a lack of series or parasitic resistance in the diffusion model which is present

in the tested diode, which restricts the true exponential rising behavior predicted. Sample 2 has an observed lower voltage (< 1 V) on-set of the diffusion current. It is hard to determine if this is a physical phenomenon or if the simultaneous fitting of the diffusion and recombination model "predicts" the diffusion current to dominate due to the dramatically increase leakage current.

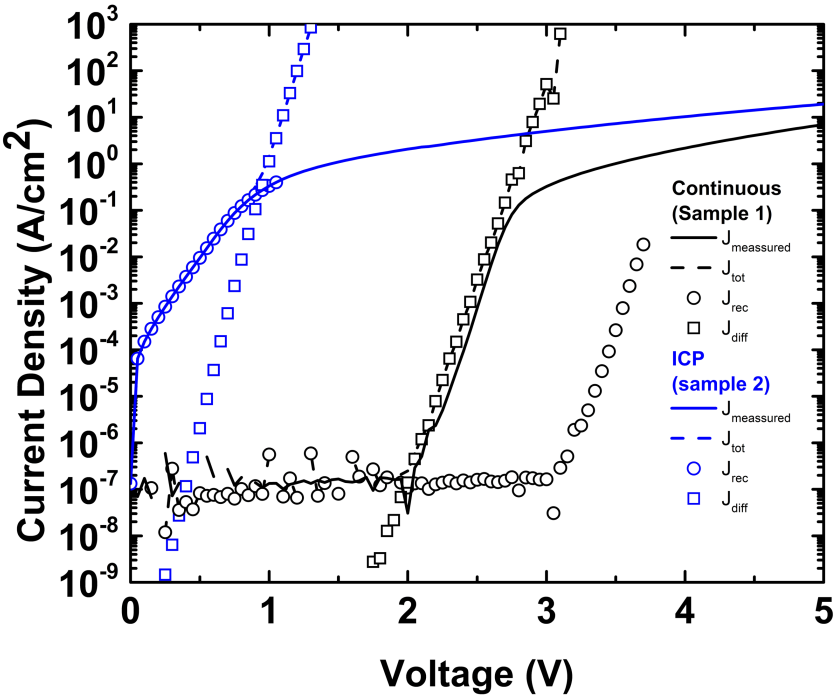

Figure 4.8: Components of forward leakage showing the total current, diffusion current, and recombination current of samples tested

Additionally, we observe the model predicts the diffusion current to rise simultaneously at the same rate in both samples, however with a shift in the on-set. Interestingly, since the on-set is lowered so far back in voltage where the recombination current dominates, the effect of the diffusion current is essentially screened-out during diode turn-on. Even if the diffusion current was similar in sample 2 as in sample 1, the increase in recombination current elevates the current density to sufficient levels which

are influenced by series resistance and high-level injection effects. This explains such a low “turn-on” for the sample 2.

We will now turn our attention to the recombination current for both samples. The recombination current is minimal in sample 1 and predicts an exponential increase at ~ 3V where the applied voltage exceeds the internal built-in voltage. However, the onset of diffusion current dominates strongly at ~ 2 V. Thus, the total diode current is dominated by the diffusion current above these voltages. Therefore, the recombination current is observed to be minimal, which leads to minimal current leakage at below ~2 V. We have discussed the diffusion current in the previous section in relation to sample 2. From the model, the parameter which would shift the effect of the exponential increase which constitutes the sharp rise in diffusion current is the built-in voltage, which is opposite in polarity to the applied voltage V_a. However, it should not be expected for this term to be reduced as it is calculated by the fundamental material characteristics of the p-n junction (N_A, N_d, and n_i). But, in the presence of impurities and defects, compensation of dopants due to point defects or impurities can affect these parameters which can affect the built-in voltage. However, the turn-on (function of V_{bi}), which is primarily associated with diffusion current, may be effectively lowered due the increase in saturation current or leakage current due to recombination current. Therefore, the depletion region collapses pre-maturely, which allows free carrier diffusion to occur more readily which constitutes diode turn-on.

Thus, we have observed the two dominant current components of the samples tested. However, the analysis may be incomplete as many assumptions must be made in order to obtain the complete model for each component. Specifically, the diffusion

coefficients or diffusion lengths must be known in addition to the carrier lifetime to satisfy the model completely. The recombination model also possesses additional challenges in terms of the total integration of the recombination rate across the effective space-charge region. Thus, many assumptions were made specifically based on the trap energy levels and the effective width. These values were extracted from the capacitance and the total area of the device. However, it is difficult to distinguish between the space charge capacitance and differential diode capacitance, especially in the presence of increased carriers due to current leakage. Nevertheless, a general understanding of the leakage mechanisms has been presented in this section, and additional experiments to qualify the leakage mechanisms more accurately will be presented in Chapter 5 (future work).

4.9 Origin of reverse leakage in etched-and- regrown *m*-plane GaN *p-n* diodes

The source of the reverse bias leakage current will be considered in this sub-section. The primary source will be identified as the reverse bias generation current. Under reverse bias we may assume n ~ p~ 0 in the space charge region. However, the presence of generated carriers may be present due to a presence of increased trap levels. Thus, the generation rate can be expressed in equation 4.19 as some of these carriers will recombine and not become part of the minority carrier distribution. Therefore, the recombination current density may be calculated from Shockley-Read-Hall recombination theory as:

$$R = -G = \frac{-C_n C_p N_t n_i^2}{C_n n' + C_p p'} \tag{4.19}$$

The negative sign denotes a negative recombination rate which infers the generation of electron-hole pairs i.e. generation. As carriers are generated, they are swept out of the space-charge region by the reverse bias induced electric field. This generated current (J_{gen}) contributes to the total current (J_R) as this flow of charge is in the direction of reverse-biased current along with the ideal reverse-biased saturation current (J_s) which is presented in equation 4.20.

$$J_R = J_s + J_{gen} \tag{4.20}$$

Similar to the recombination current, the generation current may be determined by the total integration of the generation rate over the applicable width (depletion width). This is show in equation 4.21

$$J_{gen} = \int_0^W eG\, dx \tag{4.21}$$

As with the forward-biased recombination current, we may make some assumptions in order make the integration easier. We may fold the trap density (N_t) and the constants related to the trap energy ($n'\ and\ p'$) into the minority carrier lifetimes ($\tau_{p0}\ and\ \tau_{n0}$) which have been experimentally determined. Furthermore, the trap energies may be considered at mid-gap and that τ_{p0}= $\tau_{n0} = \tau_0$ so that we may define the generation current at the maximum generation rate of electrons and holes. We thus can express the generation current density (equation 4.22) as:

$$J_{gen} = \frac{eWn_i}{2\tau_0} \tag{4.18}$$

Again, we see that the generation current is a function of the minority carrier lifetime using some assumptions about the trap energies in order to make the analysis easier. Therefore, the reverse generation and saturation models are fitted using the extracted minority carrier lifetimes of the continuous (sample 1) and etched-and-regrown (sample 2). The generation and saturation current density components are plotted along with the total (sum of the components) and experimentally measured current densities in Figure 4.9. We will first begin by looking at the saturation current model which is equally valid in the reverse-bias regime with equation 4.13 and 14. We can observe that the reverse saturation of sample 1 fits relatively well with the measured current density throughout the reverse bias sweep. The absence of any increase in saturation currents is consistent with the relatively unchanged carrier lifetimes in the reverse regime for sample 1. The reverse saturation current density of sample 2 also shows a nominally flat behavior with the magnitude increased to ~ $5x10^{-4}$ A/cm^2. The increased magnitude is attributed to the increase saturation current which is even present at V~0V. Interestingly, the carrier lifetime of sample 1 and sample 2 are nominally the same at V = 0V. However, the differential capacitance is higher and the differential resistance is lower, which suggests an increase in injected carriers that contribute to leakage current. Therefore, the diffusion coefficients (D_n and D_p) and/or the carrier concentration (N_a and N_d) are responsible for the difference between sample 1 and sample 2) near V_R = 0V.

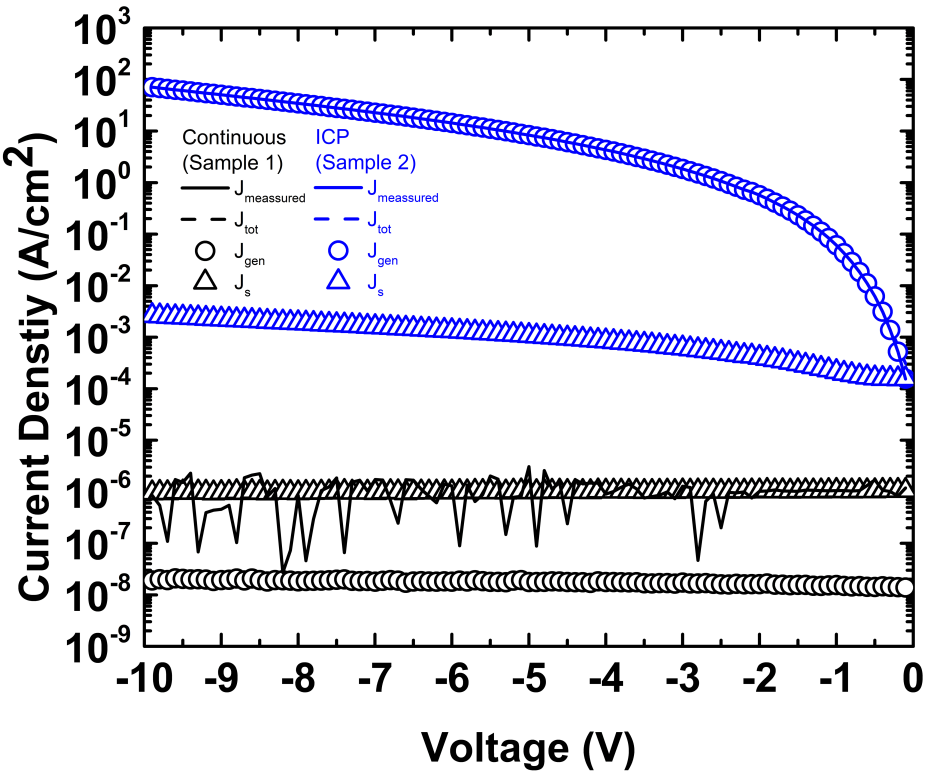

Figure 4.9: Components of reverse leakage showing the total current, generation current, and saturation current of samples tested

Differentiating which term is responsible is again difficult to do. However, if the diffusion lengths are considered to be relatively unaffected, then with reduced carrier lifetime the diffusion coefficient would increase. Nevertheless, as we will see subsequently, the increase in saturation current is dominated by the generation current, and the effect of it is only found near $V_R = 0V$.

We will now consider the reverse bias generation current component of the tested diodes. For sample 1, the generation current is nominally flat at ~ 2 x10^{-8} A/cm^2. Again, the carrier lifetime only nominally increases for sample 1 in reverse bias. Thus, we expect the generation current to only be a function of the expanding depletion width ($W \sim [V/N_d]1^{/2}$) and the generation rate. However, the depletion width only expands ~ 200 nm

from $V_R = 0V$ to $V_R = -10V$ considering the doping. Thus, this increase is only marginally effective in increasing the generation current when considering the base unit of cm in equation 4.18. Nevertheless, the generation current is dominated by the reverse saturation current in the reverse regime for sample 1. Therefore, the total current density is wholly comprised of the saturation current density. However, the generation current density of sample 2 is quite different than sample 1. Since a rapid decrease in carrier lifetime is measure in sample 2, we expect the generation current to increase solely by this metric alone. However, a reduction in the space-charge length (W) is expected with increased reverse biases. Yet, the use of equation 4.18 was determined by several assumptions. Thus, the integral over the generation rate (G) of equation 4.21 is expected to increase due to the presence of deep level traps and the generation current is observed to dominate the total current of sample 2 since the saturation current is substantially lower and only relevant near $V_R = 0V$.

We have now observed the two dominant current components of the samples tested in the reverse bias regime. As with the forward bias models, the analysis may be incomplete as many assumptions must be made in order to obtain the complete model for each component. As mentioned previously, the diffusion coefficients or diffusion lengths must be known, in addition to the carrier lifetime, to satisfy the saturation current model completely. However, the generation model more accurately predicts an increase in generation current for sample 2 (etched-and-regrown) due to an increase in the total integral of the generation rate, even in the presence of an increasing space-charge region. Thus, we have seen that the continuous diode is dominated primarily by the reverse saturation current, and the etched-and-regrown diode is dominated by the generation

current in the reverse bias regimes. As mentioned previously, the analysis presented here has been made with many assumptions and requires more detailed investigation in order to completely understand the leakage mechanisms of etched-and-regrown diodes. However, this analysis gives a general understanding of the physics and qualifies the mechanisms which we expect to dominant in each type of diode, based on experimentally obtained quantities coupled with some first order models for current leakage.

4.10 Summary of leakage mechanisms in planar *m*-plane diodes

Chapter 4 has seen the investigation of a novel RF technique to investigate the leakage mechanism in etched-and-regrown planar *m*-plane GaN *p*-*n* diodes. Rate equations considering carrier diffusion and recombination are used to derive an equivalent electrical small-signal circuit model of fabricated PN diodes to determine the differential resistance, series resistance, and capacitance in fabricated *p*-*n* diodes. Expressions for the input impedance response are fit to experimental data obtained via small signal RF perturbation superimposed on DC voltages in order to extract carrier the circuit parameters. Differences in differential resistance, capacitance, and series resistance between etched-and-regrown devices are compared to continuously grown devices in order to investigate the effects of dry-etched enhanced damage on carrier dynamics. Furthermore, minority carrier lifetimes are extracted from the extracted differential resistance and capacitance.

Electrical results (*J*-*V*) of a continuously grown and dry-etched-and-regrown *p*-*n* diode are compared to their respective extracted circuits elements obtained via the method above. Significant leakage is observed in the dry-etched-and-regrown *p*-*n* diode

versus the continuously grown *p-n* diode. Thus, differences in the extracted circuit elements are observed. Specifically, the minority carrier lifetimes show differences in both the forward and reverse regimes where the current density of each sample is quite different. Thus, a comparison of the relevant leakage components using the carrier lifetimes is conducted to understand the origin of the leakage mechanisms at etched-and-regrown junctions.

The current mechanisms in the forward regime are identified as the forward diffusion current and recombination currents. The continuously grown sample shows a dominant, yet low recombination current below diode turn-on. The model predicts a dominant diffusion current which agrees closely with the measured *J-V* of the continuously-grown diode. Additionally, the etched-and-regrown p-n diode is strongly dominated by recombination current at low biases. However, the magnitude of this current is strongly increased due to differences in carrier lifetime and the increased recombination rate due to deep level traps. Thus, it is observed that diffusion current plays no dominant role in the diode turn-on of the etched-. At higher voltages, diffusion current dominates with addition of the series resistance that reduces current in this regime. The effect of dry-etch enhanced damage is manifested in increased leakage due to an increase in recombination current.

The current mechanisms in the reverse regime are also identified as the reverse saturation current and generation current. The continuously grown sample shows a dominant saturation current throughout the reverse bias regime. The predicted generation current is consistently lower in this sample as well. Furthermore, the etched-and-regrown *p-n* diode is strongly dominated by generation current throughout the reverse bias regime.

Reverse saturation current is increased compared to the continuously grown diode, but it is constantly lower than the generation current, except near 0 V bias. Thus, we expect that generation current is increased due to an increased generation rate due to increased defect levels which lower carrier lifetime. Additionally, the depletion width of the etched-and-regrown diode may not increase with reverse bias. The increase in leakage current may effectively pin the depletion width at a smaller with. However, additional investigation is required to determine this.

The results presented in this chapter have shown a novel approach to extracting small-signal elements which are then used to fit current models in order to explain the leakage mechanisms in etched and regrown lateral *m*-plane *p*-*n* diodes. By understanding the effects of dry etching on these devices, better predictions may be made for the effects of damage at etched-and-regrown junctions for lateral power electronics devices. However, identifying the mechanisms is just the first part of solving the issues with selectively doped power devices on GaN. Thus, the topic of the next chapter (future work) will elaborate on some methods which may be able to mitigate the issues we have observed here.

4.11 References

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Chapter 5 Future Work and Conclusion

This chapter will detail the future work concerning the implementation of vertical selectively-doped power devices on GaN. Topics concerning interfacial impurity mitigation, dry-etched enhanced damage mitigation, leakage current analysis, and more complex device architectures will be elaborated upon. Additionally, a review and conclusion of the dissertation are presented.

5.1 Future work on impurity and dry-etch enhanced damage mitigation

In this section, details on increasing device performance in vertical *m*-plane GaN *p-n* diodes will be presented. As mentioned throughout this body of work, the two main challenges are identified as interfacial impurities and dry-etched enhanced damage. A few proposed methods of investigation to mitigate these challenges will thus be presented. Additionally, future analysis on leakage current mechanisms will also be presented. Thus, a move towards more complex device architectures can be made by understanding and solving some of these underlying challenges for the implementation of vertical selectively-doped power device on GaN. Additionally, some future device architectures will be presented.

5.1.1 Impurity Mitigation

Impurity incorporation has been shown to severely degrade the electrical performance of regrown vatical *m*-plane GaN *p-n* diodes (Chapter 2). Some methods have been investigated already in order to effectively remove impurities utilizing acid dips (HF) and base dips (AZ400K). However, the presence of interfacial impurities remains. Thus, alternative wet-treatment of surface cleaning methods were investigated in

order to completely mitigate their incorporation. Preliminary ozone cleaning experiments have been conducted to determine if impurities may be removed. Ozone treatments are typically used to clean residues during fabrication, and have recently been shown to reduce leakage current in Shottky diodes due to surface passivation [1]. Thus, two *n*-type GaN *c*-plane samples were regrown (one with Ozone treatment and one without at the regrown interface) to see the effect of the ozone procedure. The ozone treatment consisted of a 30 min exposure to UV ozone to generate surface oxides. A subsequent HF dip (3 min) was conducted to remove the oxide and possible impurities as well. Regrowth consisted of ~ 1µm of *n*-GaN. SIMSs results of the two samples were conducted and presented in figure 5.1. It may be observed that the ozone treatment slightly reduced the Si concentration (Si ~ $8x10^{18}$ cm^{-3}) compared to the bare wafer (Si ~ $2x10^{19}$ cm^{-3}). However, we have shown (Chapter 2) that impurity concentrations (> $1x10^{18}$ cm^{-3}) at the regrown interface of p-n diode severely reduced device performance. Therefore, additional experimentation of methods, such as ozone treatments, are further warranted Thus, these methods will be categorized as ex-situ and in-situ.

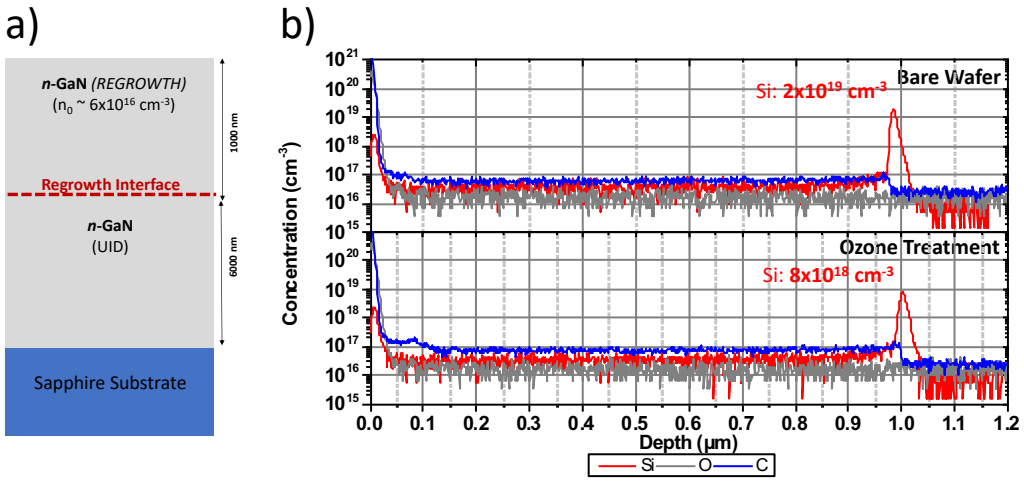

Figure 5.1: a) epitaxial stack for ozone experiment b) SIMS results

Ex-situ methods are conducted on regrown interfaces outside the growth chamber. These include many surface treatments in acids, bases, and in dry-etching chambers. The investigation of acid and base dips have been investigated in this body of work, but additional treatment such as buffered oxide dips (BOE), hydrochloric acid (HCl), agua regia ($HCl:HNO_3$), piranha ($H_2SO_4:H_20:H_2O_2$), Tetramethylammonium hydroxide (TMAH or TMAOH), etc. Furthermore, ex-situ dry-etching techniques such as reactive ion etching RIE and via remote-plasmas, and electrochemical (EC) etching may be used to effectively etch contaminated surfaces away. Due to the lack of ion-bombardment in RIE there may be less etched-enhanced damage on regrown surfaces. EC works on a similar premise as PEC, and may also lead to similar etch-enhanced reduction. Intuitively, these methods should not enhance impurity incorporation or dry-etched damage. However, through careful implementation, they may be able to effectively mitigate impurity incorporation while also reducing dry-etched damage. Additionally, a combination of such treatments may also be investigated. As can easily be seen, there are quite a numerous number of investigations that may be conducted, just in impurity mitigation alone. However, interfacial impurities may still accumulate even if all surface impurities are mitigated by such treatments prior to regrowth since any significant time a surface is exposed to ambient conditions outside a vacuum can increase the likelihood of contamination. Thus, in-situ methods may need to be investigated.

In-situ methods are conducted on regrown interfaces within the growth chamber. These methods may also be applicable for the removal of dry-etched enhanced damaged material as well, effectively mitigating the two primary challenges of selectively-doped regrowth. These methods will be mentioned in the subsequent section for mitigation of

dry-etched enhanced damage on regrown surfaces. One such method is to actively etch the GaN surface during temperature ramp up during regrowth. This may be implemented by flowing the group-V source ammonia while also flowing H_2 before flowing the group-III source TMG and switching to the carrier gas N_2. In this short window, GaN will not be actively grown, but etched under the H_2 ambient. This in-situ etching step may not need to be too long since we have observed ~ 10-20 nm regions of high concentration of interfacial impurities at regrown surfaces. However, this step must be carefully conducted in order to ensure a uniformly etched surface which doesn't increase the surface roughness of the regrown interface. Additionally, novel techniques have been presented using the implementation of Tertiarybutylchloride (TBCl) in order to actively etch GaN in-situ via a HCl formation at the semiconductor surface that actively etches GaN [2]. Since these methods are conducted within the high purity confines of the growth chamber, no additional impurities should be incorporated.

The methods described above to mitigate interfacial impurities are a continuing effort in the pursuit of selectively-doped power electronics on GaN. Thus, by developing novel techniques for impurity mitigation, these high power electronics devices are one step closer to achieving their performance metrics.

5.1.2 Dry-etch enhanced damage mitigation

Dry-etched enhanced damage has been identified and shown to severely degrade the electrical performance of regrown vatical *m*-plane GaN Schottky and *p-n* diodes (Chapter 3). Some methods have already been investigated in order to reduce the effect of dry-etch enhanced damage via surface treatments (AZ400K) and wet etches (PEC). However, the effects of dry-etch enhanced damage have not been shown to be completely

mitigated. Thus, alternative additional investigation of surface treatments and post etches methods must be investigated. Treatments consisting of Tetramethylammonium hydroxide may also be used to post wet-etch defective material after dry etching. Furthermore, enhancements to the PEC method described in this work may be introduced such as electrochemical assistance (applied bias to sample while etching) or multi-stage etched with subsequent lower molarity solutions along with alternative electrolyte solutions (Oxylic Acid, Phosphirc Acid, etc.).

Additionally, dry-etching via ICP may be further calibrated to reduce enhanced damage. ICP etching calibrations have shown (Appendix B) an intimate relationship between defect- enhanced yellow band emission and DC bias in the ICP reactor. Therefore, further investigation may be used to reduce the DC bias further which may also reduce the defectivity from enhanced damage. Previous publications have also shown multi-step dry etches via ICP in order to reduce damage and increase the maximum blocking voltage of *c*-plane GaN p-n diodes [3]. Additionally, reactive ion etching (RIE) may be conducted after ICP etching in order to further reduce etch damage enhanced via ICP. The absence of ion bombardment in RIE is expected to reduce defectivity. Therefore, multi-stage and multi-process dry-etching techniques are viable in further reducing enhanced defects.

As mentioned previously, we may categorize the methods for mitigating dry-etch enhanced damage as ex-situ and in-situ. The methods presented above are all considered ex-situ as they are conducted outside the growth chamber. However, as mentioned in the previous section, some in-situ methods are also possibly viable at reducing dry-etched enhanced damage. Primarily, the implantation of in-situ etching via (TBCl) in order to

actively etch GaN is highly promising since micro-depths of GaN can be etched while maintaining atomically smooth surfaces [2]. This method has the additional advantage of also etching away interfaces plagued by interfacial impurities.

Methods to mitigate dry-etched enhanced damage is a topic of continuing effort with promising advancements. Methods to simultaneously mitigate interfacial impurities and dry-etched enhanced damage are also being developed as well. Thus, solutions to these two major challenges will further enable the implementation of the next generation of selectively-doped power electronics on GaN.

5.2 Future work on leakage current and breakdown analysis

Current leakage was investigated in Chapter 4 using a novel RF method to fit a small-signal equivalent circuit in order to extract dynamic parameters of etched-and-regrown GaN *p-n* diodes. Improvements on the small signal equivalent circuit and leakage current models, and device architecture will be presented below. Additional methods will be introduced as well, in order to determine some of the unknown parameters that are needed to completely satisfy the current leakage models.

5.2.1 Small signal equivalent circuit

The small signal equivalent circuit presented in Chapter 4 has been used to fit experimentally complex impedance values. However, the model assumes an ideal diode model. In the presence of damage enhanced defects the model may break down which requires the implementation of additional circuit elements. Additionally, the measured complex impedance does not fit well to the existing model at high current densities where additional parasitic inductance is observed. Therefore, additional elements may be added

to account for leakage. Such elements may include the addition of a shunt resistor and shunt capacitance as seen in Figure 5.2.

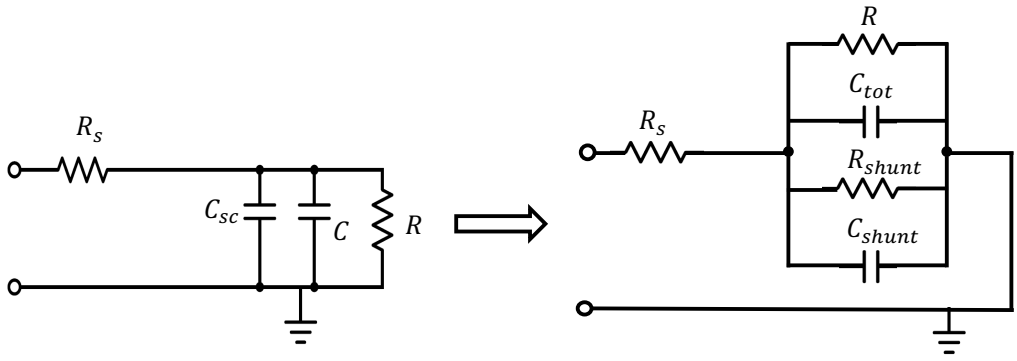

Figure 5.2: Small signal model of p-n diode including shunt resistor and capacitance.

The admittance equation can be written from the small-signal equivalent circuit in equation 5.1. The series resistance (R_s) may also be manually added.

$$Y = j\omega(C_{tot} + C_{shunt}) + \frac{1}{R} + \frac{1}{R_{shunt}} \tag{5.1}$$

By adding the additional shunt elements, an analysis of the leakage current may reveal that a majority of the current flows through these shunt elements. The shunt resistor and capacitance physically represent leakage current paths that are associated with dry-etching damage. Thus, these shunt paths enable the flow of carriers through the metallurgical junctions with a reduced effect of the internal electric field. These leakage mechanisms, which can be represented by the shunt elements, can be present both in the "sub-threshold" forward regime and in the reverse (negative) bias regime. Additionally, the inclusion of an additional RC element within the small-signal equivalent circuit may be able to more easily fit the complex impedance measurement at higher biases due to the addition of another reactive element. Even further additions to the model in Figure 5.2 may include the addition of an RCL (resistor-capacitor-inductor) element which may

represent the observable inductance at higher current regimes. Therefore, a better understanding of the leakage current observed in etched-and-regrown p-n junction may be enabled by the inclusion of additional elements into the small-signal equivalent circuit model.

5.2.2 Leakage current models

Models describing the current observed in forward and reverse biased *p-n* junctions have been presented in Chapter 4. It was observed that key leakage mechanisms can be associated with recombination and generation currents in addition to the diffusion and saturation currents in the forward and reverse bias regimes, respectively. Some assumptions concerning the recombination and generation current were made in order to solve the integral equations (equation 4.16 and 4.21) over the total recombination and generation over the effective width. Details of the diffusion constant and/or diffusion length are also necessary to solve for addition terms for the saturation current which is an integral component to the diffusion current. One proposed method to determine the effective width and minority carrier diffusion length is the implementation of cross-sectional electron beam induced current (EBIC) [4]. Leakage current attributed to dislocation and leakage sites have also been reported via this method on GaN Schottky diodes [5]. Thus, by coupling this technique with the RF technique presented in Chapter 4, a more robust model for the current components within etched-and-regrown diodes may be made.

Additionally, more complex current models may also be incorporated into the analysis of leakage currents in etched-and-regrown p-n diodes. Such models include thermionic and field-emission which excite carriers over or through the potential barrier

of the p-n diodes [6]. Leakage induced by trap-assisted tunneling [7] and variable range hoping [8] may also be considered in the presence of increased deep level states which have been observed in etched-and-regrown diodes (Chapter 3). Tunneling mechanisms such as Fowler-Nordheim and Poole-Frenkel emission may also be considered [6].

By implementing additional methods to determine fundamental carrier dynamics such as diffusion constants, diffusion lengths and implementing additional models which include carrier emission, tunneling, and trap-assisted mechanisms, a more complete understanding of leakage current in etched-and-regrown junctions may be developed.

5.3 Complex design architectures

The movement towards more complex device architectures and ultimately fully developed vertical selectively doped GaN *p-n* diodes and other power electronic devices are proposed for future investigation. Additional test structures for additional RF analysis are also described in this sub-section. Thus, more complex power electronic device architectures may be realized as solutions are developed to meet the challenges concerning the implementation of vertical selective-doping within such devices.

5.3.1 Device Implant Isolation and field plate design

The devices presented previously have all used dry etching via ICP in order to isolate the diodes using mesa structures. However, dry-etch enhanced damage on the mesa sidewall may lead to additional leakage current paths. Typical diodes or LEDs do not suffer from increased leakage at these sidewalls. However, in the presence of extreme reverse bias (> 1 kV), these leakage paths may lead to premature breakdown due to the enormous electric field dropped across the diode. Therefore, device isolation via ion-

implantation is proposed to eliminate the adverse surface current effects. A three-step implantation simulation was conducted using nitrogen (N) ions implanted into GaN to produce vacancies which severely degrade the conductivity of GaN, and effectively isolate any region that is un-implanted. The implantation energy and dose of each step are presented in table 5.1. The target vacancy density is $1x10^{19}$ cm^{-3} or above at a depth of 500 nm.

Table 5.1: Nitrogen ion-implant steps with corresponding implant energy and dose to achieve $1x10^{19}$ cm^{-3} or above at a depth of 500 nm in GaN.

Implant #	Implant energy (keV)	Dose (cm^{-2})
1	60	$5.0x10^{12}$
2	170	$1.0x10^{13}$
3	240	$1.8x10^{19}$

The target depth is determined by extending the vacancies ~100 nm past the metallurgical junction of a *p*-*n* diode with ~ 400 nm of *p*-GaN. A schematic representation of a vertical *m*-plane GaN *p*-*n* diode with device isolation via ion-implantation is presented in Figure 5.3.a. Furthermore, the top-side *p*-GaN and *p*-contact may be protected by a stack consisting of SiO_2 and Ti/Ni with appropriate thicknesses. A stopping and range of ions in matter (SRIM) simulation was performed considering ~ 500 nm of GaN with the nitrogen ion-implantation steps presented in table 5.1. The results of the vacancies versus depth obtained via the simulation, are presented in Figure 5.3.b. The total vacancy density is the summation of the three vacancy densities of each step and it can be observed that the total vacancy density is > $1x10^{19}$ cm^{-3} to a depth of ~ 500 nm.

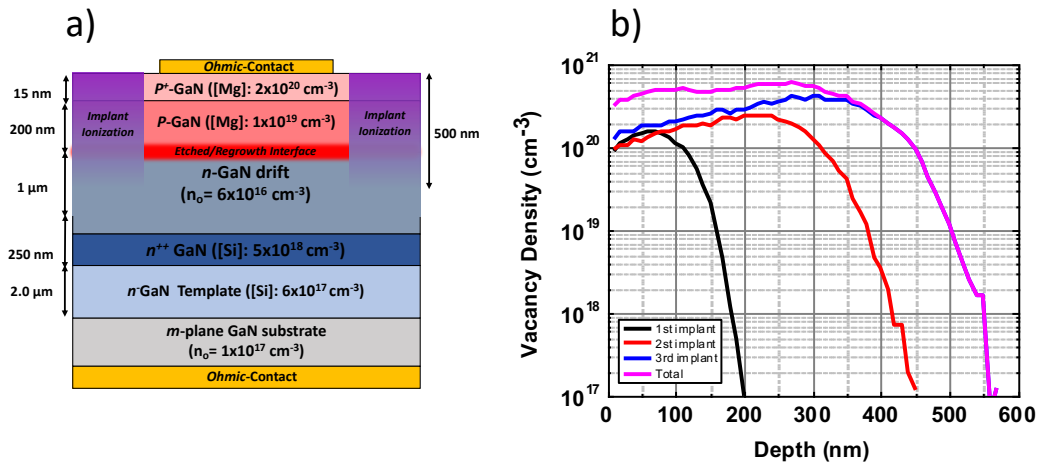

Figure 5.3: a) Vertical m-plane p-n diode with ion-implantation device isolation b) Vacancy density v. depth from SRIM simulation of table 5.1

Additionally, the implementation of field plates have been shown to reduce current leakage and increase blocking voltages in GaN diodes and transistors [9]–[11]. By implementing field plates, the maximum electric field can be reduced via field management which increased the maximum blocking voltage. Additionally, reverse current leakage is suppressed for the same reason. Therefore, device fabrication of diodes or other vertical power devices using ion-implantation isolation and field-plate configurations are realizable in order to achieve higher breakdown voltages and mitigate surface leakage current paths induced by dry-etched mesa isolation.

5.3.2 Vertical p-n diodes for RF analysis

The novel RF approach to extract parameters from a small-signal equivalent circuit was conducted on lateral p-n junction devices (Chapter 4). The lateral configuration was chosen to accommodate the ground signal (GS) RF probe tips which require co-planner *n* and *p*-contacts. However, additional parasitic impedances may arise

due to this configuration. Specifically, the addition of parasitic inductance is expected due to the current path determined by the device architecture. Thus, a move towards a vertical configuration to mitigate the addition of these parasitic impedances may be required. Singular ground (G) and signal (S) RF probe types with a backside-contact would enable this analysis. Additionally, a move towards a vertical geometry for RF testing would allow for the analysis at large reverse biases since the depletion region extends several microns into the n-GaN drift region, as we have seen from design (Chapter 1). A more comprehensive analysis of the carrier dynamics may be observed at diode breakdown.

5.3.3 Vertical selectively-doped p-n diodes

Thus far we have investigated planar devices in order to gain better understanding of the challenges facing the implementation of selectively-doped vertical power devices on GaN. By implementing all additional methods described in this chapter we may produce the planer vertical *m*-plane GaN p-n diode represented in Figure 5.4.a. Additional analysis of this device may represent the maximum possible break-down field that is attainable through the *m*-plane, and expand our understanding of the current leakage mechanisms in this plane. Intuitively, the move toward the selectively-doped vertical GaN p-n diode follows. A schematic representation of such a device, including additional methods as described previously, is represented in Figure 5.4.b. As mentioned in Chapter 1, the *c*-plane most likely will be chosen as the basal-plane in this device architecture due to the manufacturability of its native substrate and also, its ease of growth on foreign substrates (Sapphire, Si, etc.). However, the implementation may also be utilized with the *m*-plane as the basal-plane.

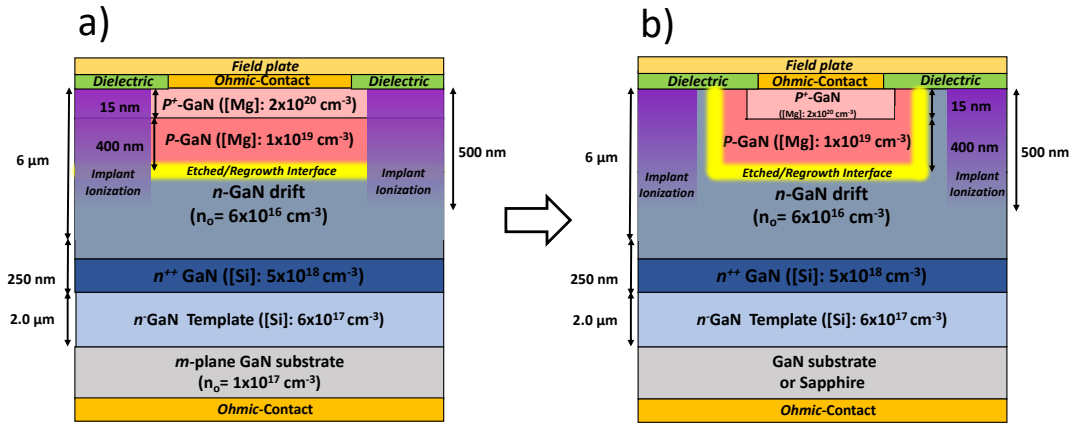

Figure 5.4: a) planar vertical *m*-plane *p-n* diode b) selective-area-doped vertical GaN *p-n* diode

The motivation of this body of work is to enable the implementation of such architectures for the next-generation of power devices on GaN by solving the many challenges using planar architectures. Thus, the full development of such devices with high figure-of-merit performance metrics may be achieved as many of the challenges are investigated and proposed solutions are realized.

5.4 Conclusions

The work presented in this dissertation considers the implementation of vertical selectively-grown power electronics on GaN through the development, experimentation, and analysis of planar *m*-plane GaN diodes. Brief conclusions of all chapters which concentrate on the investigation on *m*-plane GaN diodes are presented below.

In Chapter 1, background information concerning the next generation power electronics is presented. A motivation toward vertical geometries utilizing selectively-doped junctions on GaN is presented due to many advantages over lateral geometries and other material systems. The two primary challenges, namely, impurity incorporation and

dry-etched enhanced damage, are presented first here. A motivation to investigate planar vertical *m*-plane etched-and-regrown junctions as test-bench devices was made due to their simplicity of analysis over vertical selectively-doped. Additionally, little investigation on *m*-plane GaN devices has been conducted for power applications. Some design considerations are also presented to achieve the best possible performance metrics required for *p-n* junctions on *m*-plane GaN.

Chapter 2 presents the investigation of the effects of impurities within planar *m*-plane p-n diodes. Growth rate and doping control effects on background impurity incorporation of MOCVD grown *m*-plane Gan are investigated. Additionally, growth interruptions and surface treatments are investigated with the identification of impurities and their concentrations which are shown to affect the electrical characteristics of planar *m*-plane p-n diodes. Additionally, device architecture changes are shown to slightly mitigate interfacial impurities by moving the regrown junction away from the metallurgical junction of planar *m*-plane *p-n* diodes.

In Chapter 3, the effects of dry-etched enhanced damage on *m*-plane Schottky diodes is presented. Identification of dry-etched enhanced elevated deep level traps and concentrations are analyzed via deep level optical spectroscopy and steady-state photo-capacitance. A few surface treatments and wet etch process are also developed and shown to partially mitigate the deep levels associated with dry-etching. The concentrations of deep levels observed on *m*-plane GaN Schottky diodes are compared to electrical testing in order to identify the effects of such processes. Additionally, electrical characterization of etched-and-regrown *m*-plane GaN *p-n* diodes are compared to the deep-levels observed in associated etched-and-regrown Schottky diodes.

In Chapter 4, a novel electrical characterization method using a radio-frequency (RF) technique is used to experimentally fit a small-signal electrical circuit of etched-and-regrown lateral *m*-plane GaN *p-n* diodes. Dynamic circuit elements are investigated in order to observe the effects of dry-etch enhanced damage in the *p-n* diodes. Additionally, models of the dominant current components are presented in the forward and reverse bias regimes using the extracted minority carrier lifetimes from the RF technique in conjunction with measured *J-V* curves of the p-n diodes.

Lastly, Chapter 5 consists of proposed future work and this conclusion section. Future work focuses on continuing development of selective-doped p-n diodes on GaN for application in power electronic devices. Methods to mitigate the challenges of interfacial impurities and dry-etched enhanced damage consist of several ex-situ and in-situ processes. In-situ processes include surface treatments, multi-stage and multi-type dry etching processes, and improvements to post wet etching. In-situ processes consist of actively etching GaN within the growth chamber via a few proposed methods. Additionally, improvements to the RF small-signal equivalent circuit and improved current models are proposed for the analysis of leakage mechanisms in *m*-plane GaN *p-n* diodes. Furthermore, additional device architectures are presented considering RF testing, device isolation, and electric field management. Furthermore, the implementation of a complete vertical selective-doped *p-n* diode on potentially the *m*-plane orientation with all aforementioned improvements is proposed. Finally, this conclusion section is presented which gives a synopsis of each chapter presented in this dissertation.

In summary, the work presented in this dissertation presents detailed motivations, experiments, and analysis for the investigation of etched-and-regrown vertical m-plane

GaN *p-n* diodes as a testbench for the implementation of vertical selectively-doped power electronics on GaN. Challenges associated with interfacial impurities and dry-etched enhanced damage are identified and analyzed via several methods in order to develop proposed solutions to mitigate them. Implementation of more complex power electronic devices may be more easily realized by understanding and mitigating these challenges at a more rudimentary level. Thus, the work presented here supplements the motivation and implementation of the on-going research and development for power electronics on GaN.

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Appendix A: Supplementary Equations

This appendix provides supplementary information for equations used in this dissertation. The following equations are included: Baliga's Figure-Of-Merit, electric field distribution, and plasma ion flux.

A.1 Baligia's Figure-of-Merit

Baliga's Figure-Of-Merit is used as an indicator of the impact of semiconductor material properties on the resistance of drift regions in power application devices [1]. Specific on-resistance is dependently compared to the maximum breakdown voltage and critical electric field. Thus, the specific on resistance ($R_{sp,on}$ / Ω cm^{-2}) of a one-side p^+n junction can be written as:

$$R_{sp,on} = \left(\frac{W_d}{q\mu_n N_d}\right) \tag{A.1}$$

The specific on-resistance is a function of the depletion width of the n-side (W_d), the elemental charge (q), the mobility of electrons (μ_n), and the doping concentration of n-side (N_d). We may also write the depletion width of the *n*-side at the breakdown voltage as:

$$W_d = \frac{2V_B}{E_c} \tag{A.2}$$

The depletion width at breakdown is thus a function of the breakdown voltage (V_B) and critical electric field (E_C). The *n*-type doping concentration in the drift region at breakdown voltage can also be written as:

$$N_d = \frac{\varepsilon_s E_c^2}{2qV_B} \tag{A.3}$$

The n-type doping concentration is a function of the material permittivity (ε_s), critical electric (E_C) field, elemental charge (q), and breakdown voltage (V_B). By inserting equations A.2 and A.3 into A.1, the specific resistance of the ideal drift region as a function of critical electric field and breakdown voltages is obtained:

$$R_{sp,on} = \frac{4V_B^2}{\varepsilon_s \mu_n E_c^3} \tag{A.4}$$

The term in the denominator of equation A.4 is known as Baliga's Figure-Of-Merit (BFOM). Thus, we may write it as:

$$BFOM = \frac{\varepsilon_s \mu_n E_c^3}{4} \tag{A.5}$$

The form of the BFOM in equation A.5 is a function of the critical permittivity (ε_s), mobility (μ_n), and critical electric field (E_C) of the device. The BFOM may also be written as a function of the specific on-resistance ($R_{sp,on}$) and breakdown voltage (V_B) as:

$$BFOM = \frac{V_B^2}{R_{sp,on}} \tag{A.5}$$

Therefore, the forward bias characteristic specific-on resistance ($R_{sp,on}$) is combined with the reverse bias characteristic breakdown voltage (V_B) and critical electric field (E_C) into a single figure-of-merit known as the Baliga's Figure-Of-Merit.

A.2 Electric Field Distributions

The electric potential (ϕ) and electric field (E) distributions of a *p*-*n* diode can be extracted via Poisson's equation in the one dimension [2]:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{dE(x)}{dx} = \frac{-\rho(x)}{\varepsilon_s} \tag{A.6}$$

The electric fields are found by integrating the volume charge density $\rho(x)$ of equation A.6 over the depletion depths. Thus, the volume charge density $\rho(x)$ is determined by the doping profiles in the respective *p*-type and *n*-type regions:

$$\rho(x) = -eN_a(x), \quad -x_p < x < 0 \tag{A.7}$$

$$\rho(x) = -eN_d(x), \quad 0 < x < x_n \tag{A.8}$$

Boundary conditions of the electric field at the depletion edges and continuity of the electric field displacement at the metallurgical junction are also assumed.

$$E(x = -x_p) = E(x = x_n) = 0 \tag{A.9}$$

$$E(x = 0^+) = \frac{\varepsilon_{s,p}}{\varepsilon_{s,n}} E(x = 0^-) + \frac{Q}{\varepsilon_{s,n}} \tag{A.10}$$

Furthermore, the electric potential (ϕ) is found by integrating over the electric field distribution over the depletion depths. The electric potential is a continuous function, thus continuity is maintained specifically at the metallurgical junction as:

$$\phi(x = 0^+) = \phi(x = 0^-) \tag{A.11}$$

Therefore, by solving Poisson's equation for the specific doping concentration the electric potential and electric field distributions are determined so that the depletion region distances, built-in voltage, and maximum electric field can be tailored. Additionally, an applied bias may be added in order to determine the aforementioned parameters in the presence of an external electric field. Design parameters may be determined via such analysis in order to tailor the doping profiles of a *p-n* diode, increase the maximum blocking voltages, and reduce the maximum critical electric field. Furthermore, the inclusion of highly doped impurity concentrations may be analyzed via similar analysis in order to predict the distribution of electric fields in regrown/treated *p-n* diodes.

A.3 Plasma ion flux

The ion flux of a cylindrical discharge having low voltage sheaths at all surfaces can be calculated via the following equations [3]. The ion mean free path may be written in terms of the gas density (n_g) and the total ion–atom scattering cross section for low-energy ion σ_i of a specific gas:

$$\lambda_i = \frac{1}{n_g \sigma_i} \qquad (A.12)$$

Therefore, the center-to-edge density axial ratio (h_l) and radial ratio (h_R) considering the area density of surface sites ($n_{sl}\ and\ n_{sR}$) along the length (l) and radius (R) to the total area density of surface sites ($\mathrm{n_0}$) of a cylindrical configuration may be written as:

$$h_l \equiv \frac{n_{sl}}{n_0} \approx 0.86\left(3 + \frac{l}{2\lambda_i}\right)^{-1/2} \qquad (A.13)$$

$$h_R \equiv \frac{n_{sR}}{n_0} \approx 0.80\left(4 + \frac{R}{\lambda_i}\right)^{-1/2} \quad (A.14)$$

Additionally, the effective plasma size for particle loss (d_{eff}), which is a function of the effective area (A_{eff}) of particle loss and geometric configuration, may be written in terms of the center-to-edge density axial ratios($n_{sl}\ and\ n_{sR}$) as:

$$d_{eff} = \frac{\pi R^2 l}{A_{eff}} = \frac{1}{2}\frac{Rl}{Rh_l + lh_R} \quad (A.15)$$

The total energy loss per electron pair ($\mathcal{E}_T$) may be written in terms of the collisional energy lost per electron–ion pair ($\mathcal{E}_c$), the mean kinetic energy lost per electron ($\mathcal{E}_e$), and the mean kinetic energy lost per ion ($\mathcal{E}_i$) as:

$$\mathcal{E}_T = \mathcal{E}_c + \mathcal{E}_e + \mathcal{E}_i \quad (A.16)$$

The Bohm velocity (u_B) may be written in terms of the elemental charge (e), electron temperature (T_e), and the mass of the ion species (M).

$$u_B = \sqrt{\frac{eT_e}{M}} \quad (A.17)$$

Thus, the total area density of surface sites (n_0) or plasma density can be written in terms of plasma absorbed power (P_{abs}), the elemental charge (e), the Bohm velocity (u_B), and the total energy loss per electron pair ($\mathcal{E}_T$):

$$n_0 = \frac{P_{abs}}{eu_B A_{eff}\mathcal{E}_T} \quad (A.18)$$

Therefore, the ion flux at the axial boundary can be determined via:

$$\Gamma_{il} = n_0 h_l u_B \quad (A.19)$$

Additionally, the ion current may be obtained from the ion flux via the configuration of the plasma chamber, ion species, and associated parameters.

A.4 References

[1] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Springer Science & Business Media, 2010.

[2] M. Snider, *Microelectronics: An Integrated Approach*. Scientific e-Resources, 2018.

[3] M. A. Lieberman and A. J. Lichtenberg, *Principles of Plasma Discharges and Materials Processing*. John Wiley & Sons, 2005.

Appendix B: Growth and Fabrication

This appendix provides supplementary information on the growth and fabrication of devices mentioned in this dissertation. Calibrations of Inductively Coupled Plasma (ICP) and Photoelectrochemical etching (PEC) are also presented.

B.1 Growth of Gallium Nitride (GaN)

In this section we will elaborate on more details of the growth via Metal Organic-Chemical Vapor Deposition (MOCVD) of GaN. We will pay specific attention to the growth of non-polar (1010) *m*-plane GaN. The use of a VEECO P75 TurboDisc MOCVD was used for the duration of the growth for all structures mentioned in this dissertation. Both a schematic and picture of the growth chamber are presented in figure B.1.

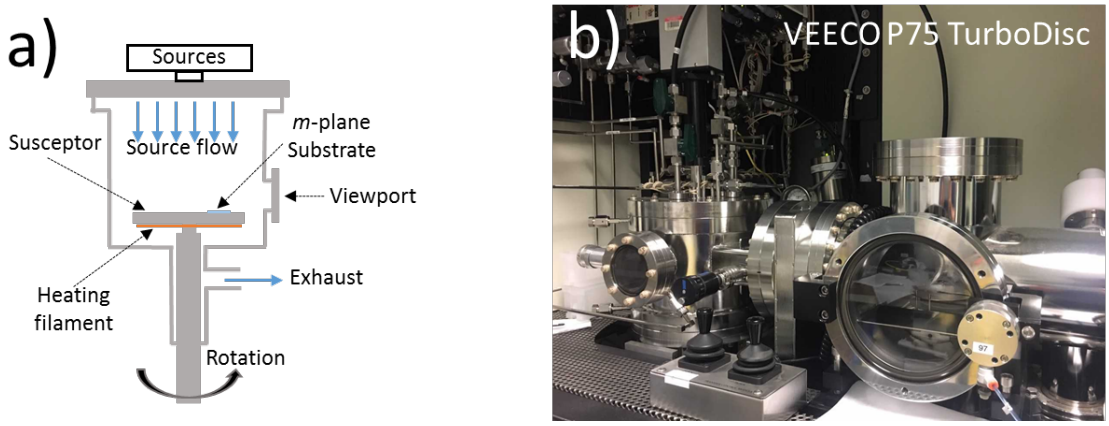

Figure B.1: a) schematic representation of MOCVD growth chamber, b) picture of VEECO P75 TurboDisc MOCVD

The growth chamber consists of sealed chamber which is kept under vacuum when not in operation using an EBARA A25S dry vacuum pump. Source gases are introduced to the chamber through a "shower head" apparatus. Gas flows and pressures are controlled by a

network of mass flow controllers (MFCs) and throttle valves. The substrates are placed on a specialized platform known as a "susceptor" which is engineered to withstand high temperature, reduce outgassing and contamination, and accommodate the footprint of the substrates. The susceptor sits on-axis with a spindle which allows the susceptor to be rotated during growth. A susceptor is specify designed to hold the *m*-plane substrate with ~ 1 cm offset to the axis of rotation of the spindle due to a uniform flow balance observed at this distance. The susceptor and substrate are simultaneously heated through convection via a heating filament directly below the susceptor. Susceptors are easily transferred into the growth chamber via a load-lock chamber attached to each other with a gate-valve to isolate each, respectively.

B.1.1 GaN metal organic sources

The reaction equation and source gases which constitute the growth of GaN will be presented in this subsection. Since GaN is a III-V semiconductor, the use of a group-III and group-V metalorganic (MO) sources are required. The group-III source MO for Ga is Trimethylgallium ($Ga(CH_3)_3$), which at room temperature is a liquid. Group-III MO is converted to a gaseous state via a source bubbler. Carrier gas (N_2) flows through the liquidous MO so that the vapor is incorporated within the carrier gas flow. The gas exiting the bubbler is a saturated mixture of MO vapor dissolved in the carrier gas. The group-V source MO is Ammonia (NH_3). Ammonia is stored in a gaseous state within compressed gas cylinders. Thus, we have the primary MOs for growth of GaN which is stoichiometrically determined by the reaction expressed in equation B.1.

$$Ga(CH_3)_3 + NH_3 \rightarrow GaN + CH_4 \qquad (B.1)$$

Elevated temperatures in the reactor induce the chemical interaction, resulting in the deposition of GaN on the substrate and a resultant methane (CH_4) gas. An additional carrier gas (N_2) is added to the aforementioned MOs in order to more easily stabilize the reaction within the chamber. The flow of gases and resulting products (CH_4) are flowed out of the exhaust outlet and scrubbed before leaving to atmosphere.

B.1.2 Doping of GaN

Controlled doping of GaN can be achieved through intentional impurities incorporated into the GaN crystal. Thus, the electronic properties of doping are determined by the addition of donor or acceptor atoms within the crystalline lattice. Typically, donors are introduced through the incorporation of Si atoms which substitute Ga atoms in the lattice (Si_{Ga}). This interstitial defect is very predictable since the formation energy is the lowest for this type of interstitial defect when considering Si incorporation [1] . Therefore, the donor impurity Si is introduced into the reaction of equation A.1 via Silane (SiH_4) gas. Silane is stored in compressed gas cylinders and controlled flow into the MOCVD through MFCs. The concentration of doping can be tailored by the flow of Silane and also the III-V ratio of the MOs. Additional information on this can be found in Chapter 2.

The implementation of *p*-type GaN has been a goal throughout the history of III-N material systems. A widely praised method was developed such that acceptors are introduced and activated through the incorporation of Mg atoms through acceptor Mg-H complexes which are formed in H_2 ambientes growth conditions [2]. Therefore, p-type

material is grown in H_2 ambient at lower temperatures to mitigate the effect of hydrogen etching. The Mg-H complexes are removed via high temperature anneal where the H diffuses out of the crotaline lattice leavening the ionized acceptor Mg. Therefore, the acceptor impurity Ga is introduced into the reaction of equation B.1 via Magnesium bis-cyclopentadienyl (Cp_2Mg). Magnesium bis-cyclopentadienyl is stored in liquidous form and introduced into the MOCVD in gaseous form though a bubbling process similar to Trimethylgallium. Again, the concentration of doping can be tailored by the flow of Cp_2Mg and also the III-V ratio of the MOs, and post anneal conditions. Additional information on this can be found in Chapter 2.

B.1.3 Recipes for GaN Growth

The recipes of *m*-plane GaN vertical p-n diodes will be presented here. The first recipe presented is for a continuously grown *p-n* diode. The details of the growth are given in table B.1. The first 5 layers ramp up the turbo disk (1500 RPM), chamber pressure (500 mTorr), temperature (644ºC at thermocouple / 950ºC by pyrometer), N_2 flow (3710 sccm), Ammonia flow (2100 sccm), set the flow balance, and flow the TMG and Silane source (vented to exhaust). In steps 6 though 7 the growth temperature is reached and all source gases are flown into the chamber to initiate the growth of the ~ 1μm (30 min) of the template GaN. In step 8 the silane flow is increased to constitute the 250 nm (7.5 min) of n^+ - GaN. In step 9 the Silane flow is reduced in order to achieve the lowest possible controllable n-doping. This layer constitutes the 5 μm (150 min) n^- -drift region. In layer 10-12 the turbo disk speed is reduced (750 RPM), Growth pressure reduced (205 mTorr) temperature is reduced (590ºC at thermocouple / 830ºC by pyrometer), N_2 flow stopped, H_2 flow (3500 sccm) ammonia flow reduced (2000 sccm),

flow balance adjusted, TMG adjusted and vented, Silane stopped, and Cp_2Mg flowed and vented.

Table B.1: MOCVD recipe for continuously grown vertical m-plane GaN p-n diode

		layer 1	layer 2	layer 3	layer 4	layer 5	layer 6	layer 7	layer 8	layer 9
	Time	01:00.0	03:00.0	09:00.0	01:30.0	01:00.0	00:00.0	00:30.0	7:30.0	150:00.0
	Grow		NH3#1	NH3#1	NH3#1	NH3#1	TMGa, NH3#1, Si	TMGa, NH3#1, Si	TMGa, NH3#1, Si	TMGa, NH3#1, Si
Turbo Disc Speed	Motor33	100	600	1500	1500	1500	1500	1500	1500	1500
	Ramp33	1	1	1	0	0	0	0	0	0
GC Press	Press38	10	100	500	500	500	500	500	500	500
	Ramp38	0	1	1	0	0	0	0	0	0
GC Temp	Temp34	40	160	644	644	644	644	644	644	644
	Ramp34	1	1	1	0	0	0	0	0	0
H2	MFC45	0	0	0	0	0	0	0	0	0
	Ramp45	1	0	0	0	0	0	0	0	0
	CMD45	RUN	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE
N2	MFC44	1000	1000	3710	3710	3710	3710	3710	3710	3710
	Ramp44	0	0	1	0	0	0	0	0	0
	CMD44	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN
NH3#1	MFC46	0	500	2100	2100	2100	2100	2100	2100	2100
	Ramp46	0	1	1	0	0	0	0	0	0
	CMD46	IDLE	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN
Hyd Push	MFC56	100	500	1000	1000	1000	1000	1000	1000	1000
	Ramp56	0	1	1	0	0	0	0	0	0
Inlet Purge	MFC57	100	500	2000	2000	2000	2000	2000	2000	2000
	Ramp57	0	1	1	0	0	0	0	0	0
GC Purge	MFC53	100	500	1500	1500	1500	1500	1500	1500	1500
	Ramp53	0	1	1	0	0	0	0	0	0
	CMD53	ON	ON	ON	ON	ON	ON	ON	ON	ON
Alk H2/N2 Select	CMD_S	N2	N2	N2	N2	N2	N2	N2	N2	N2
INJ H2/N2 Select	CMD_S	N2	N2	N2	N2	N2	N2	N2	N2	N2
Alk GC Press	Press25	350	720	720	720	720	720	720	720	720
	Ramp25	0	1	0	0	0	0	0	0	0
Alk Inner	MFC55	60	60	235	235	235	235	235	235	235
	Ramp55	0	1	1	0	0	0	0	0	0
Alk Outer	MFC58	60	200	590	590	590	590	590	590	590
	Ramp58	0	1	1	0	0	0	0	0	0

Push Inner	MFC62	60	70	228	228	228	228	228	228	228
	Ramp62	0	1	1	0	0	0	0	0	0
Push Outer	MFC64	60	230	905	905	905	905	905	905	905
	Ramp64	0	1	1	0	0	0	0	0	0
TMGa	MFC5	50	34	34	34	34	34	34	34	34
	Ramp5	0	1	0	0	0	0	0	0	0
	CMD5	IDLE	VENT	VENT	VENT	VENT	RUN	RUN	RUN	RUN
TMGa Push	MFC17	60	42	42	42	42	42	42	42	42
	Ramp17	0	1	0	0	0	0	0	0	0
TMGa DD	MFC18	10	34	34	34	34	34	34	34	34
	Ramp18	0	1	0	0	0	0	0	0	0
TMGa Press	Press12	900	900	900	900	900	900	900	900	900
	Ramp12	0	0	0	0	0	0	0	0	0
SiH4	MFC47	0	10	10	10	10	10	20	20	1
	Ramp47	0	1	1	0	0	0	1	0	1
	CMD47	IDLE	VENT	VENT	VENT	VENT	RUN	RUN	RUN	RUN
SiH4 Press	Press51	900	900	900	900	900	900	900	900	900
	Ramp51	0	0	0	0	0	0	0	0	0
SiH4 Push	MFC49	0	1000	1000	1000	1000	1000	500	500	1000
	Ramp49	0	1	1	0	0	0	1	0	1
SiH4 DD	MFC50	0	10	10	10	10	10	20	20	1
	Ramp50	0	1	0	0	0	0	1	0	1
Cp_2Mg	MFC1	0	0	0	0	0	0	0	0	0
	Ramp1	0	0	0	0	0	0	0	0	0
	CMD1	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE
Cp_2Mg Press	Press8	900	900	900	900	900	900	900	900	900
	Ramp8	0	0	0	0	0	0	0	0	0

		layer 10	**layer 11**	**layer 12**	**layer 13**	**layer 14**	**layer 15**	**layer 16**	**layer 17**
	Time	07:00.0	00:30.0	00:30.0	30:00.0	00:06.0	04:30.0	14:00.0	01:00.0
	Grow	NH3#1	NH3#1	NH3#1	Mg, TMGa , NH3#1	Mg, TMGa , NH3#1	Mg, TMGa , NH3#1	NH3#1	
Turbo Disc Speed	Motor33	800	750	750	750	750	750	100	0
	Ramp33	1	1	0	0	0	0	1	1
GC Press	Press38	205	205	205	205	205	205	10	10
	Ramp38	1	1	0	0	0	0	1	0
GC Temp	Temp34	590	590	590	590	590	590	40	0
	Ramp34	1	0	0	0	0	0	1	1
H2	MFC45	3500	3500	3500	3500	3500	3500	1000	1000

	Ramp45	1	1	0	0	0	0	1	0
	CMD45	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN
N2	MFC44	0	0	0	0	0	0	1000	1000
	Ramp44	1	0	0	0	0	0	1	0
	CMD44	RUN	IDLE	IDLE	IDLE	IDLE	IDLE	RUN	RUN
NH3#1	MFC46	2000	2000	2000	2000	2000	2000	0	0
	Ramp46	1	0	0	0	0	0	1	0
	CMD46	RUN	RUN	RUN	RUN	RUN	RUN	RUN	IDLE
Hyd Push	MFC56	500	500	500	500	500	500	100	100
	Ramp56	1	0	0	0	0	0	1	0
Inlet Purge	MFC57	1900	1900	1900	1900	1900	1900	100	100
	Ramp57	1	0	0	0	0	0	1	0
GC Purge	MFC53	1500	1500	1500	1500	1500	1500	100	100
	Ramp53	0	0	0	0	0	0	1	0
	CMD53	ON	ON	ON	ON	ON	ON	ON	ON
Alk H2/N2 Select	CMD_S	N2	N2	N2	N2	N2	N2	N2	N2
INJ H2/N2 Select	CMD_S	N2	N2	N2	N2	N2	N2	N2	N2
Alk GC Press	Press25	700	700	700	700	700	700	700	700
	Ramp25	1	0	0	0	0	0	0	0
Alk Inner	MFC55	83	83	83	83	83	83	60	60
	Ramp55	1	0	0	0	0	0	1	0
Alk Outer	MFC58	77	77	77	77	77	77	60	60
	Ramp58	1	1	0	0	0	0	1	0
Push Inner	MFC62	63	63	63	63	63	63	60	60
	Ramp62	1	0	0	0	0	0	1	0
Push Outer	MFC64	387	387	387	387	387	387	60	60
	Ramp64	1	0	0	0	0	0	1	0
TMGa	MFC5	25	25	25	25	10	10	0	0
	Ramp5	1	0	0	0	1	0	1	0
	CMD5	VENT	VENT	VENT	RUN	RUN	RUN	IDLE	IDLE
TMGa Push	MFC17	40	40	40	40	45	45	45	45
	Ramp17	1	0	0	0	1	0	0	0
TMGa DD	MFC18	25	25	25	25	10	10	10	10
	Ramp18	1	0	0	0	1	0	0	0
TMGa Press	Press12	900	900	900	900	900	900	900	900
	Ramp12	0	0	0	0	0	0	0	0
SiH4	MFC47	0	0	0	0	0	0	0	0
	Ramp47	0	0	0	0	0	0	0	0
	CMD47	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE
SiH4 Press	Press51	900	900	900	900	900	900	900	900

	Ramp51	0	0	0	0	0	0	0	0
SiH4 Push	MFC49	200	200	200	200	200	200	200	200
	Ramp49	0	0	0	0	0	0	0	0
SiH4 DD	MFC50	10	10	10	10	10	10	10	10
	Ramp50	0	0	0	0	0	0	0	0
Cp2Mg	MFC1	60	60	60	60	120	120	0	0
	Ramp1	0	0	0	0	1	0	1	0
	CMD1	VENT	VENT	VENT	RUN	RUN	RUN	IDLE	IDLE
Cp2Mg Press	Press8	900	900	900	900	900	900	900	900
	Ramp8	0	0	0	0	0	0	0	0

In layer 13 of the recipe, TMG and Cp_2Mg are run into the reactor constituting the 400 nm (30 min) p-GaN layer. In layer 14 the Cp_2Mg flow is adjusted for higher incorporation and in layer 15 the 15 nm (4.5 min) p^+-GaN layer is grown. In layers 16 and 17 the temperature, turbo disk RPM, and all source gasses are ramped down in order to conclude the growth. Subsequent post grown annealing at ~700ºC is conducted for 15 minutes to activate the Mg acceptors within the *p*-GaN layers.

The second recipe we will discuss is a regrown *p-n* diode. The details of the growth are presented in table B.2. The growth is performed on samples of GaN which have been grown previously with the underlying template, n^+ region, and n^- -drift regions grown. These are grown by the first 9 layers of the previous recipe (table B.1). As mentioned in the body of this dissertation, many surface treatments and etches may be done to these samples before regrowth. Nevertheless, the first 5 layers ramp up the turbo disk speed (1500 RPM), chamber pressure (500 mTorr) temperature (590ºC at thermocouple / 830ºC by pyrometer),N_2 flow (3500 sccm), Ammonia flow (2000 sccm), set the flow balance, flow the TMG source (vented to exhaust), Cp_2Mg flow is set

(vented to exhaust). In step 6 the growth temperature is reached and all source gases are flown into the chamber to initiate the growth of the ~ 400nm (30 min) of the p-GaN layer. In layer 7 the Cp_2Mg flow is adjusted for higher incorporation, and in layer 8 the 15 nm (4.5 min) p^+-GaN layer is grown. In layers 9 and 10 the temperature, turbo disk RPM, and all source gasses are ramped down in order to conclude the growth. Subsequent post grown annealing at ~700ºC is conducted for 15 min to activate the Mg acceptors within the *p*-GaN layers.

Table B.2: MOCVD recipe for etched-and-regrown vertical *m*-plane GaN *p-n* diode

		layer 1	layer 2	layer 3	layer 4	layer 5	layer 6	layer 7	layer 8	layer 9	layer 10
	Time	01:00.0	03:00.0	11:00.0	00:30.0	00:30.0	30:00.0	00:06.0	04:30.0	14:00.0	01:00.0
	Grow		NH3#1	NH3#1	NH3#1	NH3#1	Mg, TMGa, NH3#1	Mg, TMGa, NH3#1	Mg, TMGa, NH3#1	NH3#1	
Turbo Disc Speed	Motor33	100	500	750	750	750	750	750	750	100	0
	Ramp33	1	1	1	0	0	0	0	0	1	1
GC Press	Press38	10	100	205	205	205	205	205	205	10	10
	Ramp38	0	1	1	0	0	0	0	0	1	0
GC Temp	Temp34	40	160	590	590	590	590	590	590	40	0
	Ramp34	1	1	1	0	0	0	0	0	1	1
H2	MFC45	1000	1000	3500	3500	3500	3500	3500	3500	1000	1000
	Ramp45	1	0	1	0	0	0	0	0	1	0
	CMD45	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN
N2	MFC44	1000	0	0	0	0	0	0	0	1000	1000
	Ramp44	0	1	0	0	0	0	0	0	1	0
	CMD44	RUN	RUN	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	RUN	RUN
NH3#1	MFC46	0	500	2000	2000	2000	2000	2000	2000	0	0
	Ramp46	0	1	1	0	0	0	0	0	1	0
	CMD46	IDLE	RUN	RUN	RUN	RUN	RUN	RUN	RUN	RUN	IDLE
Hyd Push	MFC56	100	500	500	500	500	500	500	500	100	100
	Ramp56	0	1	0	0	0	0	0	0	1	0
Inlet Purge	MFC57	100	500	1900	1900	1900	1900	1900	1900	100	100
	Ramp57	0	1	1	0	0	0	0	0	1	0
GC Purge	MFC53	100	500	1500	1500	1500	1500	1500	1500	100	100
	Ramp53	0	1	1	0	0	0	0	0	1	0
	CMD53	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
Alk H2/N2 Select	CMD_S	N2	N2	N2	N2	N2	N2	N2	N2	N2	N2

INJ H2/N2 Select	CMD_S	N2	N2	N2	N2	N2	N2	N2	N2	N2	N2
Alk GC Press	Press25	350	700	700	700	700	700	700	700	700	700
	Ramp25	0	1	0	0	0	0	0	0	0	0
Alk Inner	MFC55	60	60	83	83	83	83	83	83	60	60
	Ramp55	0	1	1	0	0	0	0	0	1	0
Alk Outer	MFC58	60	77	77	77	77	77	77	77	60	60
	Ramp58	0	1	0	0	0	0	0	0	1	0
Push Inner	MFC62	60	63	63	63	63	63	63	63	60	60
	Ramp62	0	1	0	0	0	0	0	0	1	0
Push Outer	MFC64	60	230	387	387	387	387	387	387	60	60
	Ramp64	0	1	1	0	0	0	0	0	1	0
TMGa	MFC5	25	25	25	25	25	25	10	10	0	0
	Ramp5	1	0	0	0	0	0	1	0	1	0
	CMD5	IDLE	VENT	VENT	VENT	VENT	RUN	RUN	RUN	IDLE	IDLE
TMGa Push	MFC17	40	40	40	40	40	40	45	45	45	45
	Ramp17	1	0	0	0	0	0	1	0	0	0
TMGa DD	MFC18	25	25	25	25	25	25	10	10	10	10
	Ramp18	1	0	0	0	0	0	1	0	0	0
TMGa Press	Press12	900	900	900	900	900	900	900	900	900	900
	Ramp12	0	0	0	0	0	0	0	0	0	0
SiH4	MFC47	0	10	15	15	15	0	0	0	0	0
	Ramp47	0	1	1	0	0	0	0	0	0	0
	CMD47	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE	IDLE
SiH4 Press	Press51	900	900	900	900	900	900	900	900	900	900
	Ramp51	0	0	0	0	0	0	0	0	0	0
SiH4 Push	MFC49	0	1000	500	500	500	200	200	200	200	200
	Ramp49	0	1	1	0	0	0	0	0	0	0
SiH4 DD	MFC50	0	15	15	15	15	10	10	10	10	10
	Ramp50	0	1	0	0	0	0	0	0	0	0
Cp_2Mg	MFC1	0	0	60	60	60	60	120	120	0	0
	Ramp1	0	0	0	0	0	0	1	0	1	0
	CMD1	IDLE	IDLE	VENT	VENT	VENT	RUN	RUN	RUN	IDLE	IDLE
Cp_2Mg Press	Press8	900	900	900	900	900	900	900	900	900	900
	Ramp8	0	0	0	0	0	0	0	0	0	0

We have thus analyzed the two primary growth recipes for this body of work. Additional steps may be included/excluded in order to tailor the epitaxial structures for the desired structure. For example, Steps 1-9 of table B.1 may be grown with a subsequent regrowth utilizing steps 1-6 (changing the time of step 6) to regrow n-drift

after surface/etching treatments in order to constitute a Schottky diode structure. The same methodology may be applied to buried vertical *p-n* diodes and lateral *p-n* diodes. While these recipes are calibrated to the specific MOCVD reactor used, a general understanding of the growth parameters may be taken away from this discussion.

B.2 Fabrication of GaN diodes

The details of the lithographic and deposition processes for fabrication of the GaN diodes structures analyzed in this body of work are presented. These structures include vertical *p-n* diodes, lateral *p-n* diodes, and vertical Schottky diodes.

B.2.1 Vertical p-n diodes

The procedure for varication of vertical p-n diodes is detailed in Table B.3 with a photolithographic process flow in Figure B.2. After the *p-n* didoes are epitaxially grown by MOCVD they are labeled with a diamond scribed before a 3X clean consisting of Agua-Regia (HCl: HNO_3) in a 3:1concentration at 80ºC for 15 min. This procedure ensures the removal of all surface contamination, specifically metals which may be used for quick testing of the diodes. Subsequent, solvent cleaning consisting of 3-min dips in Acetone (C_3H_6O) and Isopropyl Alcohol (C_3H_8O) followed by a 3-min rinse in Deionized (DI) water in order to clean any remaining contamination of the sample surface. The samples are then dehydrated using a hotplate at 110 ºC for 5 min.

The first major step is the *p*-contact deposition. Thus, a negative photoresist (AZnLOF2020) is spun on the samples at 3000 RPM for 30s. Typical samples sized are on the order of ~ 5mm X 5mm. Therefore, a non-uniform distribution of photoresist accumulates at the edge of the samples. This “edge bead” is removed with the use of a razor blade to ensure uniform contact of the surface to the photo-mask during exposure.

The samples are then “soft” baked at 110 ºC for 90 s to ensure a proper “hardening” of the photoresist before exposure. Using a Karl Suess MJB3 mask aligner, the samples are then aligned to the “p-contact” layer on the photomask which consists of circular patterns (150, 250, 350, and 450 μm). The samples are exposed for 7 s with an output power and wavelength of 3.5 mW/cm^2 and 365 nm, respectively. A post bake is performed at 110 ºC for 60 s to ensure proper viscosity of the resist for development. The samples are subsequently developed in a base solution (AZ300MIF) 80 s and rinsed in flowing DI for 2 min. An acid dip of buffered oxide etch (BOE 6:1) is performed on the samples for 1 min followed by a 2 min DI rinse in order to remove any oxides since the *p*-metal stacks will adhere to the GaN surface. This acid dip procedure is performed immediately before loading the samples into an e-beam deposition chamber. The e-beam deposition chamber is brought down to a base pressure of 2.0×10^{-6}torr before deposition. The p-metal stack (Pd/Au) is subsequently deposited with a thickness of 20nm and 300nm respectively. The deposition rates are as follows for both metals to ensure proper adhesion and uniformity of the deposited metals: 0.2 Å/s up to 20 nm thickness, 0.5 Å/s up to 50 nm thickness, 1.0 Å/s up to 100 nm thickness, 1.5 Å/s above 100 nm thickness. After deposition, a lift-off process is performed using a PR-stripper (MICROPOSIT Remover 1165) heated to 80 ºC. A pipette to “spray” the samples is used to assist in the lift-off process. Subsequently, DI rinse for 2 min is performed before profilometry (DEKTAK 3) to measure metal thickness and inspection via microscope.

The second major step is the diode (mesa) isolation process. The samples are dehydrated at 110 ºC for 5 min after the previous step. A pre-coating of HMDS is spun on the samples at 3000 RPM for 30s following a positive photoresist (SPR-3.0) spun on

the samples at 3000 RPM for 30s with subsequent “edge-bead” removal. The samples are “soft” baked at 110 ºC for 90s and then exposed for 12 s with an output power and wavelength of 3.5 mW/cm^2 and 365 nm, respectively, using the “Trench” layer on the photomask with the Karl Suess MJB3 mask aligner. Circular patterns larger (170, 270, 370, and 470 μm diameter) than the *p*-metal patterns constitute the mesa footprint. The samples are subsequently developed (AZ300MIF) for 60s and rinsed in flowing DI for 2 min. The samples are then mounted onto a sapphire carrier wafer (no adhesion) and loaded into a PlasmaTherm Shuttlelock ICP etching tool. Carrier gases (Cl2/Ar/BCl3) are flowed (20/5/10 sccm) at a pressure of 5 mTorr with radio frequency (RF) power of 25 W and ICP power of 130 W. Calibration of the ICP etch rate and additional analysis are presented in the “ICP etching” subsection in this appendix. The samples are etched for ~ 600nm. After etching, the remaining PR is removed, PR-stripper (MICROPOSIT Remover 1165) is heated to 80 ºC, and then subsequently rinsed in DI for 2 min. The etched deep is then verified with depth profilometry (DEKTAK 3) and inspected via microscope.

The last step of the vertical *p*-*n* diode is the backside *n*-contact deposition. Samples are dehydrated at 110 ºC for 5 min before a protective photoresist (AZ P4330) is spun on the topside of the samples at 3000 RPM for 30 s. The samples are then baked at 110 ºC for 5 min to ensure a proper “hardening” of the photoresist. An acid dip of buffered oxide etch (HCL/DI 1:3) is performed on the samples for 1 min, followed by a 2 min DI rinse in order to remove any oxides, since the *n*-metal stacks whill adhere to the GaN substrate. This acid dip procedure is performed immediately before loading the samples into an e-beam deposition chamber. The e-beam deposition chamber is brought

down to a base pressure of 2.0×10^{-6}torr before deposition. The n-metal stack (Ti/Al/Ni/Au) is subsequently deposited with a thickness of 20 nm, 100 nm, 50 nm, and 300nm, respectively. The deposition rates are as follows for both metals to ensure proper adhesion and uniformity of the deposited metals: 0.2 Å/s up to 20 nm thickness, 0.5 Å/s up to 50 nm thickness, 1.0 Å/s up to 100 nm thickness, 1.5 Å/s above 100 nm thickness. After deposition, the protective PR is removed using PR-stripper (MICROPOSIT Remover 1165) and heated to 80 ºC with a subsequent DI rinse for 2 min. Samples are inspected afterward in a microscope.

Table B.3: Process flow for fabrication of vertical p-n diodes

A. LABEL WAFERS			
1	Label Samples	Bench	
B. INDIUM REMOVAL / SURFACE CLEAN			
1	Acid Dip (3x)	Acid Bench	15 min, Aqua Regia: HNO_3:HCl 1:3 (80 ºC)
2	DI Rinse (3X)	Acid Bench	
3	Inspection	Microscope	
4	ACE clean	Solvent Bench	3 min soak
5	ISO clean	Solvent Bench	3 min soak
6	DI Rinse (3X)	Solvent Bench	3 min rinse
C. PHOTO (MASK LAYER = P-contact)			
1	Dehydration Bake	Hot Plate	110C, 5 min
2	Spin AZnLOF2020	Spinner Bench	3000rpm, 30 sec
3	Remove Edge Bead	Blade or Razor	
4	Soft Bake	Hot Plate	110C, 90 sec
5	Exposure	Stepper	7 seconds (3.5 mW/cm^2 at 365 nm)
6	Post Bake	Hot Plate	110C, 60 sec
7	Develop	Developer Bench	AZ300MIF, 80 sec
8	DI Rinse	Developer Bench	2 min, flowing
9	Inspection	Microscope	
D. p-metal Deposition			
1	Acid Dip	Acid Bench	1 min dip into BOE (1:6), 3 min DI rinse and dry
2	p-metal Deposition	Metal Evap 1	Pd/Au (20 nm, 300 nm)
3	Lift-Off	Solvent Bench	1165 stripper @ 80C 10min, use pipet to spray
4	DI Rinse	Developer Bench	2 min, flowing
5	Inspection	Microscope	
6	Profilometry	Dektak	ensure proper metal thickness
E. PHOTO (MASK LAYER = TRENCH)			
1	Dehydration Bake	Hot Plate	110C, 5 min
2	Spin HMDS	Spinner Bench	3000rpm, 30 sec
3	Spin SPR 220-3.0	Spinner Bench	3000rpm, 30 sec
4	Soft Bake	Hot Plate	110C, 90 sec
5	Exposure	MJB3	12 seconds (3.5 mW/cm^2 at 365 nm)
6	Develop	Developer Bench	AZ300MIF, 60 sec
7	DI Rinse	Developer Bench	2 min, flowing

8	Inspection	Microscope	
9	Sample mount	ICP	Sapphire Carrier (no adhesion)
10	ICP Etch	ICP	Cl2: 20sccm, Ar: 5sccm, BCL_3: 10 sccm Pressure: 5mTorr, RF power: 25W, ICP power: 130 W, Time from calibration
13	PR Removal	Solvent Bench	1165 stripper @ 80C 10min, use pipet to spray
14	DI Rinse	Developer Bench	2 min, flowing
15	Inspection	Microscope	
16	Profilometry	Dektak	Dektak across the pattern and check mesa etching depth
K. n-metal Backside Deposition			
1	Dehydration Bake	Hot Plate	110C, 5 min
2	Spin 4330 PR	Spinner Bench	3000rpm, 30 sec, Recipe 0
3	Soft Bake	Hot Plate	90C, 90 sec
4	Acid Dip	Acid Bench	1 min dip into HCL:DI (1:3), 3 min DI rinse and dry
5	n-metal Deposition	Metal Evap 1	Ti/Al/Ni/Au (20/100/50/300nm)
6	Lift-Off	Solvent Bench	1165 stripper @ 80C 10min, use pipet to spray
7	DI Rinse	Developer Bench	2 min, flowing
8	Inspection	Microscope	

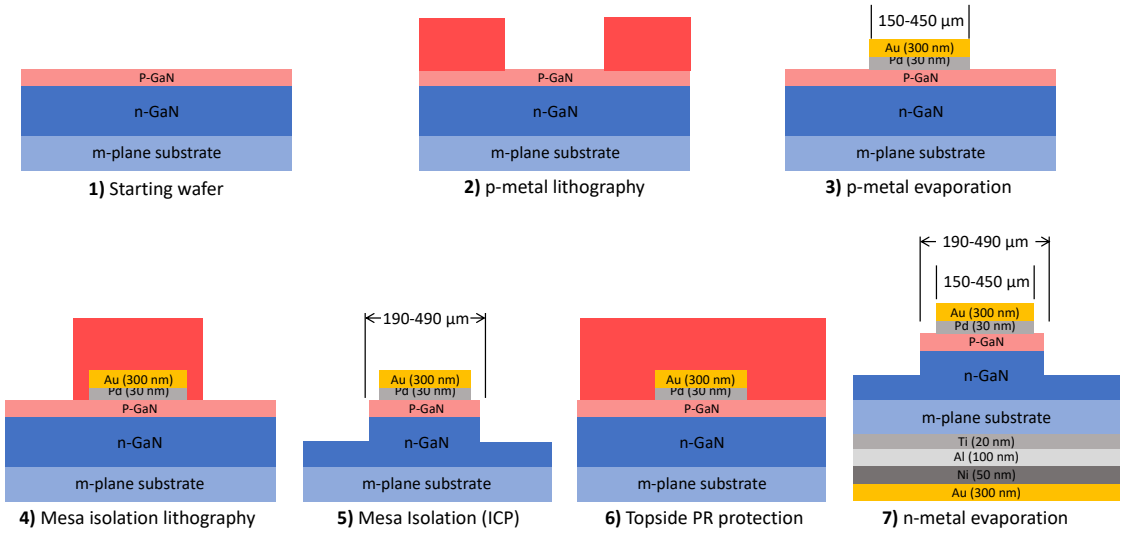

Figure B.2: photolithographic process flow of vertical m-plane p-n diode

B.2.2 Vertical Schottky diodes

The procedure for varication of the vertical Schottky diodes is detailed in Table B.4 with a photolithographic process flow in Figure B.3. After the *Schottky* didoes are epitaxially grown by MOCVD they are labeled with a diamond scribed before a 3X clean

consisting of Agua-Regia (HCl: HNO_3) in a 3:1concentration at 80ºC for 15 min and solvent cleaned as previously detailed in the vertical *p-n* diode section.

The first major step is the Schottky-contact deposition. Thus, a negative photoresist (AZnLOF2020) is spun on the samples at 3000 RPM for 30s followed by "edge bead" removal. The samples are then "soft" baked at 110 ºC for 90s. Using a Karl Suess MJB3 mask aligner, the samples are then aligned to the "p-contact" layer on the photomask which consists of circular patterns (150, 250, 350, and 450 μm). The samples are exposed for 7s with an output power and wavelength of 3.5 mW/cm2 at 365 nm, respectively. A post bake is performed at 110 ºC for 60s to ensure proper viscosity of the resist for development. The samples are subsequently developed in a base solution (AZ300MIF) 80 s and rinsed in flowing DI for 2 min. An acid dip of buffered oxide etch (BOE 6:1) is performed on the samples for 1 min followed by a 2 min DI rinse in order to remove any oxides since the *p*-metal stacks will adhere to the GaN surface. This acid dip procedure is performed immediately before loading the samples into an e-beam deposition chamber. The e-beam deposition chamber is brought down to a base pressure of 2.0×10^{-6}torr before deposition. The semi-transparent Schottky-metal (Ni) is subsequently deposited with a thickness of 9nm . The deposition rate is 0.2 Å/s. After deposition, a lift-off process is performed using a PR-stripper (MICROPOSIT Remover 1165) heated to 80 ºC. A pipette is used to "spray" the samples in order to assist in the lift-off process. A subsequent DI rinse for 2 min is performed before profilometry (DEKTAK 3) to measure metal thickness and inspection via microscope.

The second and last step of the vertical Schottky diode is the backside *n*-contact deposition. The process is the same as the last step in the vertical p-n diode process flow and can be seen in that subsection.

Table B.4: Process flow for fabrication of vertical Schottky diodes

A. LABEL WAFERS			
1	Label Samples	Bench	
B. INDIUM REMOVAL / SURFACE CLEAN			
1	Acid Dip (3x)	Acid Bench	15 min, Aqua Regia: HNO_3:HCl 1:3 (80 ºC)
2	DI Rinse (3X)	Acid Bench	
3	Inspection	Microscope	
4	ACE clean	Solvent Bench	3 min soak
5	ISO clean	Solvent Bench	3 min soak
6	DI Rinse (3X)	Solvent Bench	3 min rinse
C. PHOTO (MASK LAYER = P-contact)			
1	Dehydration Bake	Hot Plate	110C, 5 min
2	Spin AZnLOF2020	Spinner Bench	3000rpm, 30 sec
3	Remove Edge Bead	Blade or Razor	
4	Soft Bake	Hot Plate	110C, 90 sec
5	Exposure	Stepper	7 seconds (3.5 mW/cm^2 at 365 nm)
6	Post Bake	Hot Plate	110C, 60 sec
7	Develop	Developer Bench	AZ300MIF, 80 sec
8	DI Rinse	Developer Bench	2 min, flowing
9	Inspection	Microscope	
D. p-metal Deposition			
1	Acid Dip	Acid Bench	1 min dip into BOE (1:6), 3 min DI rinse and dry
2	p-metal Deposition	Metal Evap 1	Pd/Au (20 nm, 300 nm)
3	Lift-Off	Solvent Bench	1165 stripper @ 80C 10min, use pipet to spray
4	DI Rinse	Developer Bench	2 min, flowing
5	Inspection	Microscope	
6	Profilometry	Dektak	ensure proper metal thickness
E. n-metal Backside Deposition			
1	Dehydration Bake	Hot Plate	110C, 5 min
2	Spin 4330 PR	Spinner Bench	3000rpm, 30 sec, Recipe 0
3	Soft Bake	Hot Plate	90C, 90 sec
4	Acid Dip	Acid Bench	1 min dip into HCL:DI (1:3), 3 min DI rinse and dry
5	n-metal Deposition	Metal Evap 1	In (9 nm)
6	Lift-Off	Solvent Bench	1165 stripper @ 80C 10min, use pipet to spray
7	DI Rinse	Developer Bench	2 min, flowing
8	Inspection	Microscope	

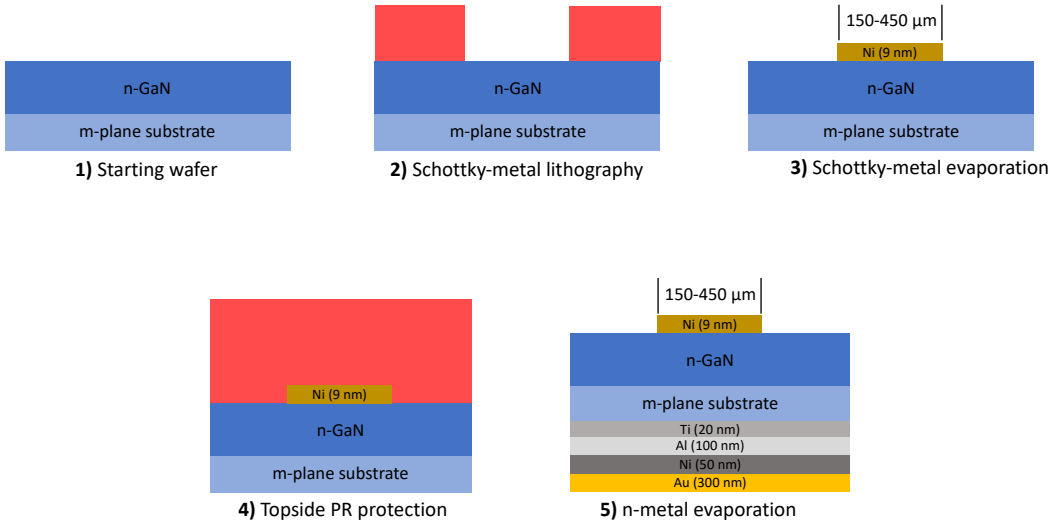

Figure B.3: photolithographic process flow of vertical m-plane p-n diode

B.2.3 Lateral p-n diodes

The procedure for the varication of lateral p-n diode is detailed in Table B.5 with a photolithographic process flow in Figure B.4. The sample labeling and cleaning processes are the same as those described in the vertical *p-n* diode section

The first and section major steps are the *p*-contact deposition and mesa isolation steps. Again, these are the same as those presented in the vertical p-n diode section. However, the ICP etch depth must be carefully performed in order to ensure an etch depth to the n^+ GaN contact layer.

The last step of the vertical *p-n* diode is the topside *n*-contact deposition. Samples are dehydrated at 110 ºC before a negative photoresist (AZnLOF2025) is spun on the samples at 3000 RPM for 30s + "edge bead" removal. The use of this PR is needed due to the extended thickness of this n-metal (~ 7µm). The samples are then "soft" baked at 110 ºC for 90s to ensure a proper "hardening" of the photoresist before exposure. Using a Karl Suess MJB3 mask aligner, the samples are then aligned to the "N-contact" layer on

the photomask which consists of annulus patterns (inside diameter: 190, 290, 390, and 490 µm / outside diameter: 290, 390, 490, and 590 µm). The samples are exposed for 6s with an output power and wavelength 3.5 mW/cm2 at 365nm, respectively. A post bake is performed at 110 ºC for 60s to ensure proper viscosity of the resist for development. The samples are subsequently developed in a base solution (AZ300MIF) 80s and rinsed in flowing DI for 2 min. An acid dip of buffered oxide etch (HCL/DI 1:3) is performed on the samples for 1 min followed by a 2 min DI rinse in order to remove any oxides since the *n*-metal stacks will adhere to the GaN surface. This acid dip procedure is performed immediate before loading the samples into an e-beam deposition chamber. The e-beam deposition chamber is brought down to a base pressure of 2.0×10^{-6}torr before deposition. The *n*-metal stack (Ti/Al/Ni/Au) are subsequently deposited with a thickness of 20 nm, 100 nm, 50nm, and 300nm, respectively. The deposition rates are as follows for both metals to ensure proper adhesion and uniformity of the deposited metals: 0.2 Å/s up to 20 nm thickness, 0.5 Å/s up to 50 nm thickness, 1.0 Å/s up to 100 nm thickness, 1.5 Å/s above 100 nm thickness. After deposition, the protective PR is removed using PR-stripper (MICROPOSIT Remover 1165) heated to 80 ºC with a subsequent DI rinse for 2 min. Samples are inspected afterward in a microscope.

Table B.5: Process flow for fabrication of vertical p-n diodes

A. LABEL WAFERS			
1	Label Samples	Bench	
B. INDIUM REMOVAL / SURFACE CLEAN			
1	Acid Dip (3x)	Acid Bench	15 min, Aqua Regia: HNO_3:HCl 1:3 (80 ºC)
2	DI Rinse (3X)	Acid Bench	
3	Inspection	Microscope	
4	ACE clean	Solvent Bench	3 min soak
5	ISO clean	Solvent Bench	3 min soak
6	DI Rinse (3X)	Solvent Bench	3 min rinse
C. PHOTO (MASK LAYER = P-contact)			
1	Dehydration Bake	Hot Plate	110C, 5 min
2	Spin AZnLOF2020	Spinner Bench	3000rpm, 30 sec
3	Remove Edge Bead	Blade or Razor	
4	Soft Bake	Hot Plate	110C, 90 sec

5	Exposure	Stepper	7 seconds (3.5 mW/cm^2 at 365 nm)
6	Post Bake	Hot Plate	110C, 60 sec
7	Develop	Developer Bench	AZ300MIF, 80 sec
8	DI Rinse	Developer Bench	2 min, flowing
9	Inspection	Microscope	
D. p-metal Deposition			
1	Acid Dip	Acid Bench	1 min dip into BOE (1:6), 3 min DI rinse and dry
2	p-metal Deposition	Metal Evap 1	Pd/Au (20 nm, 300 nm)
3	Lift-Off	Solvent Bench	1165 stripper @ 80C 10min, use pipet to spray
4	DI Rinse	Developer Bench	2 min, flowing
5	Inspection	Microscope	
6	Profilometry	Dektak	ensure proper metal thickness
E. PHOTO (MASK LAYER = TRENCH)			
1	Dehydration Bake	Hot Plate	110C, 5 min
2	Spin HMDS	Spinner Bench	3000rpm, 30 sec
3	Spin SPR 220-3.0	Spinner Bench	3000rpm, 30 sec
4	Soft Bake	Hot Plate	110C, 90 sec
5	Exposure	MJB3	12 seconds (3.5 mW/cm^2 at 365 nm)
6	Develop	Developer Bench	AZ300MIF, 60 sec
7	DI Rinse	Developer Bench	2 min, flowing
8	Inspection	Microscope	
9	Sample mount	ICP	Sapphire Carrier (no adhesion)
10	ICP Etch	ICP	Cl2: 20sccm, Ar: 5sccm, BCL_3: 10 sccm Pressure: 5mTorr, RF power: 25W, ICP power: 130 W, Time from calibration
13	PR Removal	Solvent Bench	1165 stripper @ 80C 10min, use pipet to spray
14	DI Rinse	Developer Bench	2 min, flowing
15	Inspection	Microscope	
16	Profilometry	Dektak	Dektak across the pattern and check mesa etching depth
C. PHOTO (MASK LAYER = N-contact)			
1	Dehydration Bake	Hot Plate	110C, 5 min
2	Spin AZnLOF2035	Spinner Bench	3000rpm, 30 sec
3	Remove Edge Bead	Blade or Razor	
4	Soft Bake	Hot Plate	110C, 90 sec
5	Exposure	Stepper	5 seconds (3.5 mW/cm^2 at 365 nm)
6	Post Bake	Hot Plate	110C, 60 sec
7	Develop	Developer Bench	AZ300MIF, 80 sec
8	DI Rinse	Developer Bench	2 min, flowing
9	Inspection	Microscope	
K. n-metal Backside Deposition			
1	Dehydration Bake	Hot Plate	110C, 5 min
2	Spin 4330 PR	Spinner Bench	3000rpm, 30 sec, Recipe 0
3	Soft Bake	Hot Plate	90C, 90 sec
4	Acid Dip	Acid Bench	1 min dip into HCL:DI (1:3), 3 min DI rinse and dry
5	n-metal Deposition	Metal Evap 1	Ti/Al/Ni/Au (20/100/50/300nm)
6	Lift-Off	Solvent Bench	1165 stripper @ 80C 10min, use pipet to spray
7	DI Rinse	Developer Bench	2 min, flowing
8	Inspection	Microscope	

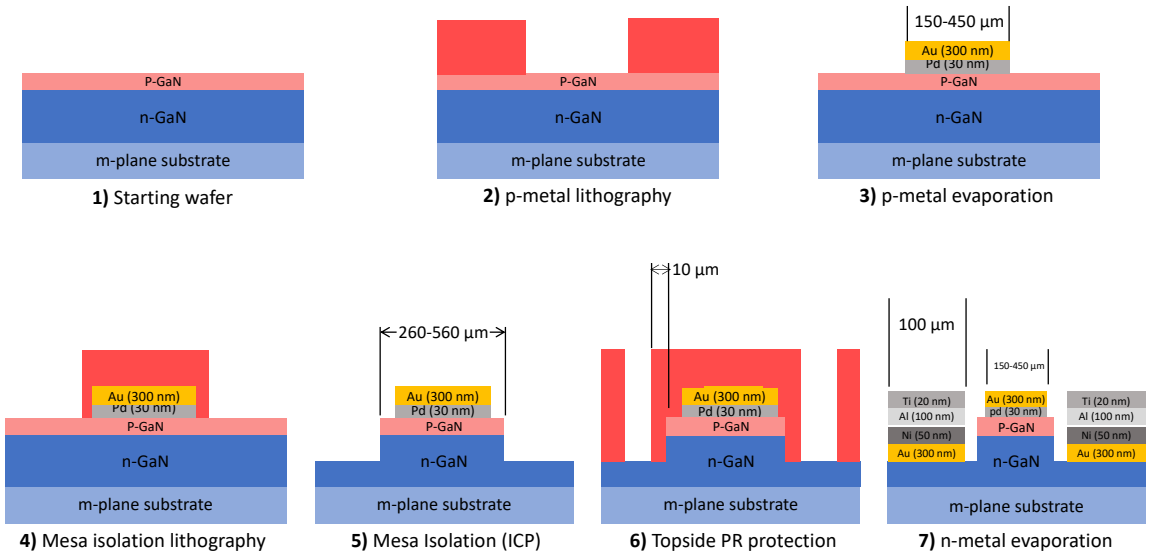

Figure B.4: photolithographic process flow of vertical m-plane p-n diode

B.3 Inductively Coupled Plasma (ICP) etching of GaN

Dry-etching has been used in this body of work for implementation of dry-etched surfaces on *m*-plane GaN for regrowth, and for use in device isolation by forming mesas during fabrication of *p-n* diodes. Inductively Coupled Plasma (ICP) refers to a system configuration where plasma is generated by means of inductively coupling RF power in the source while independently controlling the ion energy bombarding the substrate via the applied bias power. In this subsection, some background information surrounding ICP etching will be discussed along with calibrations for ICP etching of GaN.

B.3.1 Overview

The formation of plasmas though ionization of atoms via RF induced electromagnetic fields has enabled the etching of semiconductor materials (Si, GaN, GaAs, etc.) for many decades due to its low consumption of chemicals, low

environmental impact, cleanliness (vacuum-environment), repeatability, and compatibility with automation. Three categories of glow discharge (plasma) methods can be utilized for etching semiconductors: 1) plasma etching via reactive gas plasma with low energy ions, 2) reactive ion etching via reactive gas plasma with high energy ions, and 3) glow discharge sputter etching via inert gas plasma with high energy ions.

We may now investigate the basic principle of etching considering plasma etching via reactive gas plasma with low energy. Thus, Molecular gas is required to establish a glow discharge and create reactive species. For example, a reactive species of Cl is generated through dissociation ionization as represented in equation B.1 [3]:

$$\mathrm{Cl_2} + \mathrm{e^-} \rightarrow 2\mathrm{Cl} + \mathrm{e^-} \qquad (B.1)$$

Thus, the reactive species of Cl may react with GaN such that etching may result as seen via equations B.2-4:

$$\mathrm{GaN} + 2\mathrm{Cl} \rightarrow \mathrm{GaCl} + \mathrm{NCl} \qquad (B.2)$$

$$\mathrm{GaCl} + \mathrm{Cl} \rightarrow \mathrm{Ga}Cl_2 \qquad (B.3.a)$$

$$\mathrm{NCl} + \mathrm{Cl} \rightarrow \mathrm{NCl_3} \qquad (B.3.b)$$

$$\mathrm{Ga}Cl_2 + \mathrm{Cl} \rightarrow \mathrm{Ga}Cl_3 \qquad (B.4.a)$$

$$\mathrm{NCl_3} + \mathrm{Cl} \rightarrow \mathrm{N}Cl_3 \qquad (B.4.b)$$

The volatile products $\mathrm{Ga}Cl_3$ and $\rightarrow \mathrm{N}Cl_3$ are pumped away from the ICP chamber as the reactions continue. Chlorine is typically used over fluorine-based chemistries (CF_4, CF_6, etc.) for etching III-V semiconductors due to the lack of volatility of GaF_3. Another benefit of Chlorine based chemistries is the volatility of Gallium Chloride ($\mathrm{Ga}Cl_3$) at room temperatures. However, Cl_2 molecules do not etch GaN in the absence of energetic ion bombardment. Furthermore, many chlorine containing gases can be used to etch GaN

with the addition of Ar and BCl_3. Selectivity of etching may be tailored by the ratio of these species (Cl_2, Ar, and BCl_3). Volatile Cl atoms can etch GaN spontaneously at room temperature but with ion bombardment-induced enhancement, the etch rate can be large enough to allow reasonably anisotropic etching to be carried out without sidewall blocking in dilute Cl atom plasmas and high energy ion bombardment. Additionally, isotropic etching can be obtained using Cl-rich plasmas and low energy ions.

Sputter etching via inert gas plasma with high energy ions may also be present. This process is considered as a mechanical etching process as high energy ions have enough energy to displace atomic particle from the crystalline lattice of a semiconductor upon bombardment. The physics of this process can be quite complex without the use of computational methods to predict the scattering and impact of ions within the lattice. Nevertheless, this process can be used to achieve high selectivity and etch rate.

We may also consider the higher density ($n_e > 10^{13}$ electrons/cm^3) of plasmas that are present in inductively coupled plasmas. There are some advantages of these due to lower ion bombardment energies which improve the selectivity and reduce ion-bombardment-induced physical damage. However, lower etch rates are a consequence of this, but etch rates can be increased by using higher ion fluxes due to high density plasmas.

B.3.2 ICP chamber

The tool is comprised of two independent chambers: 1) load-lock, and 2) the etch chamber. A picture of the PlasmaTherm Apex SLR ICP is shown in if Figure B.5.b. For the purposes etching samples of *m*-plane GaN, a sapphire carrier wafer is used. The m-plane wafer (5mm x 5mm) is simply placed on-top of the sapphire carrier wafer. It may

be noted that adhesion of the sample to the carrier wafer ensures proper thermal conductive. However, no adhesion is performed due to the risk of impurity contamination of the samples as these samples are typically loaded directly into the MOCVD reactor after etching. The carrier wafer (with sample placed on top) is placed within the load-lock and pumped down to base pressure. Once base pressure is reached, an automated mechanical arm transfers the sample into the etch chamber.

The configuration of the PlasmaTherm Apex SLR ICP etch chamber is presented in figure B.5.a. The cylindrical configuration consists of inductive coils surrounding the top part of the cylindrical chamber. The cylindrical inductive coils generate plasma by a 2 MHz RF source while the substrate is biased by a 13.56 MHz RF source. Power is controlled through a capacitive matching network in order to minimized reflected RF power.

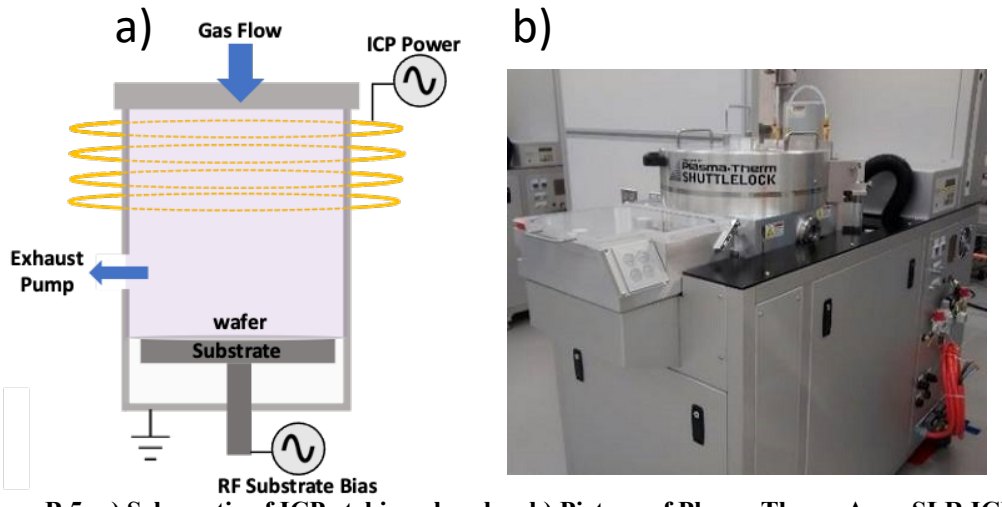

Figure B.5: a) Schematic of ICP etching chamber b) Picture of PlasmaTherm Apex SLR ICP

ICP gases for etching GaN consist of Chlorine (Cl_2), Argon (Ar), and Boron-trichloride (BCl_3). Chamber pressure and flows are controlled through mass flow controllers and a turbo vacuum pump which exhausts the gases to a scrubber.

Additionally, backside He gas is flown in order to stabilize the temperature of the carrier wafer during etching. A ceramic clamp surrounding the edge of the carrier wafer ensures that He gas does not leak into the chamber above. Once the sample is loaded into the etch chamber, the etch gases are flown at a desired pressure. ICP and RF power are turned on which strike the plasma, and etching ensues. The next subsection will give more details into the etch calibrations performed on GaN for the purposes of this work.

B.4 ICP etching calibration for GaN

A few calibration series performed on GaN for the purposes of developing consistant ICP etch recipies will be presented. These series consist of the effects of BCl_3 incorporation, ICP power, and RF power dependence on etching rates.

B.4.1 BCl_3 flow calibration

The first calibration to be presented is the addition of BCl_3 gas in addition to Cl_2 and Ar. Adding BCl_3 has been shown to stabilize the plasma DC bias by ensuring a uniform discharge glow as compared to just Cl_2 and Ar. Thus, calibration *c*-plane samples with ~ 2 um n-GaN grown on sapphire were etched with in which $Cl/Ar/BCl_3$ at a chamber pressure of 5 mTorr with an ICP power of 120W and a RF power of 30W. The ratio of $Cl/Ar/BCl_3$ was controlled by the flow rate of each gas. Cl_2 and Ar were set at 20sccm and 5sccm, respectively. The flow rate of BCl_3 was increased in subsequential etches by increasing the flow as: 0, 5, 10, 15 sccm. The etch rate (nm/min) for this series is presented in Figure B.6. It may be observed as the ratio of BCl_3 gas increases the etch

rate drops from ~115 nm/min with BCl_3 = 0sccm to ~ 85 nm/min with BCl_3 = 15sccm. This reduction in etch rate is due to an increase of non-volatile products associated with BCl_3. This trade off with increasing BCl_3 incorporation into the plasma may be compensated by increase of either the ICP or RF power in order to increase the etch rate. However, ~ 85 nm/min is a reasonable etch rate as the deepest etch deeps are no more than 1500nm.

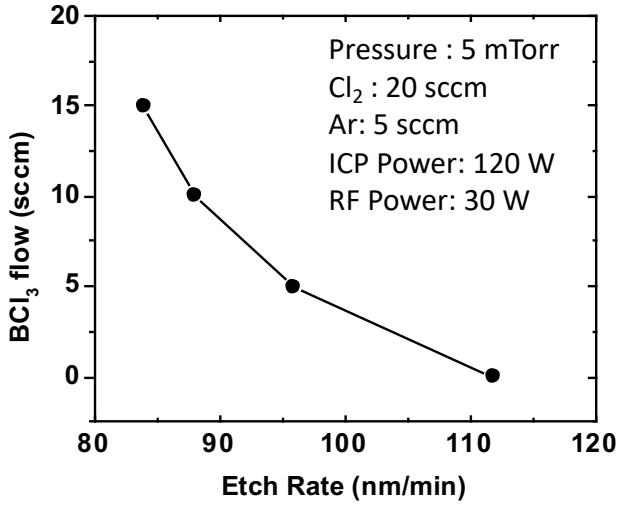

Figure B.6: ICP etch rate calibration with increasing BCL_3 flow

B.4.2 ICP power calibration

The second calibration to be presented is influence of ICP power on the etch rate of GaN. Thus, calibration *c*-plane samples with ~ 2 um *n*-GaN grown on sapphire were etched with $Cl/Ar/BCl_3$ at a chamber pressure of 5 mTorr. Cl_2, Ar, and BCl_3 flows were set at 20sccm,5sccm, and 10sccm respectively. RF power was set to 30W with and increasing ICP power: 60, 80, 100, 120 W. The etch rate (nm/min) for this series is presented in Figure B.7. As the ICP power is increased, the etch rate increases from ~20 nm/min with ICP power = 60 W to ~ 115 nm/min with ICP power = 120 W. This

increase in etch rate is due to an increase of the plasma density due to increasing ICP power coupled to the plasma.

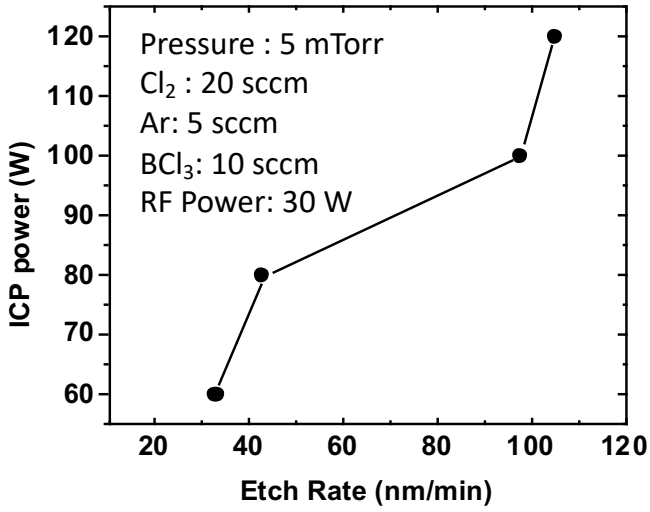

Figure B.7: ICP etch rate calibration with increasing ICP power

It may be noted that the plasma is also very unstable with ICP power less than 100 W. The plasma begins to flicker as there is the induced energy of the ICP source competes with the plasma discharge and the DC bias becomes unstable. Therefore, ICP power for this system with these gas flows is chosen to be above 100 W. Additionally, an increase in RF power while holding all other parameters constant is a reasonable calibration. However, the DC bias becomes relatively large above 30W. As the RF source is responsible for the ion bombardment of ionized species, it was chosen to calibrate this to the minimum value which was found to be ~15 W with DC bias < 20 V. However, delicate ramps of the RF power are required to reach these minimum values. Thus, RF power of ~ 35W which yields a corresponding DC bias ~ 1.5 V was selected for its repeatability.

B.4.3 DC bias calibration

The last calibration will look at the dependence of DC bias on the yellow band emission of GaN. The yellow band emission is due to a radiative transition from a shallow donor to a deep level acceptor with the bandgap of GaN [4]. The states producing the levels responsible for the YL and donner-acceptor emissions, arise from complexes of extended defects and native-point defects or impurities such as carbon [5]. Thus, if an increase in damage induce defects levels are present within the band gap, the yellow band emission will increase. By observing the ratio of the yellow band emission and band-edge emission of etched GaN we may observe the dependence of DC bias on these deep level concentrations. Therefore, calibration *c*-plane samples with ~ 2 um n-GaN grown on sapphire were etched with Cl/Ar/BCl_3 at a chamber pressure of 5 mTorr. Cl_2, Ar, and BCl_3 flows were set at 20sccm, 5sccm, and 10sccm respectively. RF power was set to 35W with and increasing ICP power: 200, 300, 400, 500, 600, and 700 W. Photoluminescence of the samples was conducted using a 355nm laser to pump the band edge (BE) and yellow bands (YB), and is presented in Figure B.8.a . The associated DC bias and BE/YB ratios of this calibration series is presented in Figure B.8.b.

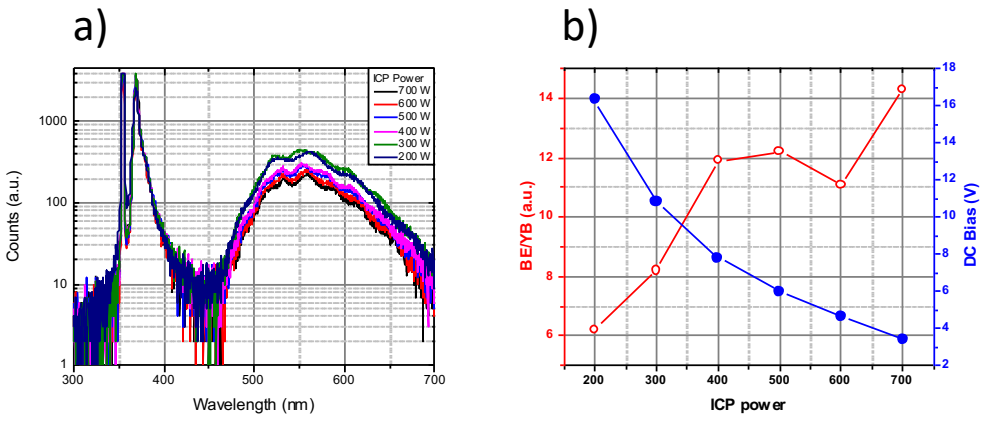

Figure B.8: a) Photoluminescence of samples with increasing ICP power b) plot of band-edge/yellow-band ratio and associated DC bias of increasing ICP power on etched calibration samples

From figure B.8.b we can observe the DC bias decreasing with increasing ICP power from ~ 16V at ICP = 200 W to ~ 3V at ICP = 700W. This is due to the increasing sheath that is generated at the plasma interface with the substrate with increasing plasma densities attributed to the larger ICP powers. Interestingly, we can see the BE/YB ratio increasing with reducing DC bias. Thus, it is expected that decreasing DC bias produces less etch-enhanced damage within the band gap of GaN. Therefore, it may be a rule of practice to ensure the lowest possible DC bias while ensuring proper etch rates when using ICP for dry-etching GaN.

B.5 Photoelectrochemical Etching (PEC)

Wet-etching via photoelectrical etching (PEC) has been used in this body of work for the removal of dry-etched surface damage on *m*-plane GaN prior to regrowth. In this subsection, some background information surrounding PEC etching will be discussed along with calibrations for PEC etching of *m*-plane GaN.

B.5.1 Overview

In the pursuit to mitigate dry-etch enhanced damage, an alternative process was required that was able to etch significant amounts of GaN while not inducing additional defects into the material. Thus, PEC etching was selected since it enables significant etching into GaN [6]–[9] while maintaining low defectivity compared to dry-etching via reactive ions or ion bombardment generated through plasmas. Therefore, the basic physics of PEC etching will be presented. PEC etching is primarily driven by the chemical reactions presented in equations B.5-7:

$$\mathrm{GaN} + \mathrm{photon} \rightarrow \mathrm{GaN} + e^- + h^+ \quad (B.5)$$

$$\mathrm{GaN} + 3h^+ \rightarrow \mathrm{Ga}^{3+} + \frac{1}{2}N_2 \quad (B.6)$$

$$2\mathrm{Ga}^{3+} + 6OH^- \rightarrow Ga_2O_3 + 3H_2O \quad (B.7)$$

In the above equations above, samples of GaN are emersed in an electrolyte solution. Potassium hydroxide (KOH) is selected for the purposes of this work since KOH is dissolved in water via equation B.8:

$$\mathrm{KOH} + H_2O \rightarrow K^+ + OH^- \quad (B.8)$$

Electron-hole pairs are generated via illumination of light as the sample of GaN is continually emersed in the electrolyte (equation B.5). Electrons and holes begin to accumulate at the semiconductor/electrolyte interface of the samples as they diffuse towards the regions where the band profiles bend. Bandbending of n-type GaN typically bends the band profile upwards [10]. Therefore, holes will accumulate more easily at the surface. Ohmic metals may be deposited on the surface to assist in the accumulation of electrons beneath the metal which also increases the accumulation of holes away from the metal due to lower recombination. Oxide formation begins to occur due to the presence of holes at the semiconductor/electrolyte interface (equation B.6 and 7). As oxide is generated it is also subsequently dissolved by the electrolyte solution. Etching through this mechanism proceeds as long as the solution is kept consistent. A schematic representation of PEC etching is presented in figure B.9.

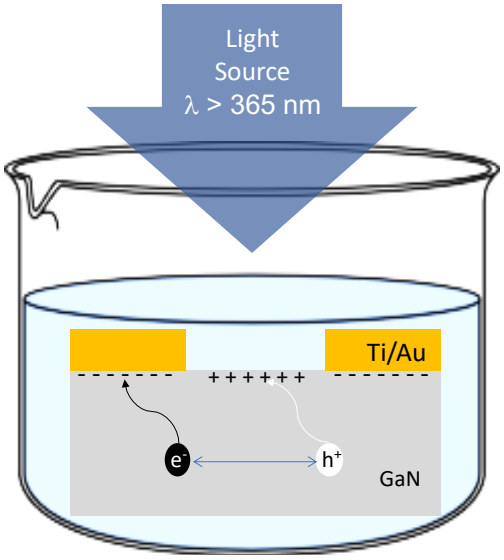

Figure B.9: Schematic of PEC etching process showing GaN submersed in electrolyte with generated electron-hole pairs via illumination.

B.5.2 PEC etching apparatus

The PEC etching apparatus used for etching is presented in figure B.10.a. The samples are placed on a specially designed Teflon holder within a glass beaker to allow the resulting N_2 gas to properly vent to the surface of the electrolyte solution. The beaker is placed on top of a hot plate and stirred in order to control the temperature of the solution and ensure proper consistency. The illumination source is chosen so that the wavelength of illumination is $\lambda < 365$nm. Illumination can be implemented by several methods: 1) Mercury arc lamp 2) LED array, or 3) laser diode. For the purposes of this work, the Mercury arc lamp is chosen due to its high intensity. The use of a focusing lens concentrates the isotropic source to further increase intensity. The power density v spatial distance at the sample location is presented in Figure B.10.b at $\lambda = 365$nm and $\lambda = 405$nm.

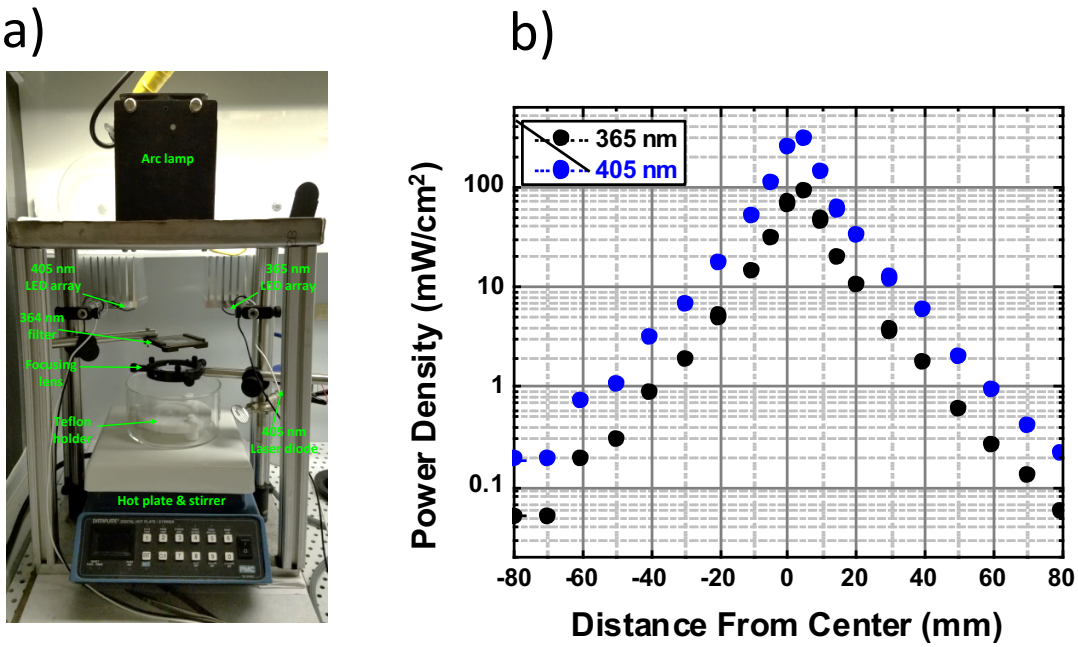

Figure B.10: a) PEC etching apparatus b) power density v distance for Hg arc lamp

B.5.3 PEC etching calibrations

Calibrations of PEC etching on *n*-type m-plane were conducted in order to determine etch rate and surface morphology roughness. Thus, PEC etching was conducted on n-GaN (6×10^{16} cm^{-3}) grown on *m*-plane free standing substrates using 0.01M KOH in de-ionized (DI) water at room temperature. A surface flux of 100 mW/cm^2 is used. Samples were etched for varying times on continuously grown *m*-plane GaN and also ICP etched (400 nm) *m*-plane GaN in order to differentiate the etch rate on the two types of surfaces. Mesa structures were fabricated using sputtered silicon nitride (Si_3N_4) deposited pads in order to conduct profilometry to determine etch rate. Since the dielectric Si_3N_4 is non-conductive, there is no enhancement of etching due to the accumulation of electrons beneath it leading to lower recombination of holes. Therefore,

the etch-depth v. time for the *m*-plane PEC and ICP+PEC etched calibration samples are presented in Figure B.11.a.

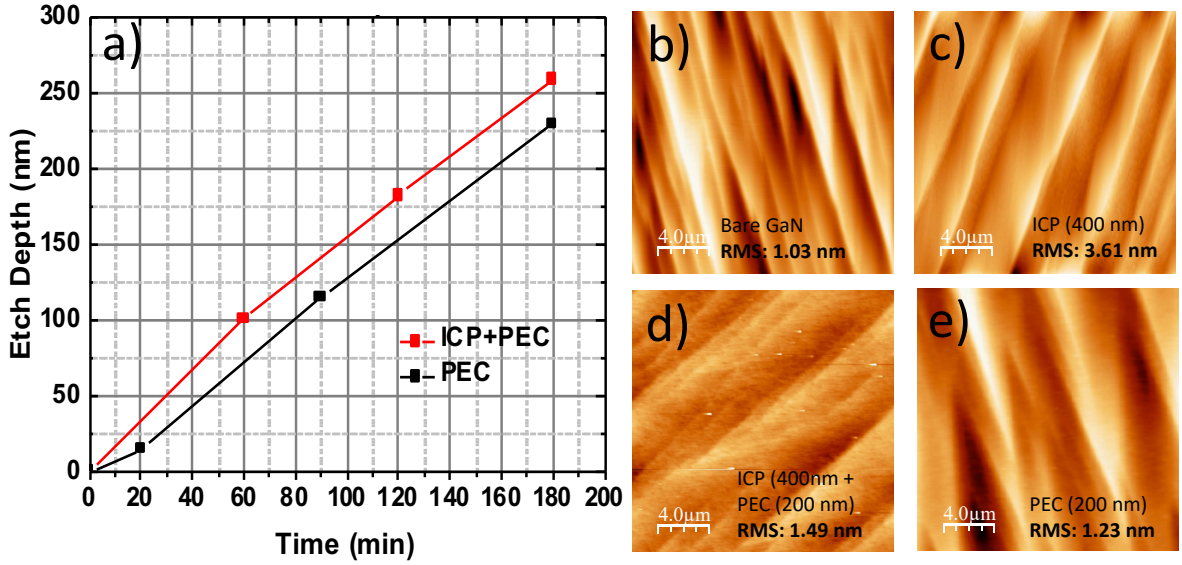

Figure B.11: a) PEC and ICP (400nm) + PEC etching calibration, AFMs of b) bare m-plane sample c) ICP etched (400 nm) sample, d) ICP etched (400 nm) + PEC etched (200 nm) sample, e) PEC etched (200 nm) sample

It may be observed that ICP+PEC calibration sample shows a faster etch rate (~1.5 nm/min) for short etching times (~ 20 min) than the PEC etched-only sample (~0.7 nm/min). However, the rate at longer etching time (> 30 min) is ~ 1.2 nm for both ICP+PEC and PEC etched m-plane samples. AFM images of a bare (unetched m-plane sample), ICP etched sample, ICP (400 nm) + PEC (200 nm) etched sample, and PEC etched sample are shown in figure B.11b-e. The bare sample shows the lowest RMS roughness at ~ 1.03 nm of all samples. ICP (400 nm) etching further roughens the surface with a RMS roughness of ~ 3.61 nm. Subsequent PEC etching (200 nm) on an ICP etched (400 nm) surface reduces the RMS roughness to ~ 1.49 nm. Thus we can see that PEC etching can effectively smoothen ICP etched-enhanced roughness. PEC etching (200 nm)

only slightly roughens the surface as compared to unetched surface to ~ 1.23 nm. Thus, we have shown etch rate calibrations and the roughness of PEC etched surfaces as compared to unetched surfaces and ICP etched surfaces.

B.6 References

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Appendix C: Characterization Methods

This appendix provides additional information on the characterization methods utilized in this dissertation. These methods include current-voltage J-V measurement, Secondary Ion Mass spectroscopy (SIMS), Deep-Level Optical Spectroscopy (DLOS), Atomic Force Microscopy (AFM), and Radio Frequency (RF) impedance measurements.

C.1 Electrical (*J-V*) Characterization

A review of the methods used to characterize the electrical current-density voltage (J-V) measurements of the diodes in this study is presented below. Two experimental setups were utilized to conduct J-V measurements for low-voltage and high-voltage testing, respectively. Details of the experiment setups are presented below.

C.1.1 Low voltage testing

Low-voltage testing is conducted via an automated source-meter connected to a probing station which enables contact to the anode and cathode of the devices under test. The source meter consists of a Kiethley 2400 utilized as a voltage source while simultaneously measuring the current. The maximum voltage and current measurable for this source is ± 20 V and 5 A, respectively. Also, the minimum measurable current is 50 pA. The current compliance is automatically scaled to ensure proper resolution throughout the device testing range. The probing station consist of two or four Signatone micro-manipulator with Tungsten/Gold-plated probe tips (25 μm diameter) for contacting

the device terminals in either 2-probe or 4-probe configuration. Automation is enabled via a software (MATLAB) controlled program to set the voltage limits, voltage increment steps, and over-current limits.

C.1.2 High voltage testing

High-voltage testing is also conducted via an automated source meter connected to a probing station which enables contact to the anode and cathode of the devices under test. The source meter consists of a Kiethley 2600 high-voltage source while also simultaneously measuring the current. The maximum voltage and current measurable for this source is ± 3000 V and 120 mA respectively. Also, the minimum measurable current is 1 fA. Device probing is performed via micro-manipulator with probe tips for contacting the device terminals. Probing of back-side contact devices is enabled through the use of a conductive substrate that makes contact with the back-side contact and enables probing from above. Automation is also enabled via a software (MATLAB) controlled program to set the voltage limits, voltage increment steps, and over-current limits.

C.2 Secondary Ion Mass spectroscopy

Secondary ion mass spectroscopy (SIMS) is a method used to detect atomic elements within semiconductor materials. Low concentration of dopants and impurities are also detectable. Depth profiles on elemental dopants and impurities can be measured over several micrometers with resolutions as low as a few angstroms. The driving principle of SIMS is a sputtered/etching process enabled via an ion beam of either O_2^+ or Cs^+ which produced secondary ions. These secondary ions are extracted and analyzed via mass spectroscopy in order to determine the elemental species and concentration. SIMS

measurements in this body of work were conducted by EAG laboratories in order to determine the impurity concentration of Si, O, and C within epitaxially MOCVD grown *m*-plane GaN. Specifically, impurity concentrations at interfaces within p-n diodes were analyzed via this method. The detection limits (sensitivity) and depth resolution are the same as previously stated at: $Si = 3\times 10^{15}\text{cm}^{-3}$, $O = 1\times 10^{16}\text{cm}^{-3}$, $C = 5\times 10^{15}\text{cm}^{-3}$and 12.5 Å, respectively. Therefore, a comprehensive analysis of these pertinent impurities within the devices presented in the work is enabled.

C.3 Steady-state photocapacitance and lighted capacitance voltage

The review and analysis of deep level optical spectroscopy considering capacitance transients, photoluminescence, deep state dependence on depletion capacitance, deep level optical spectroscopy, steady-state photocapacitance, and Lighted capacitance-voltage measurements is presented in this section. All information in this section is referenced from [1].

C.3.1 Capacitance transients

Transients in capacitance may result either by thermally or optically stimulated transitions of carriers (electrons/holes) into or out of deep levels located in the depletion region of a semiconductor. For our purposes, only optically stimulated transitions will be considered for *n*-type majority carrier (electron) Schottky diodes. These methods may also be implemented on minority carrier devices such as *p*-*n* junctions as well. Thus, considering majority carrier Schottky diodes, electrons within deep levels in the depletion region may be emitted into the conduction band by the depletion region built-in electric field. A net increase in charge in the depletion region results by a compensation of free

carriers. Therefore, the reduction in the depletion width is measured as an increase in depletion capacitance.

Capacitance-voltage (*C-V*) measurements are used to determine the free carrier concentration ($N_d^+ - N_a^-$) in Schottky diodes. The depth of the depletion region is controlled by the applied reverse bias V_r to move the depletion edge x_d. The change in the space-charge can be measured by the change in the depletion capacitance as a function of the applied reverse bias. Therefore, the spatially dependent carrier concentration can be determined as [2]:

$$n(x) = \frac{-C^3}{q\varepsilon_s A}\left(\frac{dC}{dV_r}\right)^{-1} \tag{C.1}$$

The constant q is the elementary charge, ε_s semiconductor dielectric constant, A is the diode area and C is the measured capacitance. The depletion edge x_d may also be expressed as [2]:

$$x_d = \frac{\varepsilon_s A}{C} \tag{C.2}$$

C.3.2 Photoluminescence (PL)

Photoluminescence (PL) is a technique that allows shallow and deep levels within wide-gap materials to be identified through radiative capture and recombination. Typically, a light source with energy exceeding the bandgap of the semiconductor is used to create optically generated electron-hole pairs within the semiconductor. These free carriers can thus participate in several types of optical transitions, including band-to-band

recombination, free and bound excitonic transitions, as well as band-to-deep state (radiative capture) and donor-acceptor pair (DAP) transitions. Radiative capture can occur through interaction of a free electron and an ionized donor-like deep state or a free hole and a neutral acceptor-like deep state. However, the spectrum obtained from the resulted photoluminescence of free carries may not be used to identify optical deep level transitions, since phonon-coupling effects can produce a nearly continuous range of optical transition energies between a free carrier and a given deep level [3]. Additionally, it is not clear from PL with which band the deep level interacts. Therefore, identification of deep level concentrations is very difficult to obtain from PL measurements.

C.3.3 Deep state dependence on depletion capacitance

The space-charge region may be influenced by ionized deep level defects that can trap either electrons or holes in localized states in addition to influences from ionized donor and acceptor states. Therefore, the capacitance transient is influenced by a change in the depletion capacitance as emission or capture of electrons or holes from deep levels effect the charge within the depletion region. The changes in capacitance are easily measured in order to extract the capture or emission rates of the deep levels. Thus, deep levels may be characterized using depletion capacitance methods. The ratio of the electron thermal emission rate e_n to the electron thermal capture rate c_n of a deep level is given [2]:

$$\frac{e_n}{c_n} = \exp\left(\frac{E_t - E_F}{kT}\right) \qquad (C.3)$$

The term E_t is the energy of the deep level and E_F is the Fermi level. The electron thermal capture rate c_n of a deep level considering non-degeneracy may also be written

$$c_n=\sigma_n<V_{th}>N_c\exp\left(\frac{E_F-E_C}{k_BT}\right) \quad (C.4)$$

The term σ_n is the thermal capture cross-section for electrons, v_{th} is the electron thermal velocity and N_C is the effective conduction band density of states. By combining equations (C.3) and (C.4) together we may obtain an expression that relates e_n to trap energy and capture cross section as a function of temperature:

$$e_n(T)=\sigma_n<V_{th}>N_c\exp\left(\frac{E_t-E_C}{k_BT}\right) \quad (C.5)$$

For electron traps in an n-type semiconductor, the net emission rate τ^{-1} is effectively (c_n + e_n). In the case of a fully occupied majority carrier electron deep level in a depletion region at large reverse bias, the electron thermal capture rate is $c_n \sim 0$ due to the lack of free carriers. The space-charge in the depletion region changes in time as $q[N_d + N_t - n_t(t)]$, where $n_t(t) = N_t\exp(-e_nt)$ is the concentration of occupied traps, N_t is the total trap concentration, and N_d is the concentration of ionized dopants. For $N_t << N_d$, the capacitance can be expressed as:

$$\frac{\Delta C(t)}{C_0}\cong\frac{N_t}{2N_d}\exp(-e_nt) \quad (C.6)$$

The term C_0 is the final (steady-state) value of the capacitance and ΔC is the amplitude of the transient. Thus, this is the fundamental of depletion capacitance methods for deep level spectroscopy.

C.3.4 Deel Level Optical Spectroscopy

The optical characteristics of a deep level such as the classical optical ionization energy E_o and Franck-Condon energy d_{FC} can be extracted from the spectral dependence of the optical cross-section $\sigma^o(h\nu)$ [4]. The concentration of the deep levels (N_t) can also be found from the intimately related steady-state photocapacitance (SSPC) and LCV techniques. The energy E_o is the minimum energy required for a photon to promote an electron or hole from a localized bandgap state to a delocalized free carrier state upon absorption. The energy released in the form of multi-phonon excitation as the local bonding configuration relaxes around a defect center immediately after a photoabsorption or photoemission event is given by d_{FC}. The measurement of DLOS is presented in Figure C.1.

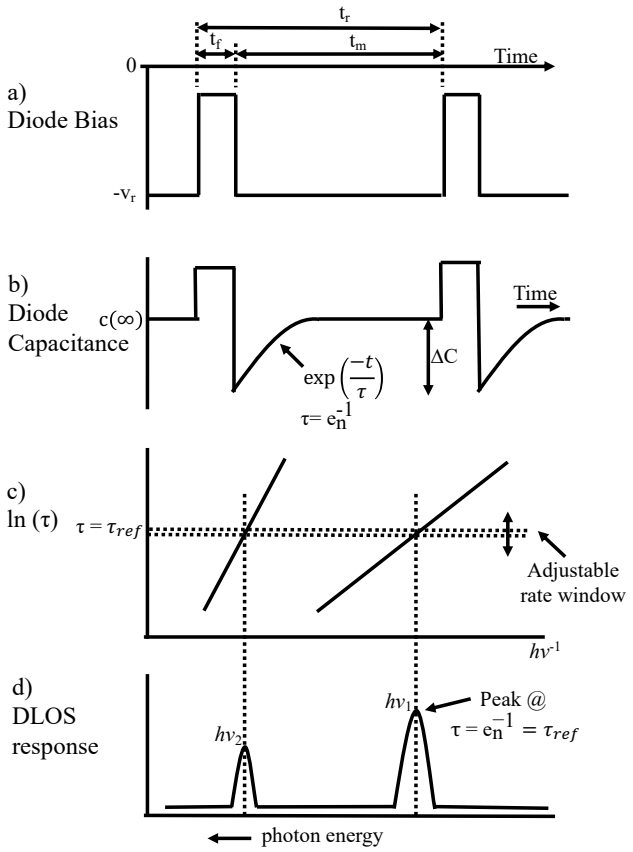

Figure C.1 Principles of the DLOS measurement and analysis

We will consider again an n-type Schottky diode. The DLOS measurement begins with the depletion region under reverse bias *Vr*, and the traps residing therein are assumed to be empty. A fill pulse bias *Vf* is applied for a time *tf* to collapse the depletion region and bring free electrons in proximity of the empty traps where capture occurs. When the fill pulse is removed and the free carriers retract, thermal emission of the trapped electrons produces an exponential capacitance transient with time constant $\tau_{ref} = 1/e_n$, which from equation C.5 depends on the temperature *T* and both E_{th} and σ_t. The temperature is held constant and low enough so that thermal emission rates are assumed to be negligible. Sweeping monochromatic illumination excites deep level emission and τ decreases, and the transient is processed into a signal that peaks at hv_m when τ equals the preset value τ_{ref}. As monochromatic illumination excites deep level emission, it is assumed that thermal emission rates are negligible. As the incident photon energy *hv* is scanned, the capacitance transient is measured to extract the optical emission rate that is given as:

$$e_o(hv) = \sigma_n^0(hv)\Phi(hv) \tag{C.7}$$

The term $\sigma_n^0(hv)$ is the optical cross section for electrons or holes. The term $\Phi(hv)$ is the photon flux (# photons/area·time) which is a function of the experimental setup. The time derivative of the photocapacitance transients C(t) near t = 0 is taken in order to extract $e_o(hv)$. It may be noted that photons with $hv < E_g/2$ can only cause electron emission from deep levels in the upper half of the bandgap. Also, photons with $h\nu > E_g/2$ can may only promote both electrons and holes from the same deep level to the conduction and valence

band, respectively. Thus, it is important to prime the deep levels to be initially either completely filled or completely empty so as to unambiguously isolate electron and hole emission. The occupied concentration if deep levels filled at t = 0 can be represented by:

$$\left.\frac{dn_t(t)}{dt}\right|_{t=0} = \sigma_n^0 \Phi N_t \qquad (C.8)$$

The change in $n_t(t)$ may be observed in a change in junction capacitance as:

$$\left.\frac{1}{C_o}\frac{dC(t)}{dt}\right|_{t=0} \cong \frac{1}{2N_d}\left.\frac{dn_t(t)}{dt}\right|_{t=0} \qquad (C.9)$$

The value of dC(t)/dt|t=0 is proportional to $\sigma^0_n(hv)$. This relationship holds even for ΔC ~ C0 [2]. The concentrations of Nt and Nd must be known beforehand in order to determine absolute values for $\sigma^0_n(hv)$. However, the spectral dependence is sufficient to determine photoionization energy (Eo) and the Franck-Condon energy (dFC) by fitting $\sigma_n^0(hv)$ to a theoretical expression.

C.3.5 Steady-state photocapacitance

Steady-state analysis of the photocapacitance spectrum also enables the deep level density Nt to be determined. Thus, steady-state photocapacitance (ΔC_{ss}) is recorded as a function of *hv*. Onsets of deep level emission occur near $hv \cong E_o - d_{FC}$ which identify individual deep levels whose concentrations are given by:

$$\frac{\Delta C_{ss}}{C_0} \cong \frac{N_t}{2N_d}\frac{\sigma_n}{\sigma_n + \sigma_p} \qquad (C.10)$$

This ratio is maximized for *hv* that produces the largest photocapacitance response. Again, for $h\nu > E_g/2$, competing electron and hole emission can occur from the same deep level, putting a lower limit on N_t. The expression is typically valid for only $\Delta C << C_0$.

C.3.6 Lighted capacitance-voltage measurements

As mentioned previously, a change in the junction capacitance ΔC due to trapped carrier emission from deep levels due to incident photons is observed due to photoionized carriers that are swept from the junction of a Schottky diode. Additionally, a change in space charge within the depletion region is also observed. The junction capacitance ΔC is small compared to the dark quasi-equilibrium junction capacitance C_0 when $N_t << N_d^+$. This indicates that the depletion depth remains approximately constant and the photocapacitance transient proceeds exponentially. However, when $Nt \sim N_d+$, the junction capacitance ΔC may become comparable to C_0. When this occurs, the space charge within the depletion region is rearranged due to deep level emission. The movement of the depletion depth correlates with a non-exponential behavior of the capacitance for times less than the inverse of the electron thermal emission rate $(e_n)^{-1}$ [4]. Therefore, the determination of e_n from the capacitance transient at a time $t < (e_n)^{-1}$ may produce an erroneous value for e_n and an incorrect thermal activation energy E_a.

Using DLOS, the optical electron emission rate e_n^0 is determined from the initial rate of change of the depletion capacitance with respect to time upon illumination. Thus, the onset of e_n^0 in the photocapacitance transient corresponds with the onset of the optical cross-section $\sigma(h\nu)$ of a deep level. Thus, $dC(t)/dt|_{t=0} \propto e_n^0$ is valid even for $N_t \sim N_d^+$ [2].

This allows the differential capacitance transient analysis to produce the proper spectral dependence of $e_n^0(h\nu)$ from which the optical ionization energy E_o is determined by fitting $\sigma(h\nu)$ to a theoretical expression [4] .

Thus, deep levels with $N_t \sim N_d^+$ can be spatially profiled using similar techniques to determine the net dopant concentration in semiconductors using *C-V* profiling. The difference in voltage ΔV required to maintain a junction capacitance C when a deep level is filled compared to when it is empty, is equal to the integrated space charge of the deep level in the depletion region. Therefore, differentiating ΔV with respect to C provides a spatial profile of the deep level $N_t(x)$, with $x = A\varepsilon_s/C$ [5]. Therefore, the difference in net fixed charge densities determined via LCV scans taken with the deep level both empty and full are attributed to $N_t(x)$. Once steady-state is reached under illumination, the only change within the space charge of the depletion region occurs due to a change in deep level occupancy at the depletion depth as it moves through the semiconductor during the LCV scan.

C.4 Atomic Force Microscopy

Atomic force microscopy (AFM) is a method to "image" the surface morphology of as-grown surfaces on m-plane GaN. AFM is enabled via a small centiliter probe (typically Si) which is placed on (contact-mode) or in close proximity (tapping-mode) to a sample surface.

The cantilever is raster scanned in order to effectively image the sample surface. Imaging is enabled by the bending of the cantilever via surface features (contact-mode) or through attractive or repulsive interactions between the sample surface and cantilever

(tapping-mode). The tapping-mode is elaborated further for the purposes of this dissertation. Attractive or repulsive interactions are measured via observing changes in the sinusoidal motion of the cantilever which is oscillated near its resonance frequency. The amplitude of the sinusoidal motion is kept constant via A feedback-loop. The feedback-loops consisting of a detector-source configuration which closely monitors the cantilever quasistatic deflection and voltage bias of the potential between cantilever and sample. Therefore, the surface morphology is traced line by line utilizing this tapping-mode configuration of an AFM.

Surface morphologies of samples of MOCVD grown *m*-plane GaN are imaged via an Asylum Research MFP-3D-BIO AFM operated in a tapping-mode configuration. A MikroMasch low frequency tapping-mode AFM cantilever with a force constant of 45 N/m and resonant frequency of 190 kHz is utilized. The cantilever is focused on the probe tip to ensure no deflections and the proper amplitude. The cantilever is then calibrated and tuned for tapping mode based on its force constant and resonant frequency. The cantilever is then lowered into close proximity of the sample surface by monitoring the DC voltage (~ 50-60 mV). Number of points is set to 512/line, scan rate is set to 1 Hz, and the scan angle is set to 90°. The AFM image window is set to 20 μm x 20 μm. Integral gain and voltage threshold are set to 20 and 650 mV, respectively, in order to achieve proper resolution of the sample surfaces. AFM images consist of height, amplitude, and phase 2-D plots. Upon completion, root-mean-square (RMS) roughness calculations are conducted on the height scan of the resulting AFM images. Results of these images and RMS values are presented for various growths of m-plane GaN throughout this dissertation.

C.5 Radio Frequency (RF) impedance measurements

This section presents information about the radio frequency RF setup and impedance measurements. Details on the network analyzer, measurement calibration, configuration, and data analysis for the work presented in this dissertation is elaborated.

C.5.1 RF measurement setup

The configuration of the RF setup is presented in Figure C.2. Impendence measurements are enabled via a Keysight e5061b network analyzer (NA) by combining a time-dependent small-signal voltage provided by port 1 of the NA to a DC bias via a bias-tee. The *p-n* diodes tested are probed using a Cascade Microtech Inc. (ACP40-GS-150) micro-RF ground-signal-ground probe. The frequency range capability of the NA is from 5 Hz to 3 GHz. A frequency range of 500 kHz to 2 GHz is selected for the devices presented in this dissertation. The real and imaginary parts of the complex impedance were extracted from the measured reflection coefficient (S_{11}) via the equation below:

$$Z = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \qquad (C.11)$$

The power level at the transmitter ranges from -30 dBm to 10 dBm . The Measurements presented in this dissertation are carried out at a power -20 dBm with a peak-to-peak amplitude of ~20 mV. The maximum intermediate-frequency (IF) bandwidth of the NA is 3KHz. The IF bandwidth and refers to the filters that are used inside the NA to detect the signal at the receivers. The IF bandwidth is set to 500 Hz for the experiments presented. Thus, this low IF bandwidth ensured the accuracy of the measurement of the modulation response.

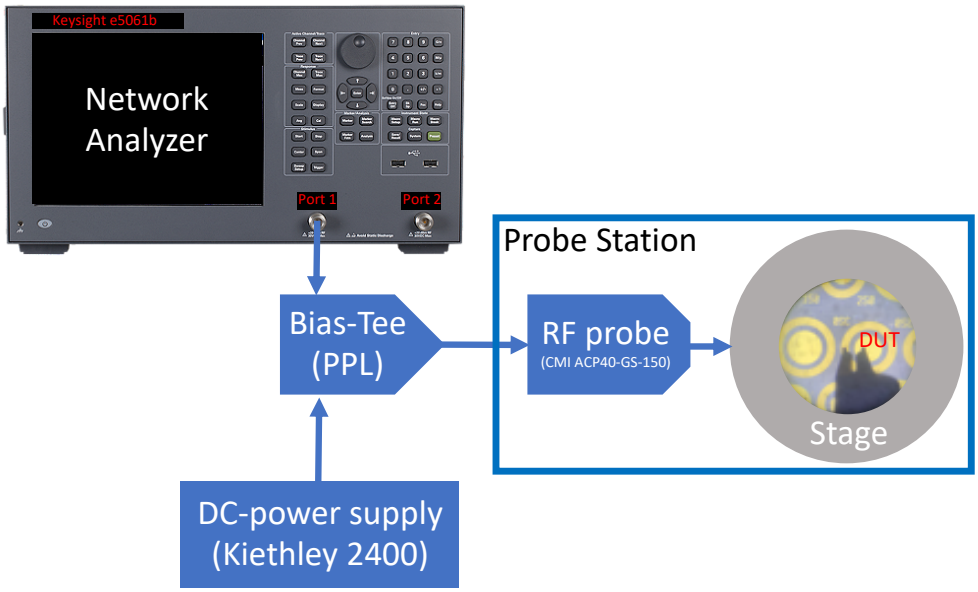

Figure C.2: RF measurement configuration

C.5.2 Calibration of System

Calibration of the port impedance (S_{11}) is required in order to remove the response from all cables, connectors, and electrical junctions. Thus, these components are selected to operate with a constant response (Typically 50-Ω impedance) across the frequency range of testing. The Cascade Microtech GS RF micro-probe has a -3dB bandwidth up to 50 GHz. The Picosecond Pulse Lab bias-tee ensures a minimum reflection of pulses with frequencies above 12 GHz. Connections between components consist of SMA cables (3.5 mm or 2.4 mm). Typically, the 2.4 mm cables can go up to 67 GHz while 3.5 mm cables can go up to 18 GHz. The use of adaptors may also be used to accommodate interchangeability.

All components, cables, and electrical junctions of the RF setup are calibrated in order to discriminate the response of the device under test (DUT). Therefore, the response of the DUT can be lost in the overall response of the rest of the setup.

Calibration is assisted by the NA by measuring the response (S_{11}) of the system with impedances of *open*, *short*, and *load(50-Ω)* from calibration kit. The calibration is subsequently subtracted from the response (S11) when measuring the DUT.

C.5.3 Data Analysis

Data is analyzed via fitting the measured input impedance response (S_{11}) to an equivalent small-circuit model (Chapter 4) to obtain the dynamic parameters versus frequency. The fittings are easily obtained via the assistance of software (MATLAB) which enables the implementation of an assortment of non-linear fitting functions. The MATLAB function used for this work is defined as *nlinfit.* In this function, an estimation of the fitting parameters (circuit parameters) for a nonlinear regression of a response (complex impedance) to predictors (frequency) based on the specific model is utilized. A least squares estimation is utilized to obtain parameters based on initial values. Initial values must be carefully selected based on previous simulations or from physical models in order to ensure the fittings are convergent. Thus, a 95% confidence interval for predictions of the nonlinear regression of the nonlinear least squares parameter is required. These estimates are enabled via the MATLAB function *nlpredci*. The function returns residuals and a variance-covariance matrix of the fittings for the model at the input data points. Thus, if the estimated parameters fall in between the confidence intervals, the robustness of the fittings is ensured.

Additionally, simultaneous fittings of the dependent real and imaginary impendence spectrum are enabled through the implementation of the *nlinfit* wrapper function. This implementation is used to call another function. The wrapper function

enables the same simulation/function with different parameters and also allows the parameters to be modified independently. Therefore**,** a N×2 (N = number of data points) matrix is computed utilizing this method for the simultaneous fit of the complex impedance. A small-signal circuit simultaneous fit is made using the complex impedance spectrum from measured diodes.

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