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# A Unique Analog-to-Digital Voltage Conversion Network

Thomas O. Summers

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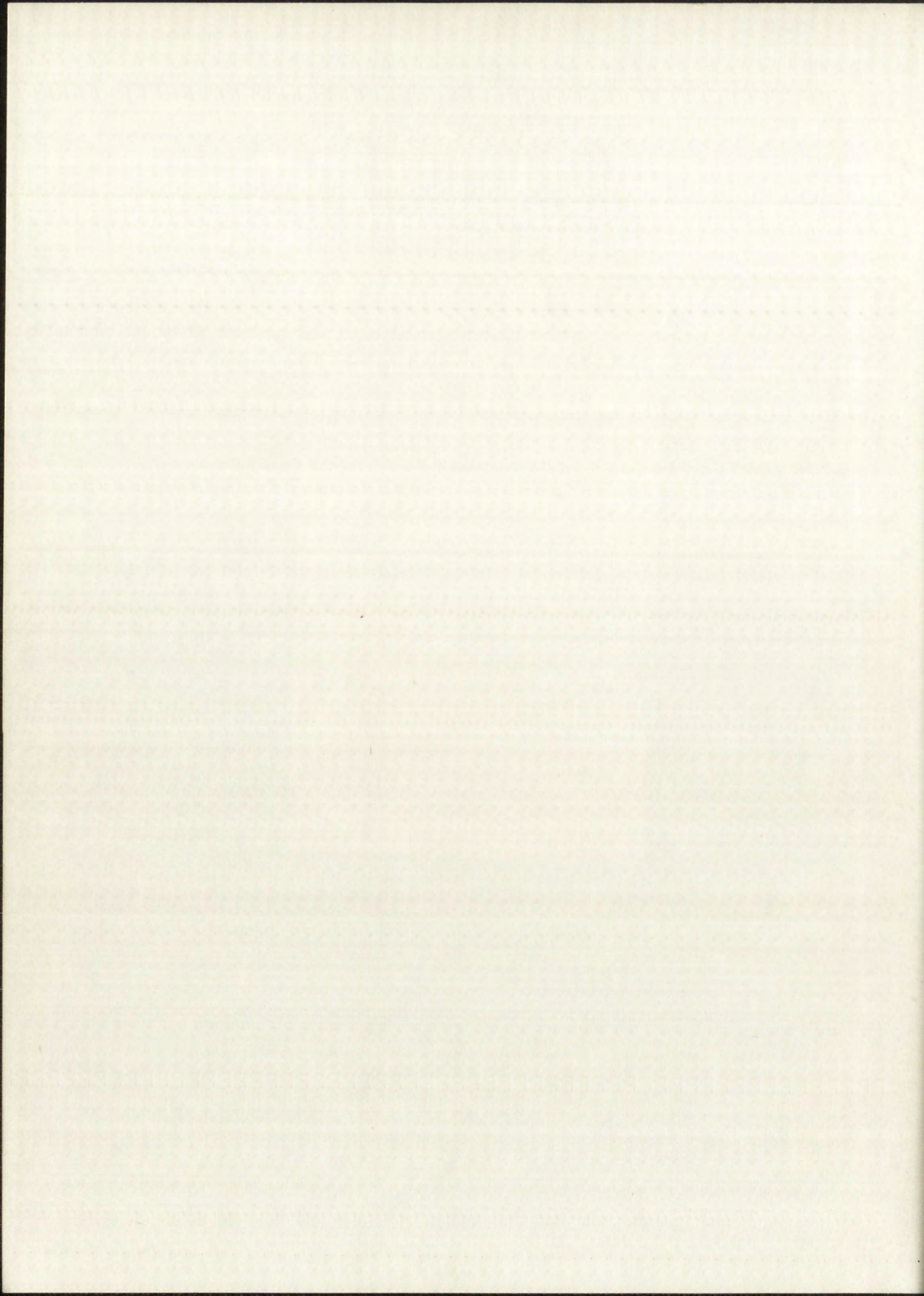
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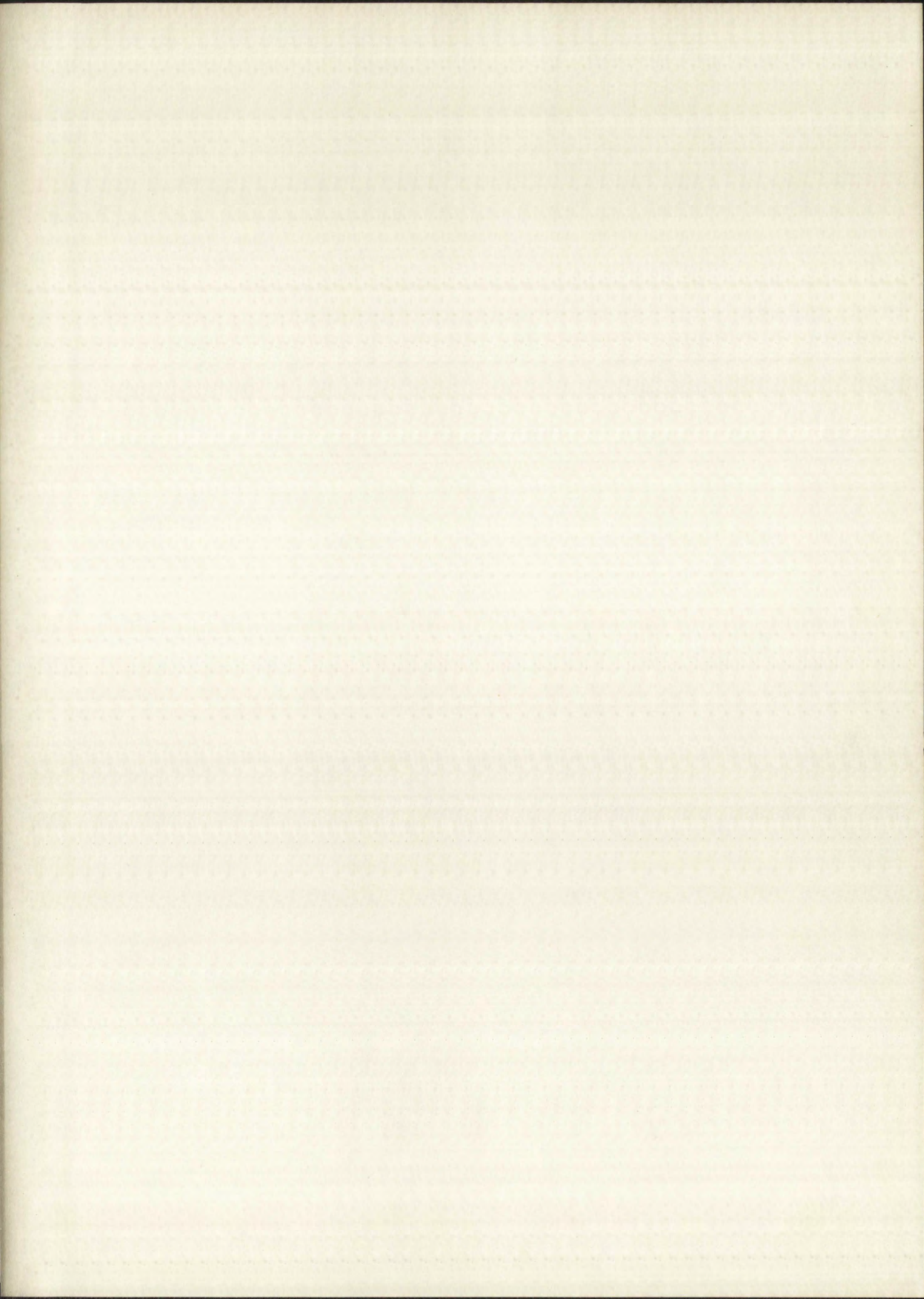
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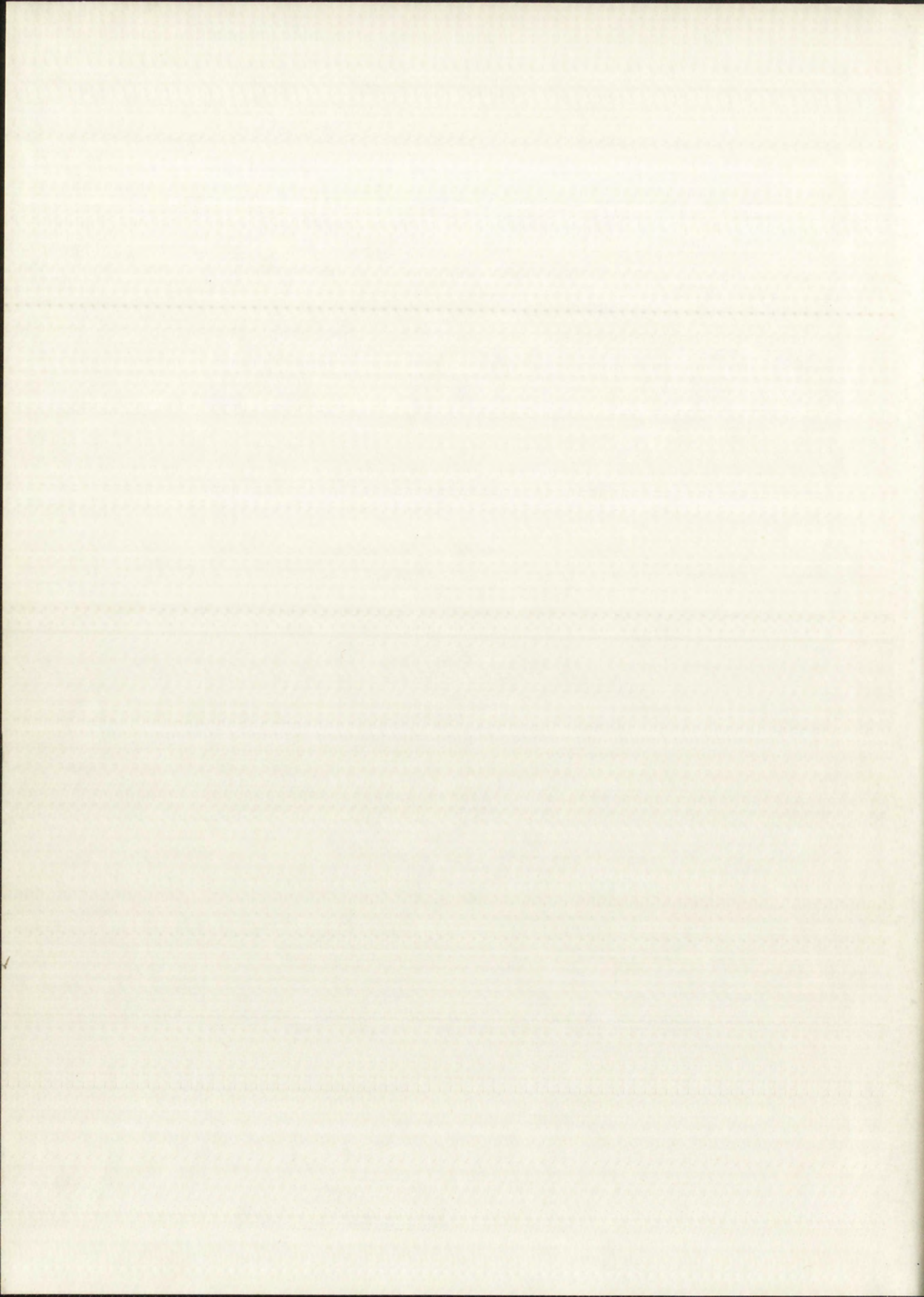
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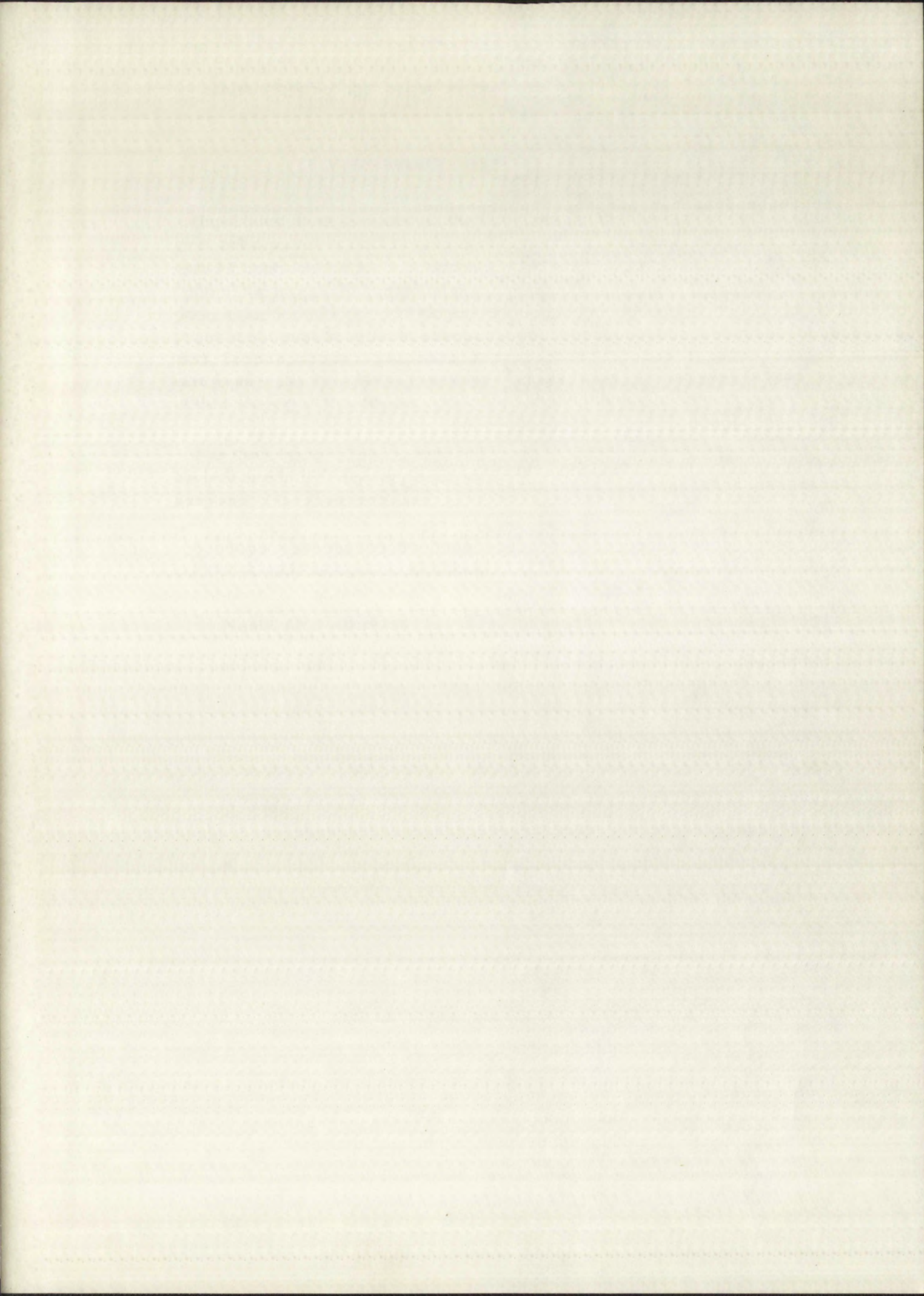


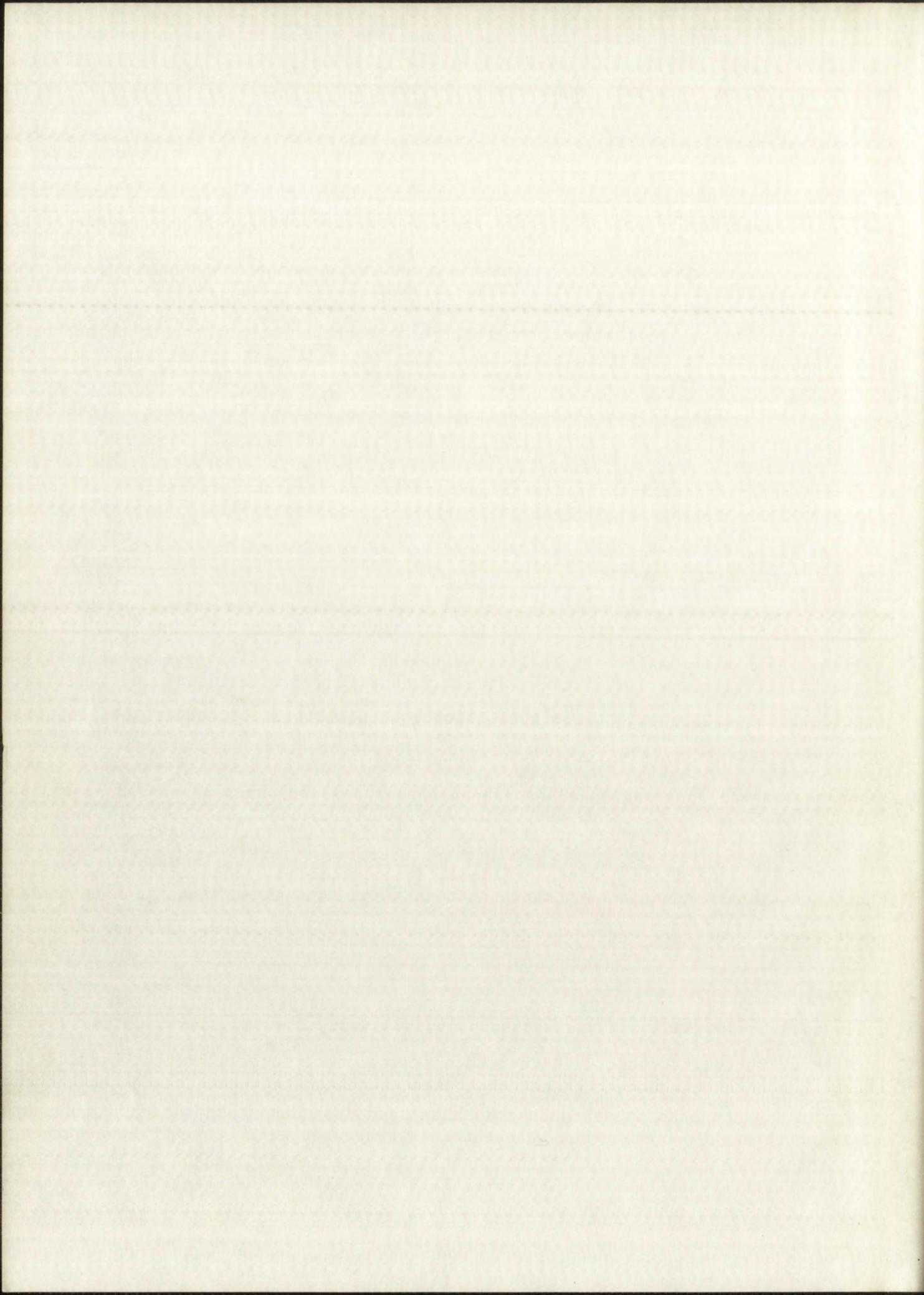














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A UNIQUE ANALOG-TO-DIGITAL  
VOLTAGE CONVERSION NETWORK



By

Thomas O. Summers

A Thesis

Submitted in Partial Fulfillment of the  
Requirements for the Degree of  
Master of Science in Electrical Engineering

The University of New Mexico

1962



THE UNIVERSITY OF CAMBRIDGE  
FACULTY OF ENGINEERING

THE UNIVERSITY OF CAMBRIDGE

1962



This thesis, directed and approved by the candidate's committee, has been accepted by the Graduate Committee of the University of New Mexico in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

W. J. Parist  
Dean

May 28, 1963  
Date

A UNIQUE ANALOG-TO-DIGITAL  
VOLTAGE CONVERSION NETWORK

Thesis committee

W. W. Kaysil  
Chairman

Al [Signature]

James [Signature]



This thesis, directed and approved by the candidate's committee, has been accepted by the Graduate Committee of the University of New Mexico in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Dean

Date

A UNIQUE ANALOG-TO-DIGITAL  
VOLTAGE CONVERSION NETWORK

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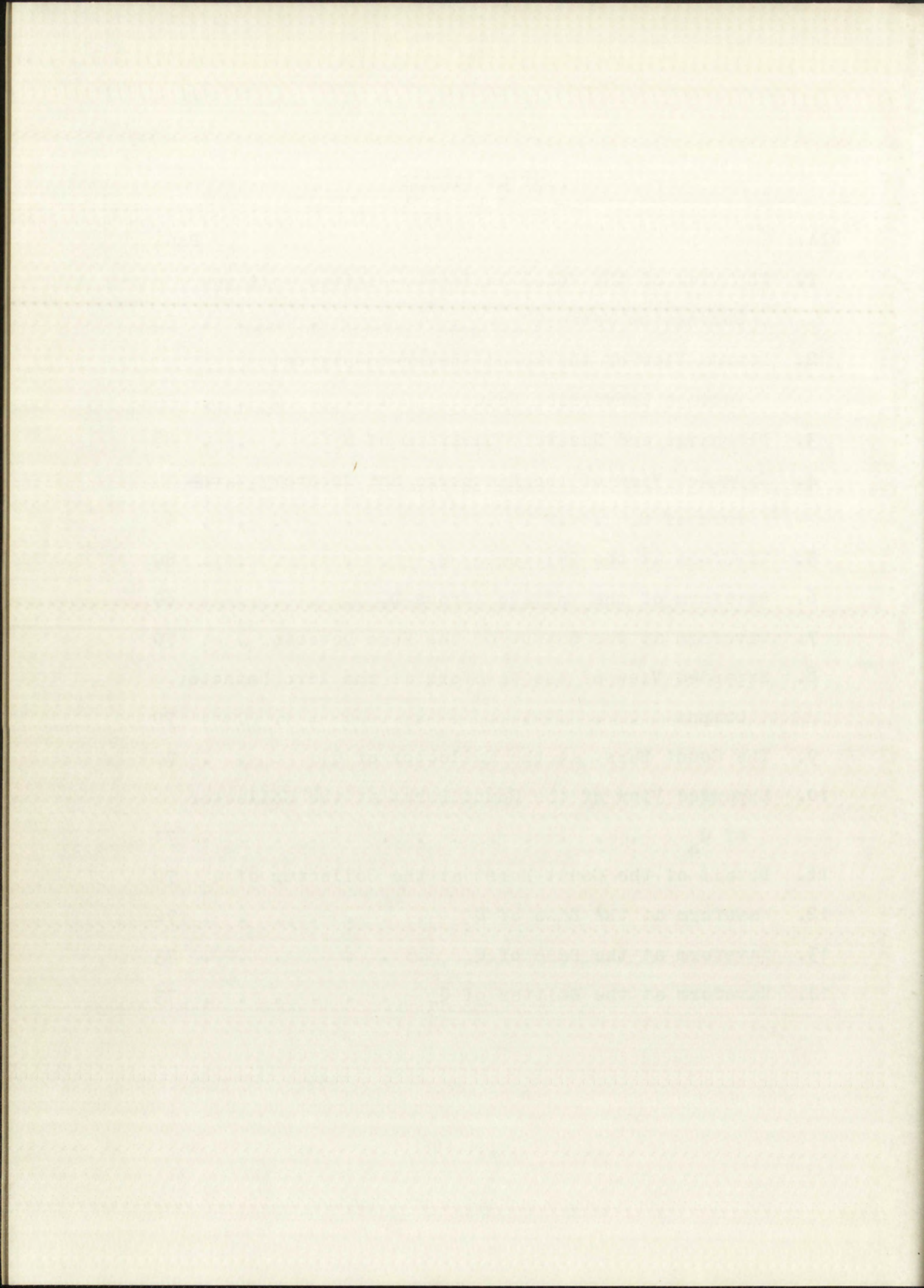
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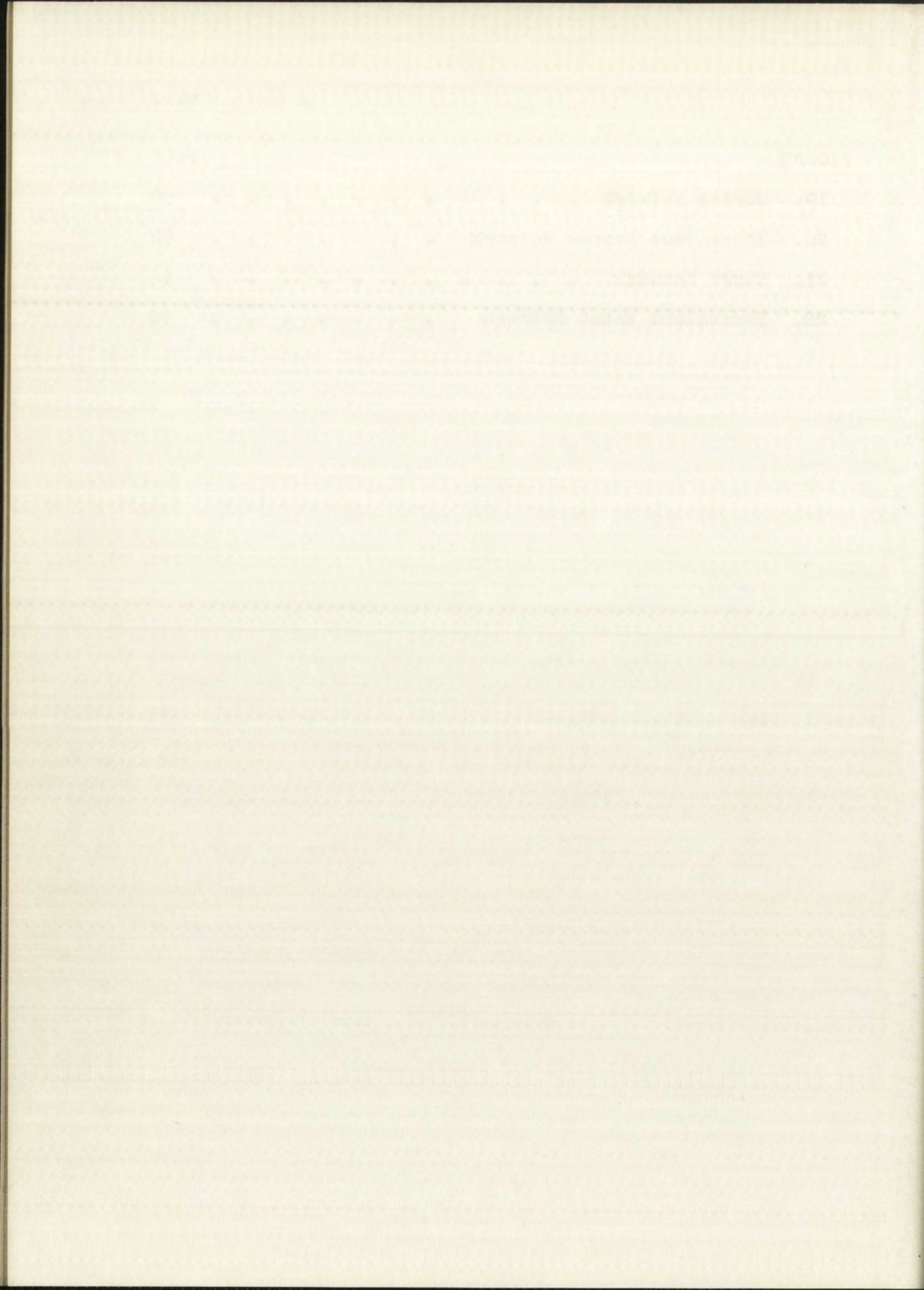




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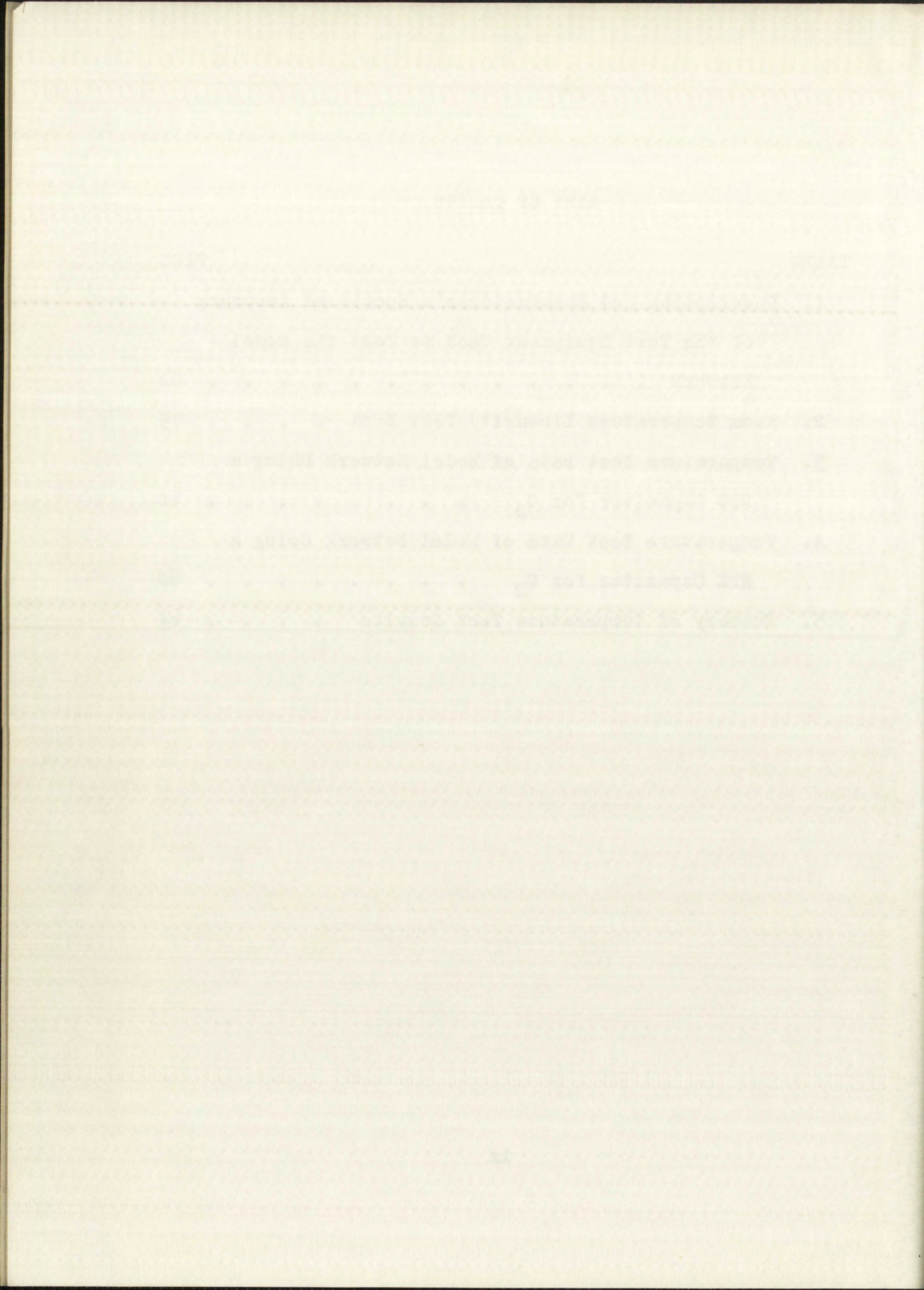
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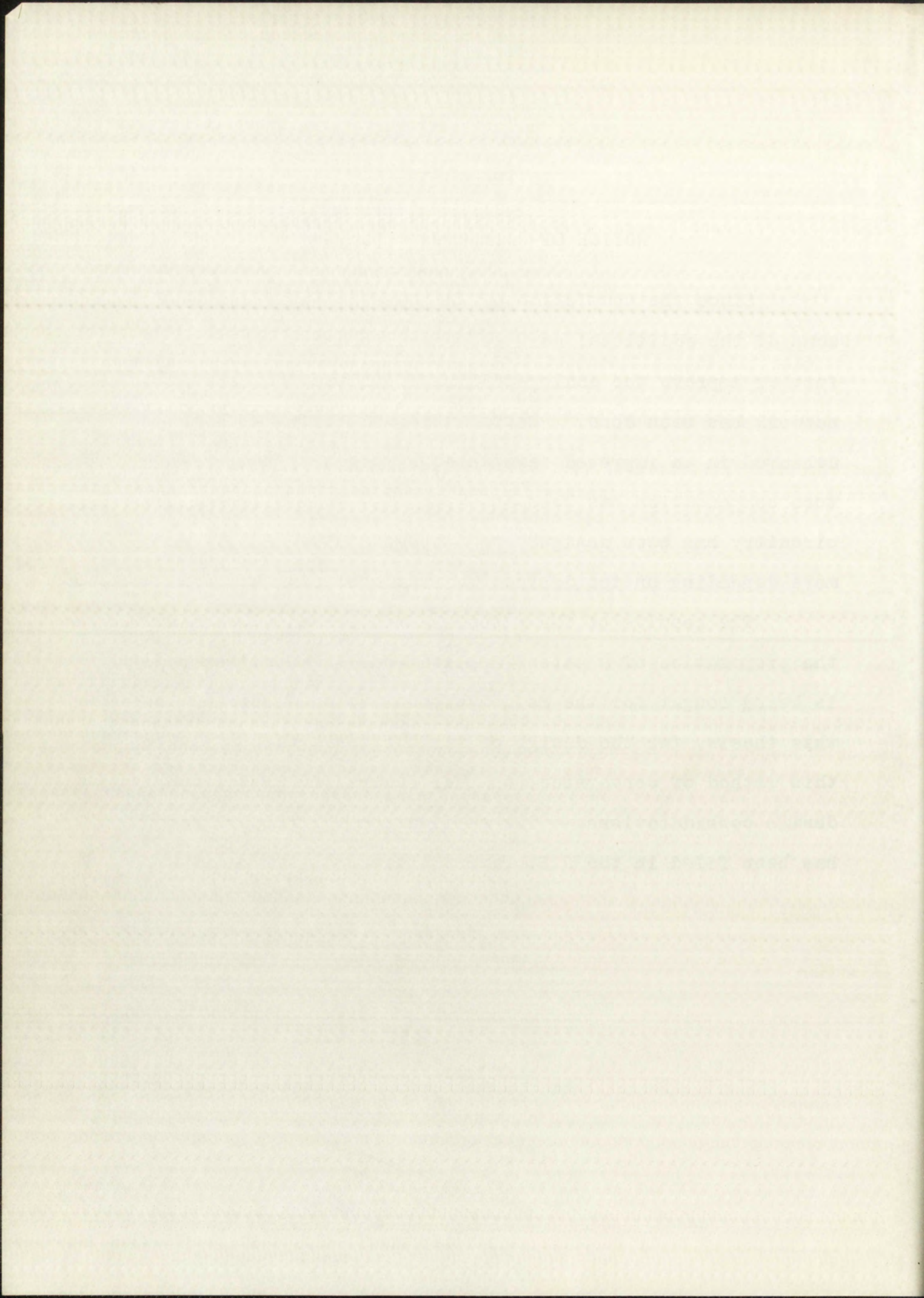


## TO THE READER

### NOTICE OF PATENT IN PROCESS

Since the completion of this thesis in August 1962, some of the additional work suggested in chapter six to further improve the analog-to-digital voltage conversion network has been done. Better zero stability has been achieved in an improved zero detector circuit; temperature compensation has been accomplished; and multiplexing circuitry has been designed to accommodate ten inputs or more depending on the desired maximum operating temperature.

The results of the patent search seemed to warrant the preparation of a patent application. Patent coverage is being sought for the method of conversion described in this thesis, for the design of various converters utilizing this method of conversion, and for several multiplex operation design considerations. The application for Letters Patent has been filed in the U.S. Patent Office.





## CHAPTER I

### INTRODUCTION

#### I. PURPOSE

The purpose of this thesis is to describe the origin, theory, operating principles, and design of a unique analog-to-digital voltage conversion network.

#### II. ANALOG-TO-DIGITAL CONVERSION DEFINED

Analog-to-digital conversion is, in the broad sense, the process of assigning to a representative quantity (analog) a numeric or digital equivalent. The oldest and still most common analog-to-digital converter is man. Every time an investigator observes the position of a pointer, the height of a mercury column, or the position of the hands of a clock and records his observation in numeric form, he is performing an analog-to-digital conversion.\*

In recent years, common usage in the electronics industry has caused the term "analog-to-digital converter" to mean a device that accepts a continuously variable analog voltage and provides, as an output, some form of binary

---

\*This presumes that the investigator's intent is to measure quantities such as voltage, temperature, or time rather than just the position of a pointer, the height of a mercury column, or the position of the hands of a clock.

# Introduction

The purpose of this document is to describe the analog-to-digital converter and its operation. The converter is designed to convert an analog signal into a digital representation.

The converter consists of several stages. The first stage is the input buffer, which provides a high impedance input to the converter. The second stage is the sample-and-hold circuit, which samples the input signal and holds it for a period of time. The third stage is the comparator, which compares the sampled signal with a reference voltage. The output of the comparator is a digital signal, which is then converted back to an analog signal by the output buffer.

In recent years, common usage of the converter has increased. This is due to the fact that the converter is now available in a wide range of packages and prices. The converter is also becoming more popular in applications where high accuracy and low noise are required.

The converter is a very important component in many systems. It is used to convert the analog signals from sensors and transducers into digital signals that can be processed by a computer. The converter is also used in many other applications, such as in the control of motors and in the measurement of physical quantities.



representation of the input voltage. Technically, such a device is an analog-to-digital voltage converter.

In this thesis the distinction between an analog-to-digital voltage conversion network and an analog-to-digital voltage converter is that the conversion network is the essential circuitry in an analog-to-digital converter, but it does not include all the circuitry found in a converter; the conversion network described in this thesis requires the addition of a counter circuit and power supply to make up a complete analog-to-digital converter.

### III. THE PROBLEM

The increasing utilization of digital data acquisition systems has resulted in the design and development of a large number of different analog-to-digital voltage converters [ 9 ] .\*

Each of these designs exhibits varying specifications with regard to accuracy, speed, environmental tolerance, reliability, and cost.

These specifications are usually interrelated and the nature of the interrelations are, in turn, related to the design approach.

As an example of these interrelations, one could consider the specifications of a converter designed around an electro-

---

\*The asterisk (or asterisks) signify the footnote (or footnotes) on that page. Arabic numerals in square brackets indicate references in the List of References on page 96.

...of the input voltage ...  
...in an analog-to-digital converter.

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### III. THE THEORY

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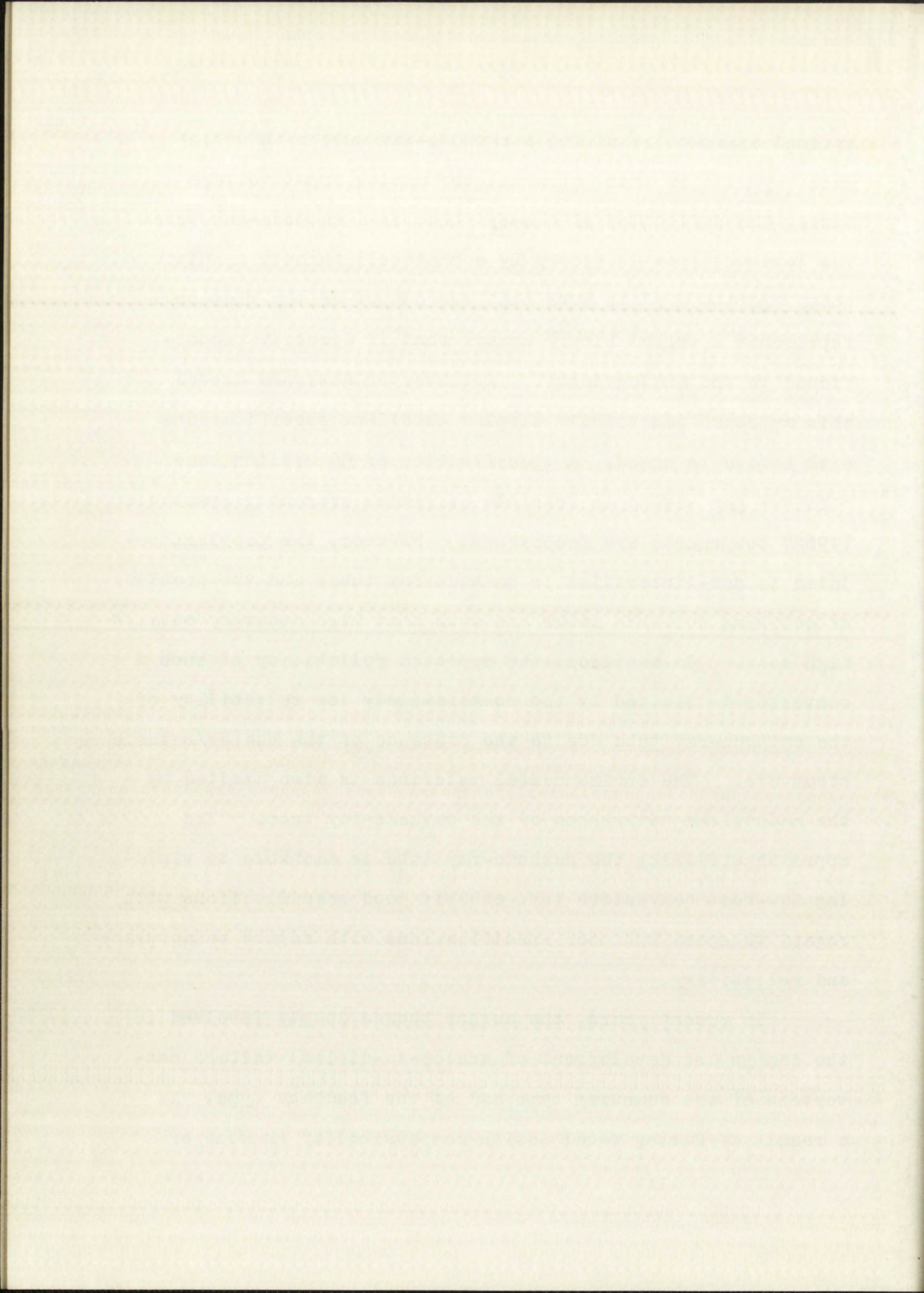
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optical approach requiring a cathode-ray tube with coding mask [ 9 ]. In this approach, the analog input voltage causes the deflection of a swept beam in a cathode-ray tube. The luminous spot is viewed by a photocell through a suitably coded aperture plate such that the output of the photocell represents a serial binary number that is directly proportional to the analog input. A converter designed around this approach can readily display excellent specifications with regard to speed. A specification of 50 million conversions per second is feasible utilizing presently available (1962) components and techniques. However, the problems related to non-linearities in cathode-ray tubes and the problems of devising suitable masks are such that high accuracy entails high cost. In addition, the expected reliability of such a converter is limited by the comparatively low reliability of the cathode-ray tube due to the presence of the heater/cathode structure. The environmental tolerance is also limited by the mechanical weaknesses of the cathode-ray tube. The approach utilizing the cathode-ray tube is amenable to yielding low-cost converters that exhibit good specifications with regard to speed but poor specifications with regard to accuracy and reliability.

In recent years, the author became deeply involved in the design and development of analog-to-digital voltage converters of the counting type and of the feedback type. As a result of having total design responsibility on some of

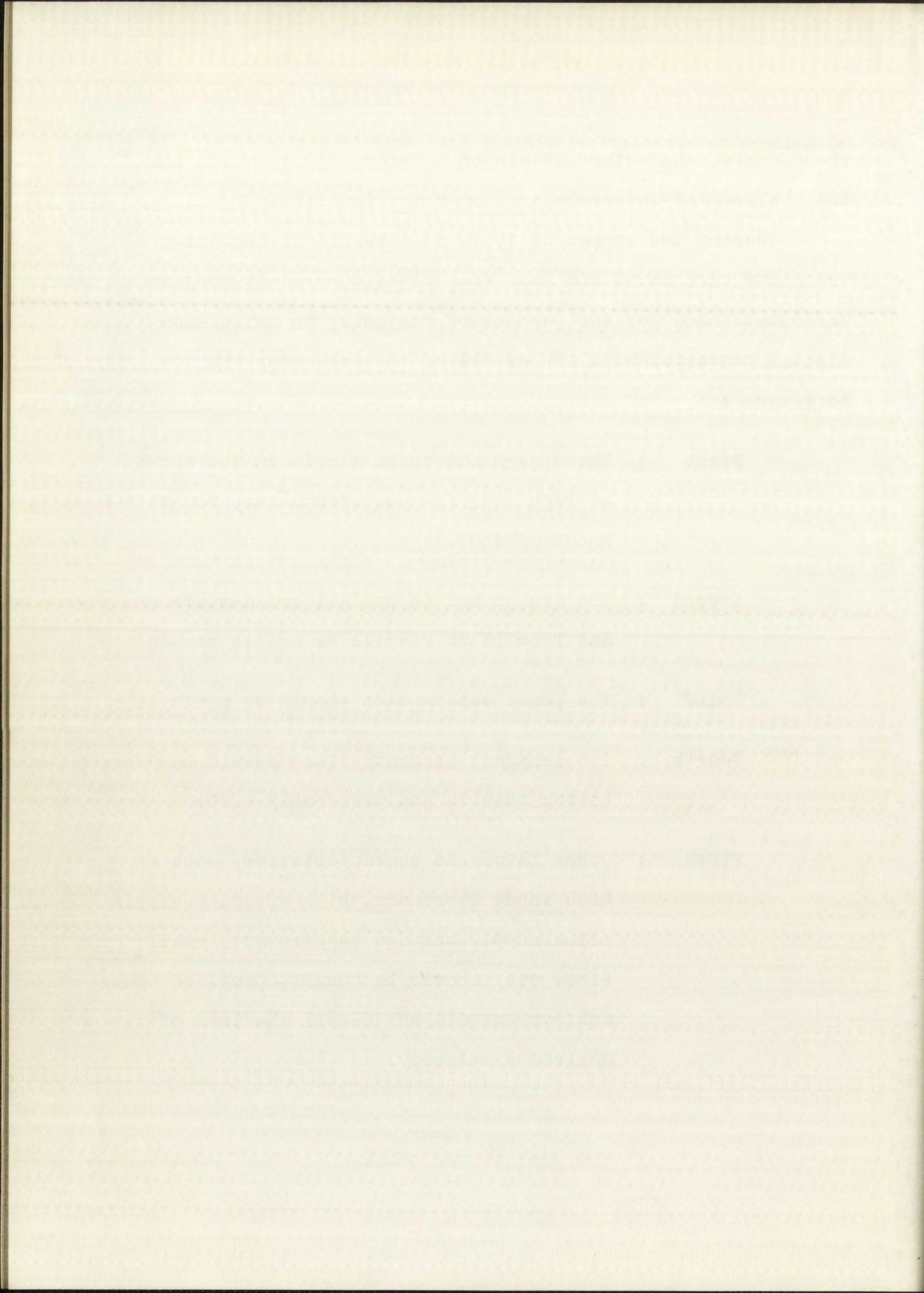




these units, the author developed a strong appreciation for the problems of interrelations of specifications.

During the summer of 1961, as a result of acquiring the above background and some free time, a personal program was established for the purpose of designing an analog-to-digital converter with any or all of the following characteristics :

- First : The design had to be simple in the sense of requiring few components compared to known designs.
- Second : The design had to be "all solid-state" and require no fragile or exotic components.
- Third : The power consumption should be minimal.
- Fourth : The inherent accuracy limit should be better than 1% and preferably 0.1%.
- Fifth : Other favorable characteristics, such as : high input impedance, high speed, a simple prime supply voltage requirement, small size, etc. should be sought, provided their achievement did not entail the loss of the desired simplicity.





In time, the development program proved successful. The following chapters embody a report of the orderly development of this program and an evaluation of the results of this program to determine the degree of success achieved.

#### IV. THE ORGANIZATION

In the following chapters, the report and analysis of the development of an analog-to-digital conversion network proceeds in approximate chronological order.

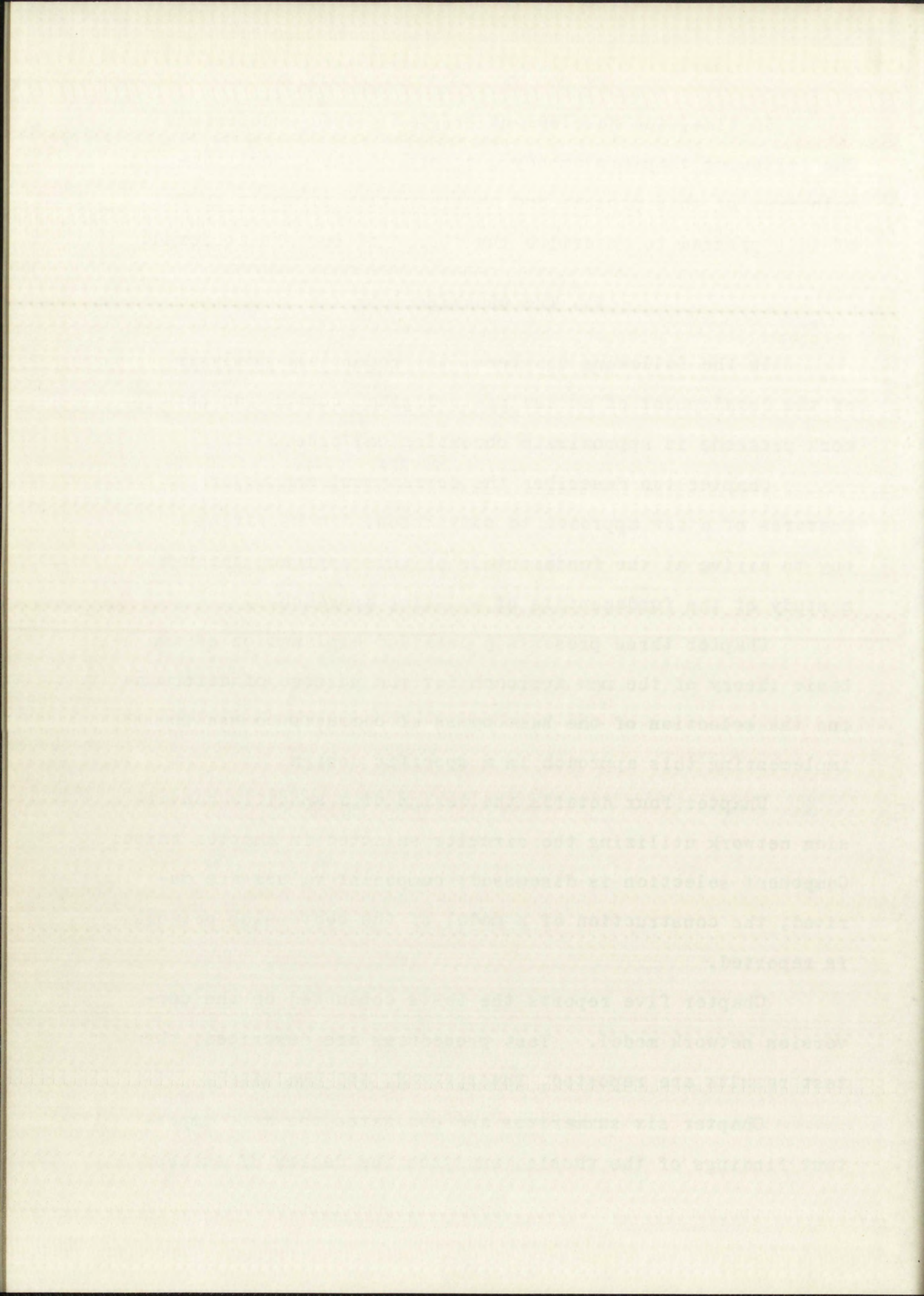
Chapter two describes the development and major features of a new approach to conversion, demonstrating a way to arrive at the fundamentals of this approach through a study of the fundamentals of existing approaches.

Chapter three presents a detailed explanation of the basic theory of the new approach for the purpose of determining the selection of the best types of circuits to use in implementing this approach in a specific design.

Chapter four details the design of a specific conversion network utilizing the circuits selected in chapter three. Component selection is discussed; component values are derived; the construction of a model of the conversion network is reported.

Chapter five reports the tests conducted on the conversion network model. Test procedures are described; the test results are reported, interpreted, and evaluated.

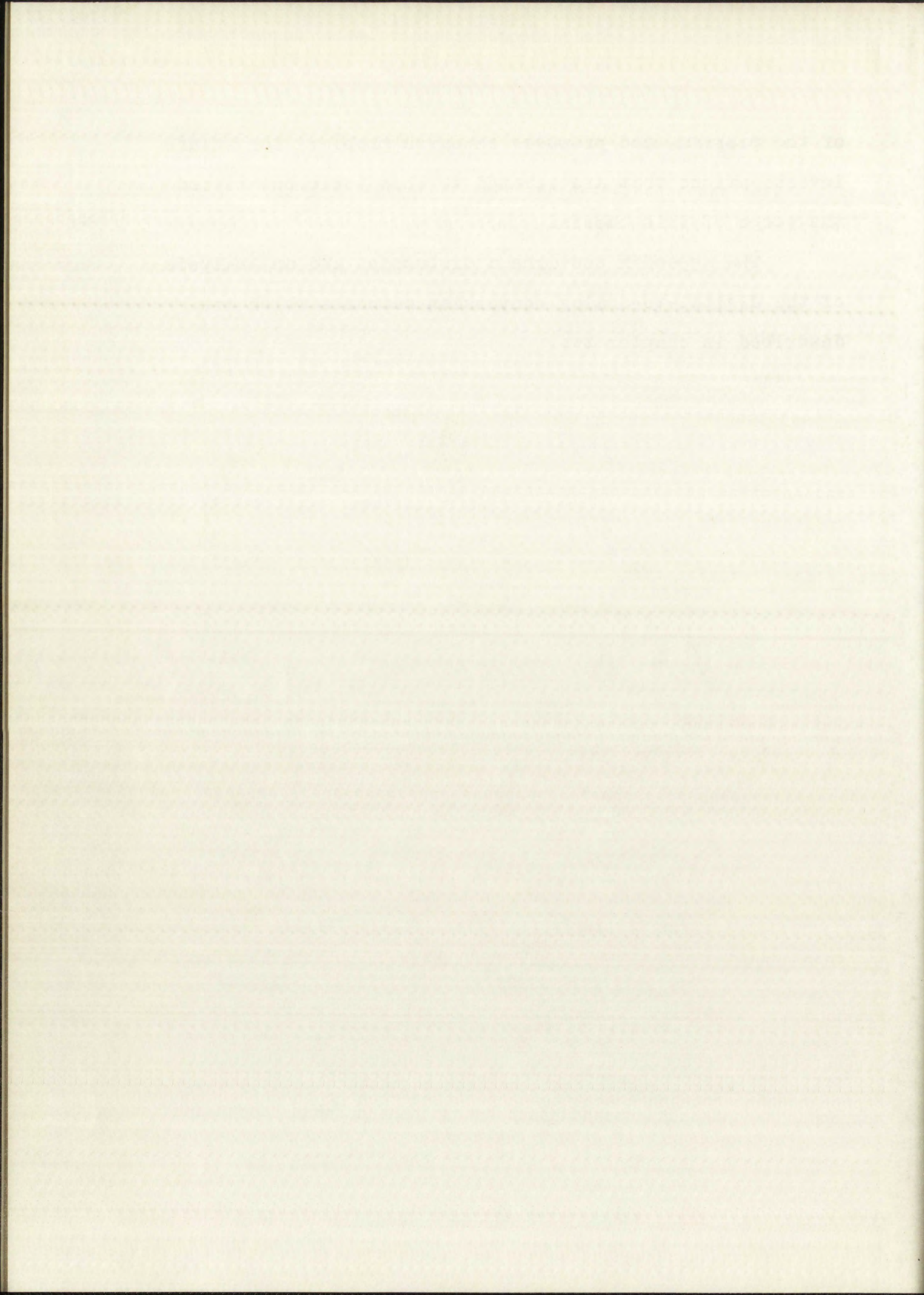
Chapter six summarizes and evaluates the most important findings of the thesis, analyzes the degree of success





of the program, and proposes research problems for future investigations that are related to this topic but beyond the scope of this thesis.

The appendix contains a discussion and an analysis of the digital-to-analog conversion networks which are described in chapter two.





## CHAPTER II

### THE FUNDAMENTAL APPROACH

The purpose of this chapter is to logically derive a different approach to analog-to-digital conversion through an analysis of other approaches to conversion. The study of other approaches begins by establishing two general classifications of converters as an aid in describing and analyzing two specific types of converters. From the analysis of the two types, a new approach is derived.

#### I. GENERAL CLASSIFICATIONS

For the purposes of this analysis, converters are classified as employing a synthesis procedure or a decomposition procedure to achieve conversion.

Conversion by synthesis. Conversion by synthesis involves the controlled generation of a voltage that is caused to be equal to the unknown voltage. The digital output is derived from the controlled voltage. In general, the synthesized voltage is not equal to the unknown voltage until some time after the process of forming that voltage is started. This means that the exact time of voltage measurement cannot be predicted before the measurement starts.





Conversion by decomposition. Conversion by decomposition is accomplished by acting on a stored sample of the unknown voltage in such a way as to decompose that sample and in so doing, produce a digital number representing the amplitude of the original sample. Because the unknown voltage is stored and processed, the voltage measurement indicates the magnitude of the unknown voltage at the time the sample was taken. In general, the time of measurement can be predicted before the measurement process is started.

## II. ANALYSIS OF TWO TYPES OF CONVERTERS

The converters to be analyzed are : (1) a digital ramp converter [ 17 ] , and (2) a pulse-peak-amplitude converter [ 10 ] [ 14 ] [ 15 ] [ 16 ]. These converters are fully described in the references cited, so this analysis considers only those features that are important to the ultimate purpose of arriving at a new approach to conversion. The first type utilizes the principle of synthesis, while the last type utilizes the principle of decomposition.

Digital ramp converter. The digital ramp converter utilizes the principle of synthesis. The internal voltage that is made equal to the unknown voltage is generated by a digital-to-analog network [ 7a ] [ Appendix ] which is controlled by a binary counter. The counter is, in turn, driven by a periodic pulse generator that can be started and stopped on command.





A block diagram of the major features of a digital ramp converter is shown in Fig. 1. The functions represented by the various blocks are :

The comparator signals when the synthesized voltage is equal to or greater than the unknown input voltage.

The digital-to-analog network generates a voltage (the synthesized voltage), the amplitude of which is directly proportional to the digital number contained in the counter.

The counter accumulates a digital representation of the number of pulses that are generated by the clock. Each stage of the counter drives a switch in the digital-to-analog network.

The clock generates a train of pulses to drive the counter. The clock is controlled by separate "start" and "stop" signals.

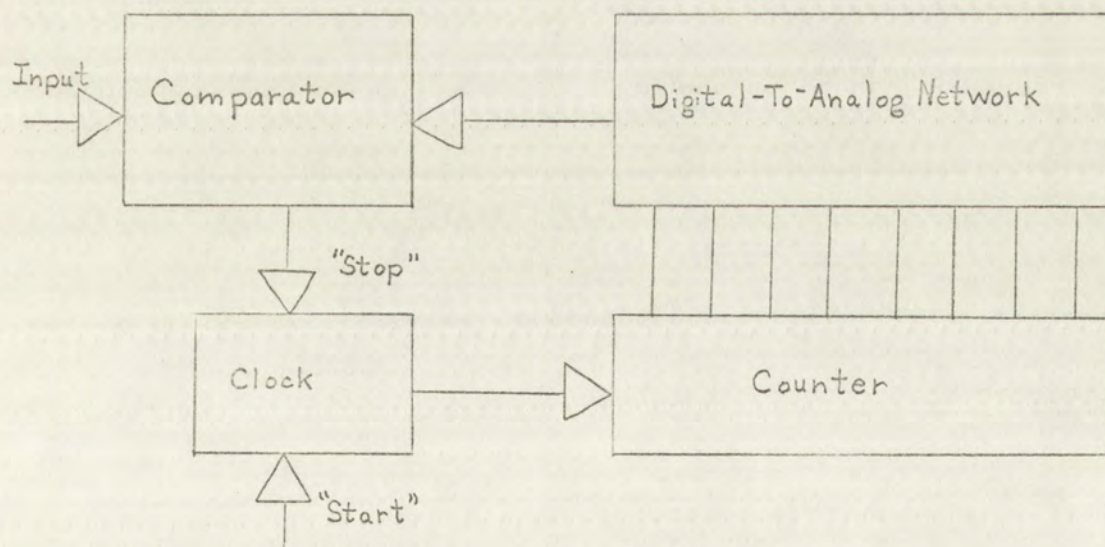
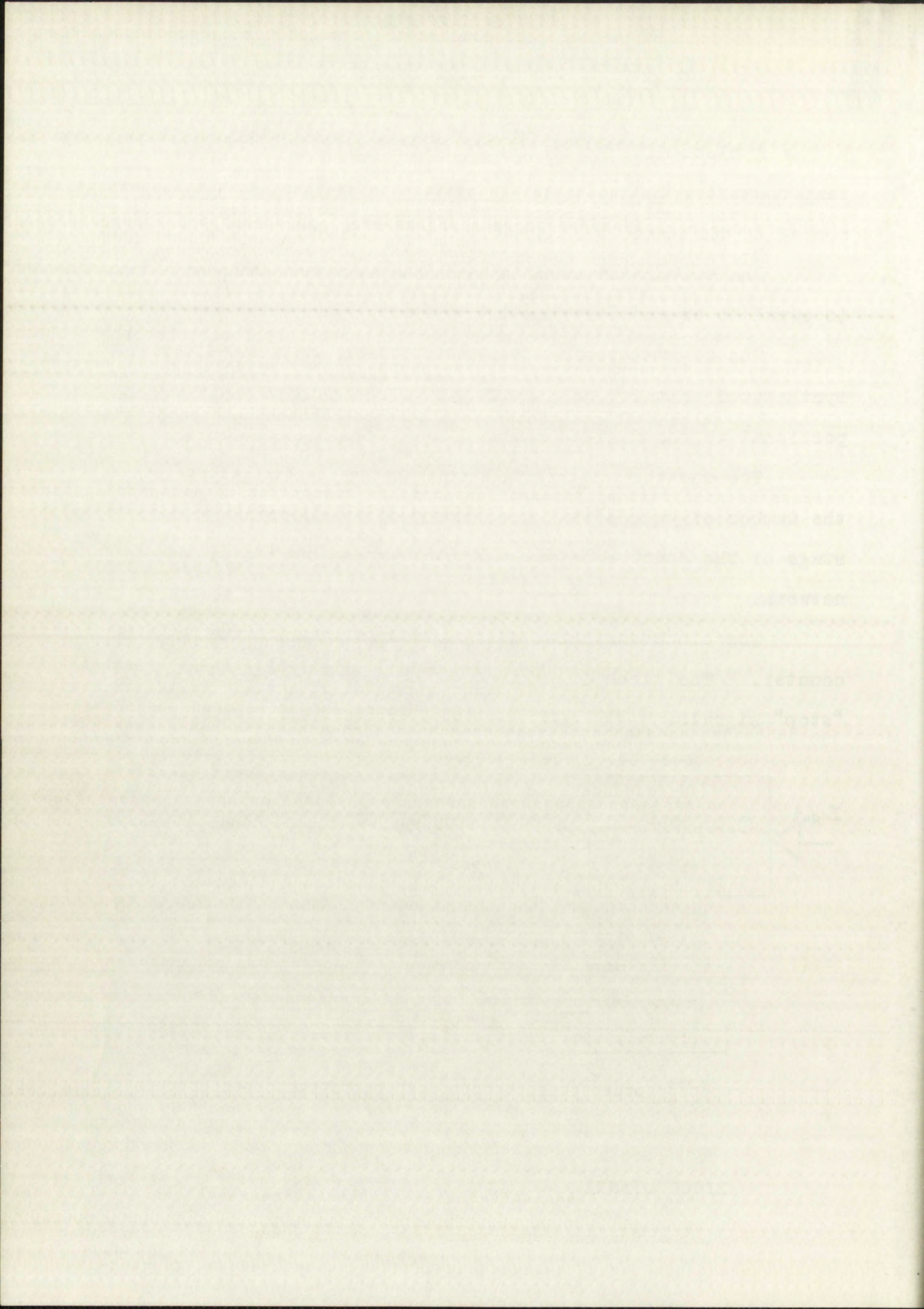


FIGURE 1

BLOCK DIAGRAM -- DIGITAL RAMP CONVERTER





A typical conversion cycle proceeds as follows :

The counter is set to zero so that the output of the digital-to-analog network is zero volts. When the clock receives a start signal, the clock begins sending pulses to the counter. As each pulse is sensed by the counter, the digital number represented by the various states in the counter is increased by one, which causes the output of the digital-to-analog network to increase by one voltage step for each pulse counted, thereby generating a staircase voltage. The counting process continues until the synthesized voltage equals the unknown voltage, at which time the comparator generates a signal that causes the clock to stop pulsing.

The conversion cycle is now essentially complete except for resetting the counter to zero. The counter contains a number that is related to the analog input by

$$V_{in} = N(\Delta V) - S \quad (1)$$

$V_{in}$  = unknown voltage

$N$  = digital output

$\Delta V$  = change of the synthesized voltage caused by adding one count to counter

$S$  = digital error,  
 $0 \leq S < \Delta V$

Equation 1 is independent of time because the amplitude of the





synthesized voltage, determined by the states of the counter stages, is independent of time. This means that the frequency of the clock pulses is not critical unless the clock frequency is high enough to affect  $\Delta V$  or the performance of the comparator. It is possible to design this type of converter to be unusually insensitive to clock frequency variations.

The point of particular interest in this design is that the defining equation is independent of time. The relative simplicity of this type of converter is discussed later in this chapter.

Pulse-peak-amplitude converter. The pulse-peak-amplitude converter utilizes the decomposition principle.

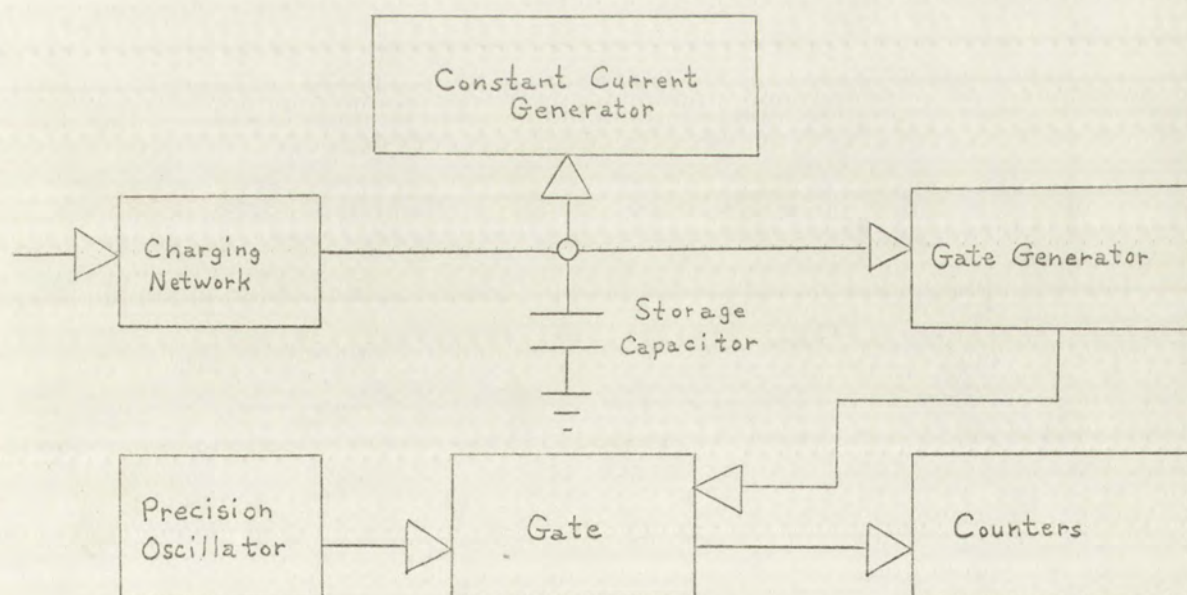


FIGURE 2

BLOCK DIAGRAM -- PULSE-PEAK-AMPLITUDE CONVERTER

AFTER LONGEROT [14]





Referring to Fig. 2, the storage capacitor is caused to be charged to a voltage that is equal to the peak voltage of the unknown input voltage (a pulse). The capacitor is then discharged linearly with respect to time by the constant current generator until the voltage on the storage capacitor is returned to zero volts. The time required to return the capacitor voltage to zero is measured by using a precision clock and counter. Pulses from the clock are gated into the counter only while the capacitor is being discharged. At the end of the discharge period, the counter contains a number that represents the height of the original pulse.

Because of the intermediate time conversion step in the above process, two equations are required to fully describe the input - output relations. The equations are :

$$V_{in} = \left( \frac{i}{C} \right) T \quad (2)$$

describing the time conversion, and

$$N\tau = T - \sigma \quad (3)$$

describing the conversion from time to count, where

$V_{in}$	=	unknown peak voltage
$i$	=	constant discharge current
$C$	=	capacitance, storage capacitor
$T$	=	gate time
$N$	=	digital output
$\tau$	=	precision clock period
$\sigma$	=	digital error





Combining the two equations

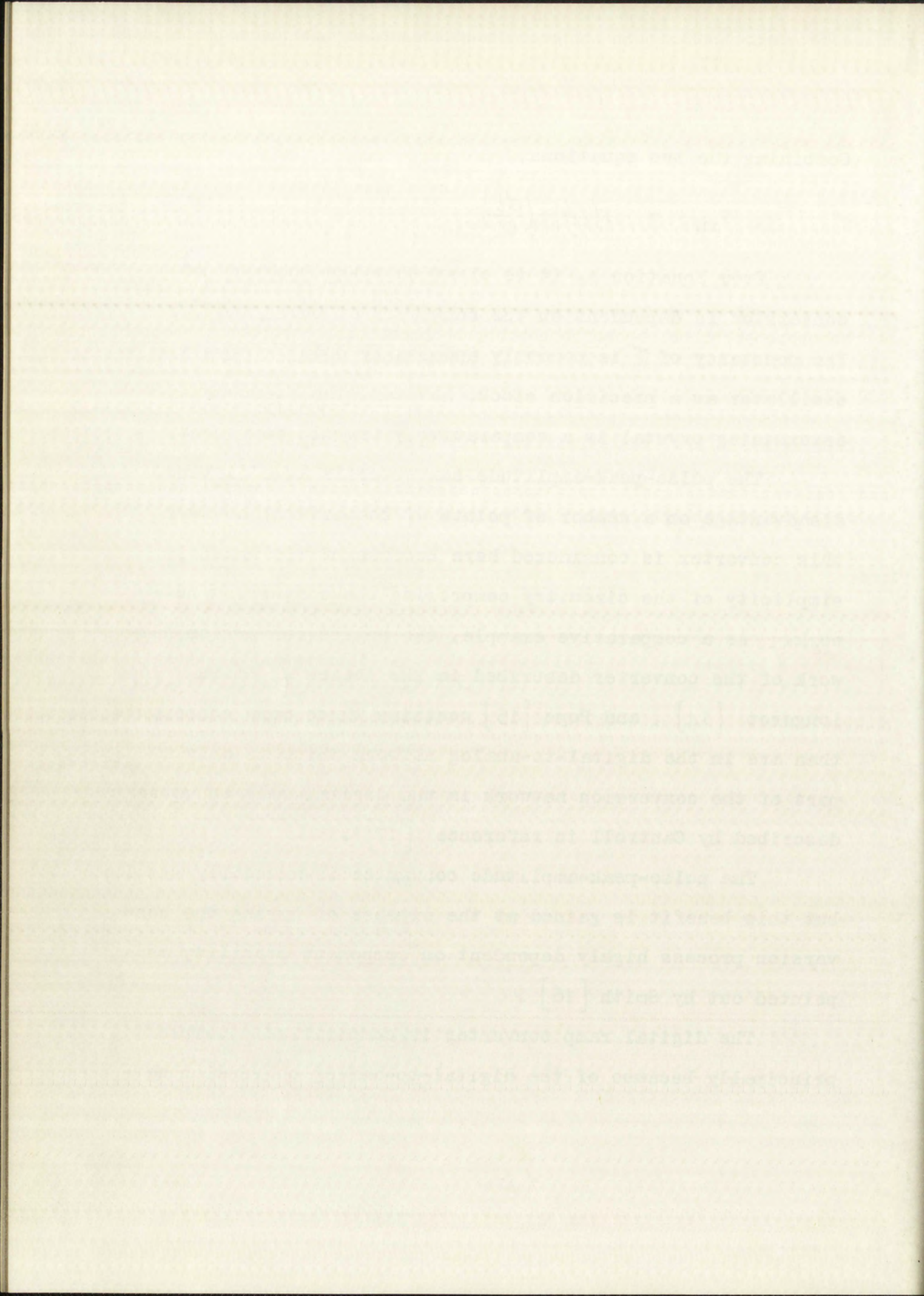
$$V_{in} = N\left(\frac{\tau \dot{L}}{C}\right) + \left(\frac{\sigma \dot{L}}{C}\right) \quad (4)$$

From Equation 4, it is clear that the accuracy of conversion is dependent on the constancy of both  $\dot{L}$  and  $\tau$ . The constancy of  $\tau$  is commonly assured by using a crystal oscillator as a precision clock; however, the frequency determining crystal is a comparatively fragile component.

The pulse-peak-amplitude converter is at a distinct disadvantage on a number of points of comparison; however, this converter is considered here because of the unusual simplicity of the circuitry comprising the conversion network. As a comparative example, the entire conversion network of the converter described in the theses of Smith [16], Longerot [14], and Pope [15] contains three more components than are in the digital-to-analog network which is only a part of the conversion network in the digital ramp converter described by Cantrell in reference [17].

The pulse-peak-amplitude converter is unusually simple, but this benefit is gained at the expense of having the conversion process highly dependent on component stability as pointed out by Smith [16].

The digital ramp converter is comparatively complex, principally because of the digital-to-analog conversion net-





work. However, because of the digital-to-analog network, the conversion process is nearly independent of time considerations and the stability of the conversion process is less dependent on component stability.

### III. DERIVATION OF A NEW APPROACH

From the above considerations, it appeared that a simple converter could result from combining the basic features of the pulse-peak-amplitude converter with the time independent feature of a digital ramp converter.

To explore this possibility, the equations defining the operation of the two types of converters are reconsidered. The operation of the digital ramp converter is defined by Equation 1

$$V_{in} = N(\Delta V) + S \quad (1)$$

and the operation of the pulse-peak-amplitude converter is defined by Equation 4

$$V_{in} = N\left(\frac{\tau \dot{v}}{C}\right) + \frac{\partial \dot{v}}{C} \quad (4)$$

By direct comparison,  $\left(\frac{\tau \dot{v}}{C}\right)$  in Equation 4 corresponds to  $\Delta V$  in Equation 1 ; however,

$$\frac{\tau \dot{v}}{C} = \frac{\Delta Q}{C} \quad (5)$$

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The inference that can be drawn from these relations is that the purpose of the constant current generator is to subtract charge from the storage capacitor and the purpose of the clock is to "mark off" small increments of charge to ultimately indicate the number of increments of charge removed from the storage capacitor during the conversion process.

From the above point of view, the question can be raised, is it necessary to have a two-stage process for removing increments of charge from the charge capacitor? An answer is : not if a more direct way of removing small equal increments of charge from the storage capacitor can be found. Some form of charge impulse generator can be envisioned to impulsively discharge the storage capacitor; however, an ideal charge impulse generator is difficult to realize in practice. One solution, suggested by Guillemin, is to have " ... a little boy toss coulombs at the capacitances ... "[3a] , but this solution cannot be considered practical in the present case. A practical solution is suggested in the relation

$$\Delta Q = \int_{a \rightarrow 0}^a i dt \quad (6)$$

where  $i$  is defined as a pulse of current. The question





arises : would it be possible to pre-measure a small quantity of charge,  $\Delta Q$ , convert the quantity of charge to a current pulse of short duration, and transfer the current pulse to the storage capacitor? The means of transferring the current pulse is available in the form of a grounded-base transistor used in the same way a grounded-base transistor is used for the constant current generator in the pulse-peak-amplitude converter [16] . An obvious way to meter small equal quantities of charge is to charge and discharge a small capacitor under controlled conditions. From the above, it appears reasonable to say that some form of a circuit can be realized that will impulsively discharge a storage capacitor in a way that is defined by

$$V_c = N \left( \frac{\Delta Q}{C} \right) + \Delta v \quad (7)$$

where

$V_c$  = starting voltage on the storage capacitor

$v$  = residual voltage

$$0 \leq \Delta v < \frac{\Delta Q}{C}$$

Equation 7 is independent of time, provided that the impulse of current that constitutes  $\Delta Q$  rises from zero and falls back to zero within each impulse period and that leakage of current from the storage capacitor is non-existent.

The pulse-peak-amplitude converter is designed for the conversion of pulses. To accomplish conversion of d.c. voltages by decomposition, a switch circuit must be devised

The circuit is a simple RC network. The input voltage is applied to the series combination of the resistor and capacitor. The output voltage is taken across the capacitor. The transfer function of the circuit is given by:

$$H(s) = \frac{V_c(s)}{V_i(s)} = \frac{1}{1 + sRC}$$

where  $V_c(s)$  is the Laplace transform of the capacitor voltage,  $V_i(s)$  is the Laplace transform of the input voltage,  $s$  is the complex frequency variable,  $R$  is the resistance, and  $C$  is the capacitance.

The magnitude of the transfer function is given by:

$$|H(s)| = \frac{1}{\sqrt{1 + (sRC)^2}}$$

The phase of the transfer function is given by:

$$\angle H(s) = -\tan^{-1}(sRC)$$

The circuit is a low-pass filter. It passes low-frequency signals and attenuates high-frequency signals. The cutoff frequency of the filter is given by:

$$f_c = \frac{1}{2\pi RC}$$

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to allow the storage capacitor to be charged to the input voltage, then disconnect the input from the storage capacitor so that conversion can be accomplished. A simple switch designed specifically for this application is described in the next chapter.

Basically, the new approach to voltage conversion is to charge a capacitor (the storage capacitor) to the input voltage, disconnect the input voltage and impulsively discharge the storage capacitor by small equal increments of charge until the storage capacitor voltage is returned to zero volts. The number of increments of charge required to return the capacitor voltage to zero are counted in a counter to form the digital value of the input voltage.

Chapter three presents a detailed explanation of the basic theory of this new approach to voltage conversion for the purpose of determining the selection of the best types of circuits to use in implementing this approach in a specific design.





## CHAPTER III

### SYSTEM DESIGN AND CIRCUIT SELECTION

The approach to analog-to-digital voltage conversion is that of charging a capacitor (storage capacitor) to the input voltage, disconnecting the input voltage, and impulsively discharging the capacitor by small equal increments of charge until the voltage on the capacitor is returned to zero. The number of increments of charge required to return the capacitor voltage to zero are counted in a counter to form the digital value of the input voltage.

#### I. AN IDEALIZED ANALOG-TO-DIGITAL CONVERSION NETWORK

The idealized analog-to-digital conversion network shown as a block diagram in Fig. 3 is an idealized implementation of the above approach to conversion. The operation of this idealized conversion network is described because it is functionally identical to the operation of the practical network designed later in this chapter. A clear understanding of the operating characteristics of the idealized network provides a basis for establishing practical circuit requirements.

The following assumptions are necessary regarding the elements of Fig. 3. The block labeled "zero detector" rep-

The approach to analog-to-digital voltage conversion

is that of converting a continuous (analog) voltage to the

digital voltage, determined by the input voltage, and representing

the difference between the input and the digital voltage.

The digital voltage on the output is referred to

as the output voltage. The number of steps required to convert

the input voltage to zero is referred to as the resolution.

The digital value of the input voltage

## 11.1 ANALOG-TO-DIGITAL

### CONVERSION SYSTEMS

The idealized analog-to-digital conversion system

shown in Fig. 11.1 is an idealized representation

of the above approach to conversion. The operation of

this idealized conversion system is described in terms of

the operation of the practical network

with detailed later in this chapter. A clear understanding

of the operating characteristics of the idealized network

provides a basis for establishing practical requirements

The following assumptions are necessary regarding the

elements of Fig. 11.1. The block labeled "analog input" represents



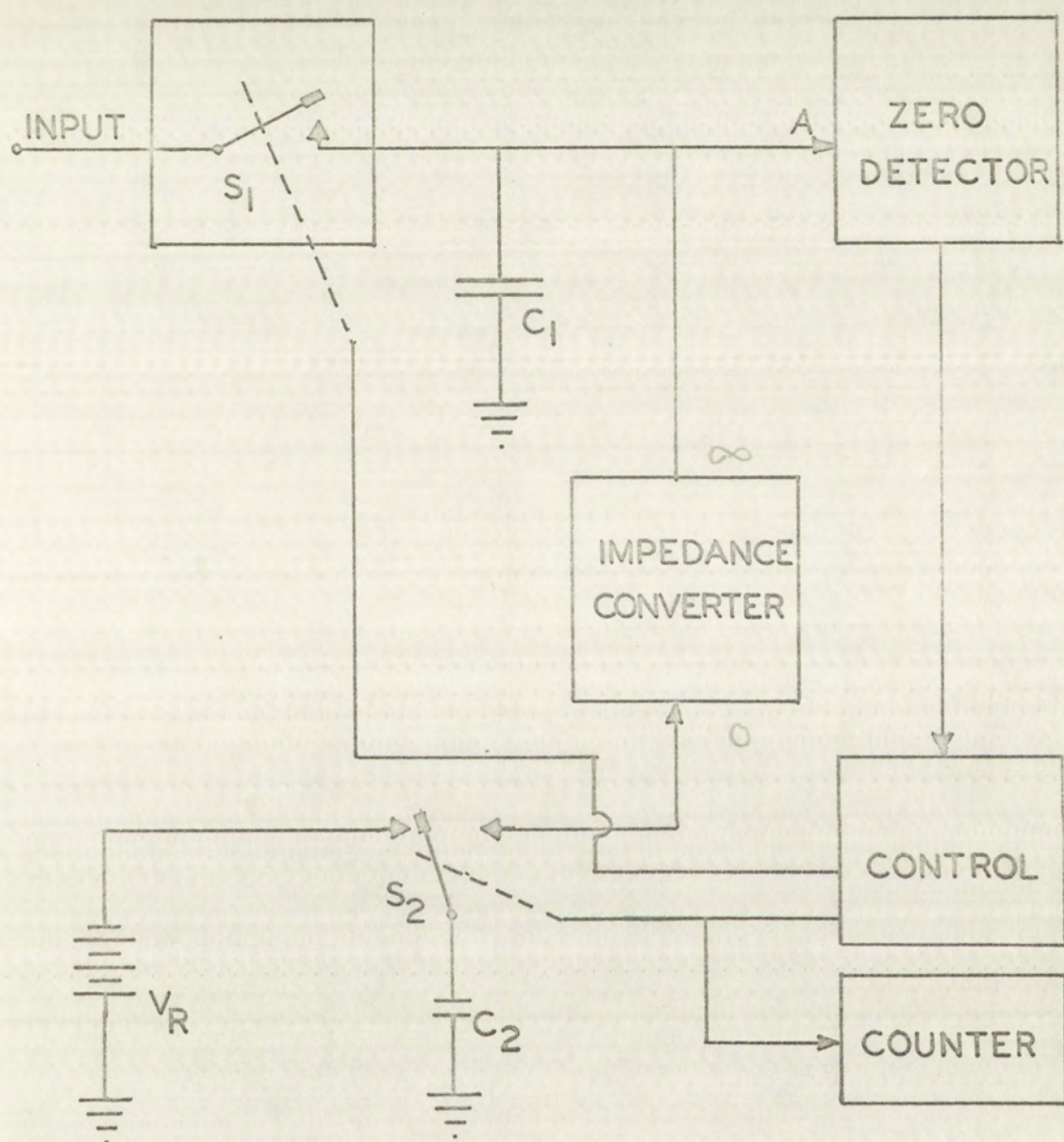


FIGURE 3

AN EXPLANATORY DIAGRAM OF AN IDEALIZED  
ANALOG-TO-DIGITAL CONVERSION NETWORK



AN EXPLANATION  
OF THE  
ANALOG-TO-DIGITAL



resents an ideal voltage comparator, i.e., no current is drawn at the input terminal, marked "A", and a pulse only appears at the output when the input voltage is equal to, or less than, the reference voltage, which is zero volts. The block labeled "impedance converter" represents an amplifier with zero input impedance, infinite output impedance, and a current gain exactly equal to unity for all frequencies. The block labeled "control" represents circuits that control the operation of ideal switches  $S_1$  and  $S_2$  in proper sequence. The block labeled "counter" represents circuits that count the number of times that switch  $S_2$  operates during a given conversion cycle.  $C_1$ , the storage capacitor, is assumed ideal as is  $C_2$ , the metering capacitor.

A conversion cycle consists of two time intervals. During the first interval, the charge interval,  $S_1$  is closed so that  $C_1$  is charged to the input voltage. The remainder of the circuit is quiescent during this interval. During the second time interval, the discharge interval,  $S_1$  is open and the remainder of the circuit is actively engaged in the conversion process. The following description of the conversion process is assumed to start at the end of the charge interval and it is further assumed that the counter contains the number "zero".

When the control circuit causes  $S_1$  to open, the storage capacitor is charged to a voltage,  $V_{in}$ , equal to the input voltage present at the instant  $S_1$  opens.  $V_{in}$  is assumed large





enough to allow the action to be described.

The quantity of charge,  $Q_c$ , retained on  $C_1$  is given by

$$Q_c = C_1 V_{in} \quad (8)$$

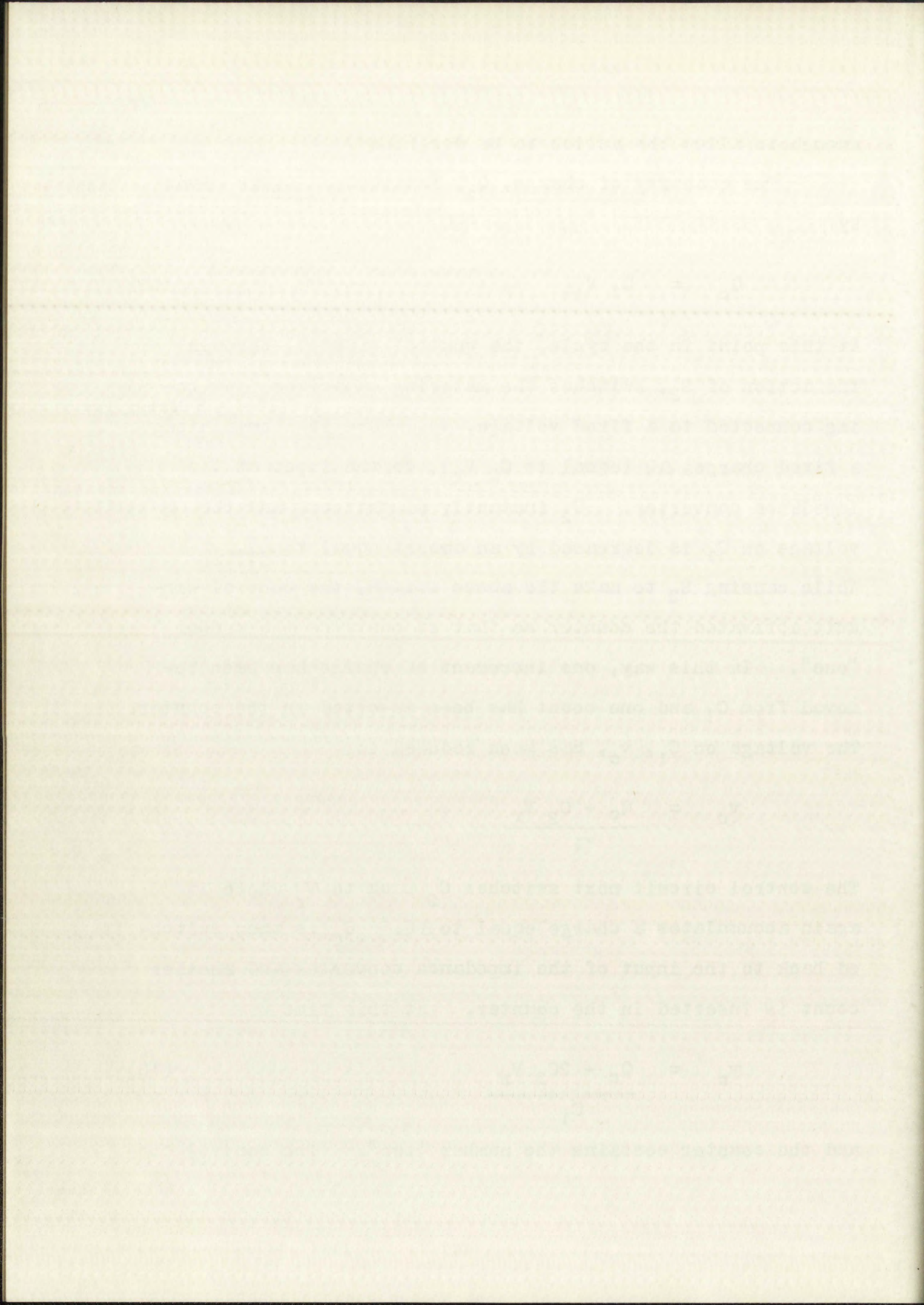
At this point in the cycle, the control circuit, through the action of  $S_2$ , switches the metering capacitor from being connected to a fixed voltage,  $V_r$ , where it accumulated a fixed charge,  $\Delta Q$  (equal to  $C_2 V_r$ ), to the input of the impedance converter.  $C_2$  instantly discharges, and the voltage on  $C_1$  is decreased by an amount equal to  $\frac{\Delta Q}{C_1}$ . While causing  $S_2$  to make the above switch, the control circuit activated the counter so that it contains the number "one". In this way, one increment of charge has been removed from  $C_1$  and one count has been inserted in the counter. The voltage on  $C_1$ ,  $v_c$ , has been reduced to

$$v_c = \frac{Q_c - C_2 V_r}{C_1} \quad (9)$$

The control circuit next switches  $C_2$  back to  $V_r$  where it again accumulates a charge equal to  $\Delta Q$ .  $C_2$  is then switched back to the input of the impedance converter and another count is inserted in the counter. At this time

$$v_c = \frac{Q_c - 2C_2 V_r}{C_1} \quad (10)$$

and the counter contains the number "two". The control cir-





cuit continues to switch  $C_2$  from reference voltage to the impedance converter and back again until the zero detector puts out a pulse indicating that  $C_1$  has been discharged. At this point the control circuit stops the switching action, terminating the discharge interval, and the counter contains a number that is representative of the voltage,  $V_{in}$ . Switch  $S_1$  is caused to close, starting the charge interval, and the conversion cycle will be complete when the counter is reset to zero.

The illustration above presumes ideal circuitry that is not attainable in practice. A discussion of practical circuitry follows the development of a mathematical model of the technique.

## II. THE MATHEMATICAL MODEL

The voltage on any charged capacitor may be expressed as

$$V_c = \frac{Q_T}{C} = \frac{n\Delta Q + S}{C} \quad (11)$$

where

$V_c$	=	voltage on the capacitor
$Q_T$	=	total charge on the capacitor
$C$	=	capacitance of the capacitor
$n$	=	an integer
$\Delta Q$	=	increment of charge
$S$	=	charge, $0 \leq S < \Delta Q$





If  $\Delta Q$  is presumed constant for all values of  $V_c$ , each value of  $V_c$  is associated with a unique value of  $n$ .<sup>\*</sup> The variable  $n$  may be defined as a digital representation of  $V_c$ .

Just as any voltage may, within specific accuracy limits, be synthesized by accumulating equal increments of charge on a capacitor, a voltage may be decomposed through the removal of equal increments of charge from a capacitor that is initially charged to that voltage.

A relation that is more significant to the technique under discussion is

$$V_c = \frac{N\Delta Q - \epsilon}{C} \quad (12)$$

$$N = n+1$$

$$\epsilon = \Delta Q - \delta, \quad 0 \leq \epsilon < \Delta Q$$

It is apparent that  $\frac{N\Delta Q}{C} > V_c$ . This defines  $N$  as being the smallest integer that can multiply  $\frac{\Delta Q}{C}$ , the product exceeding  $V_c$ . The conversion approach is to perform incremental charge subtraction until the voltage on the capacitor is reduced to less than zero, hence the number of increments required will be  $N$ , not  $n$ .

---

<sup>\*</sup>The converse is not true in that a given value of  $n$  may be associated with an infinite number of  $V_c$ 's within an interval of voltage equal to  $\Delta Q/C$ .

the voltage  $V$  may be defined as a ratio, represented

by the ratio  $V = \frac{E}{R}$ , where  $E$  is the voltage and  $R$  is the resistance.

Thus, the resistance of a component is equal to the ratio of the

voltage across it to the current through it.

The ratio of the voltage across a component to the current through it

is called the resistance of that component.

A relation that is more significant to the technician

is the relation

$$R = \frac{V}{I}$$

where  $R$  is the resistance,  $V$  is the voltage, and  $I$  is the current.

It is evident that  $R = \frac{V}{I}$ . This defines  $R$  as being

the voltage across the component divided by the current through it.

exceeding  $V$ . The conversion approach is to perform factor-

mental change subtraction until the voltage on the capacitor

is reduced to less than zero, hence the number of increments

required will be  $N$ , not  $n$ .

The converse is not true in that a given value of  $n$

may be associated with an infinite number of  $V$  values but

interval of voltage equal to  $2V_0$ .



Until now, no time dependence has been expressed or implied in this development; however, if leakage occurs at the storage capacitor, a quantity of charge given by

$$Q_L = \int T_d i_L dt \quad (13)$$

where

$$\begin{aligned} Q_L &= \text{charge gain (or loss)} \\ &\quad \text{due to leakage} \\ i_L &= \text{leakage current} \\ T_d &= \text{discharge time interval} \end{aligned}$$

alters Equation 12 to the form

$$V_C = \frac{N \Delta Q + Q_L - \epsilon}{C} \quad (14)$$

Because of the time dependence of  $Q_L$ ,  $N$  can no longer be unequivocally defined as an accurate digital representation of  $V_C$ . To realize maximum application of this technique  $i_L$ ,  $T_d$ , or both must be minimized. The approach used here is to minimize  $i_L$  since the relatively free choice of  $T_d$  is one of the advantages of this technique.

Examining Equation 14 further, it can be written as a sum of voltages or

$$V_C = \frac{N \Delta Q}{C} + \frac{Q_L}{C} - \frac{\epsilon}{C} \quad (15)$$





Equation 15 states that the voltage on the capacitor is equal to  $N$  times the voltage resolution (or voltage represented by one count), plus a voltage due to leakage, plus a small term representing the amount the last count carried the capacitor voltage below zero. If the leakage current is constant under all conditions of operation and the rate of discharge pulsing is constant, then  $Q_L$  can be written as  $Q_L = N i_L \tau$ , where  $\tau$  equals the time between discharge pulses. Equation 15 then becomes

$$V_c = \frac{N(\Delta Q + i_L \tau)}{C} - \frac{e}{C} \quad (16)$$

and, within the specified conditions, the leakage term effectively vanishes.

Examining the conditions leading to the cancellation of leakage effects, it is quite unreasonable to expect any leakage associated with the charge on the capacitor to be a constant under all conditions of operation, particularly varying temperature. Further, one of the advantages associated with the conversion technique is that precise frequency control is not necessary, provided that  $Q_L$  is kept quite small. For the purpose of this chapter, it is arbitrarily stipulated that  $Q_L$  should be less than  $\Delta Q$ , if leakage effects are to be negligible. The significance of leakage effects can be expressed by the ratio  $Q_L / \Delta Q$ . More realistic limits are considered in chapter four.





Resolution versus accuracy. In Equation 15 the voltage resolution attributable to this technique is equal to  $\Delta Q/C$ . The voltage resolution of the system can be decreased by either decreasing  $\Delta Q$  or increasing  $C$ . If the discharge pulse rate is fixed, any decrease in voltage resolution is accompanied by an increase in the discharge time interval for a given input voltage. This in turn causes an increase in  $Q_L$  in direct proportion to the increase in the discharge time interval. If resolution is improved by decreasing  $\Delta Q$ , the term  $\Delta Q/C$  decreases while the term  $Q_L/C$  increases in inverse proportion to the change in  $\Delta Q$ . Since the accuracy of the system can be related to the ratio  $Q_L/\Delta Q$ , it is seen that leakage effects can readily limit the resolution attainable by decreasing  $\Delta Q$ , the ratio rising as the inverse square of the ratio of voltage resolutions. If resolution is decreased by increasing  $C$ , then  $\Delta Q/C$  decreases, whereas, for reasons already related,  $Q_L/C$  remains constant. The ratio  $Q_L/\Delta Q$  then rises only as the direct inverse of the ratio of the voltage resolutions. Stated another way, if an attempt is made to decrease the resolved voltage by a factor of 5 through decreasing  $\Delta Q$ , the ratio  $Q_L/\Delta Q$  will increase by a factor of 25. If the same change in resolution is effected by increasing  $C$ , the ratio  $Q_L/\Delta Q$  will increase by a factor of 5. Although it appears obvious that increases in resolution should be effected through increases in  $C$ , other considerations, such as the time required to charge  $C$ , may prove important in a particular design.





The choices to be made may depend on other design requirements, but obviously it is most desirable to increase C if possible.

Assuming leakage is negligible, the linearity attainable by this technique is dependent on the constancy of  $\Delta Q$  through the discharge interval. The accuracy of the conversion will be determined by the accuracy of the setting of  $\Delta Q$ .

### III. PRACTICAL CIRCUIT CONSIDERATIONS

The importance of minimizing leakage has been stressed. The following section examines some of the ways of charging, discharging, and detecting zero with particular reference to leakage.

Methods of charging. Charging can be accomplished through a diode or a transistor.

When a diode is used as a charging device, all the charging current must come from the voltage source. A diode is not bilateral and does not have zero forward impedance, hence the voltage on the capacitor will be slightly less than the highest input voltage if the diode is used without supplementary circuitry. As shown in Fig. 4 on page 29, there is no way to prevent the input voltage from interfering with the discharge process. Unless additional circuitry is included to prevent this interference, the use of a diode is restricted to applications featuring controlled pulse inputs. The reverse impedance of a diode is high but finite. Reverse leakage on the order of  $10^{-9}$  amperes is attainable at room temperature but doubles with every  $6^{\circ}\text{C}$  increase in junction temperature [ 5a ]. Diode

The choice to be made may depend on other design requirements. It is most desirable to include both possibilities.

According to the above, the structure of the device is determined by the requirements of the circuit. The structure of the circuit is determined by the requirements of the device.

The importance of maintaining the temperature of the device is emphasized. The following section contains some of the data of the device. The following section contains some of the data of the device.

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leakage is composed of junction leakage and surface leakage. The junction leakage is essentially independent of voltages but dependent on temperature. Surface leakage is essentially ohmic in nature and is relatively constant with temperature [5a] .

The application of a transistor to charging is shown in Fig. 5. The same considerations given the diode as a charging device apply to the use of a transistor with the exception that most of the charging current comes from the collector supply. This results in an apparent decrease in diode impedance and less loading of the voltage source. The time required to charge a given capacitor is considerably reduced [10] . Leakage considerations are essentially the same as for the diode except that there are relatively few transistors that exhibit good diode reverse bias characteristics at voltages greater than five volts.\*

The circuit of Fig. 6 on page 30 incorporates a switching capability. During the charge interval, the combination of  $Q_1$ ,  $Q_2$ ,  $R_1$ , and  $R_2$  constitutes a feedback amplifier having a high input impedance and low output impedance.

During the discharge interval, the lower end of  $R_2$  is switched from -6 volts to 0 volts so that  $Q_2$  is saturated, causing  $D_1$  to be back-biased and the emitter-base diode of  $Q_1$  to be back-biased. In this way, the input is disconnected

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\*Determined from a thorough search of a tabulation [18] .





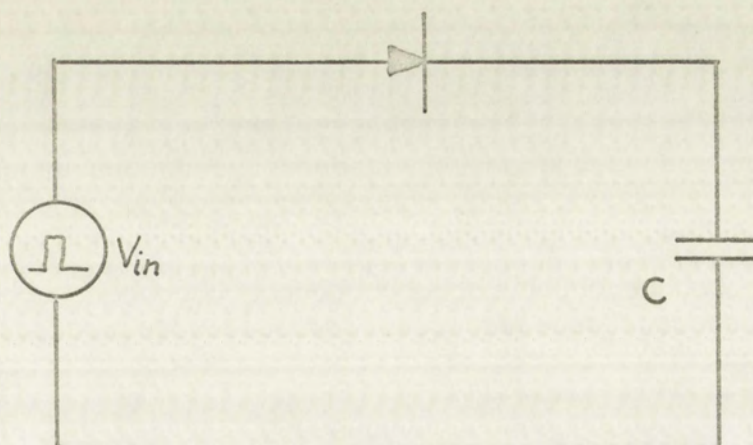


FIGURE 4  
A DIODE USED AS A CHARGING DEVICE

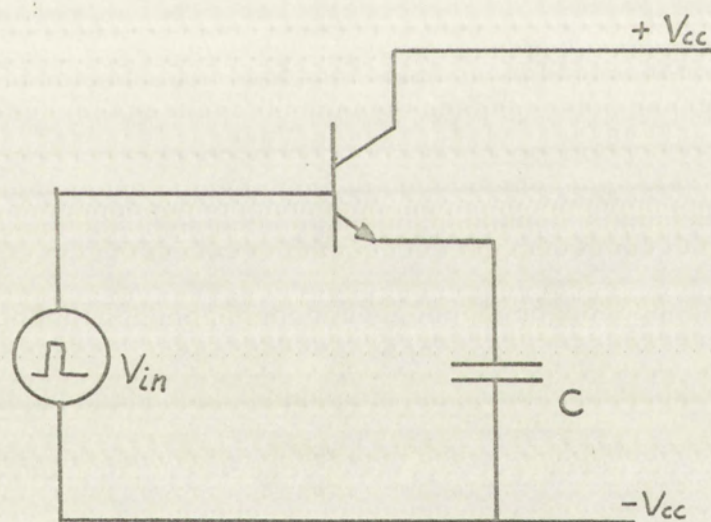


FIGURE 5  
A TRANSISTOR USED AS A CHARGING DEVICE



FIGURE 4  
A DIODE USED AS A CHARGING DEVICE



FIGURE 5  
A TRANSISTOR USED AS A CHARGING DEVICE



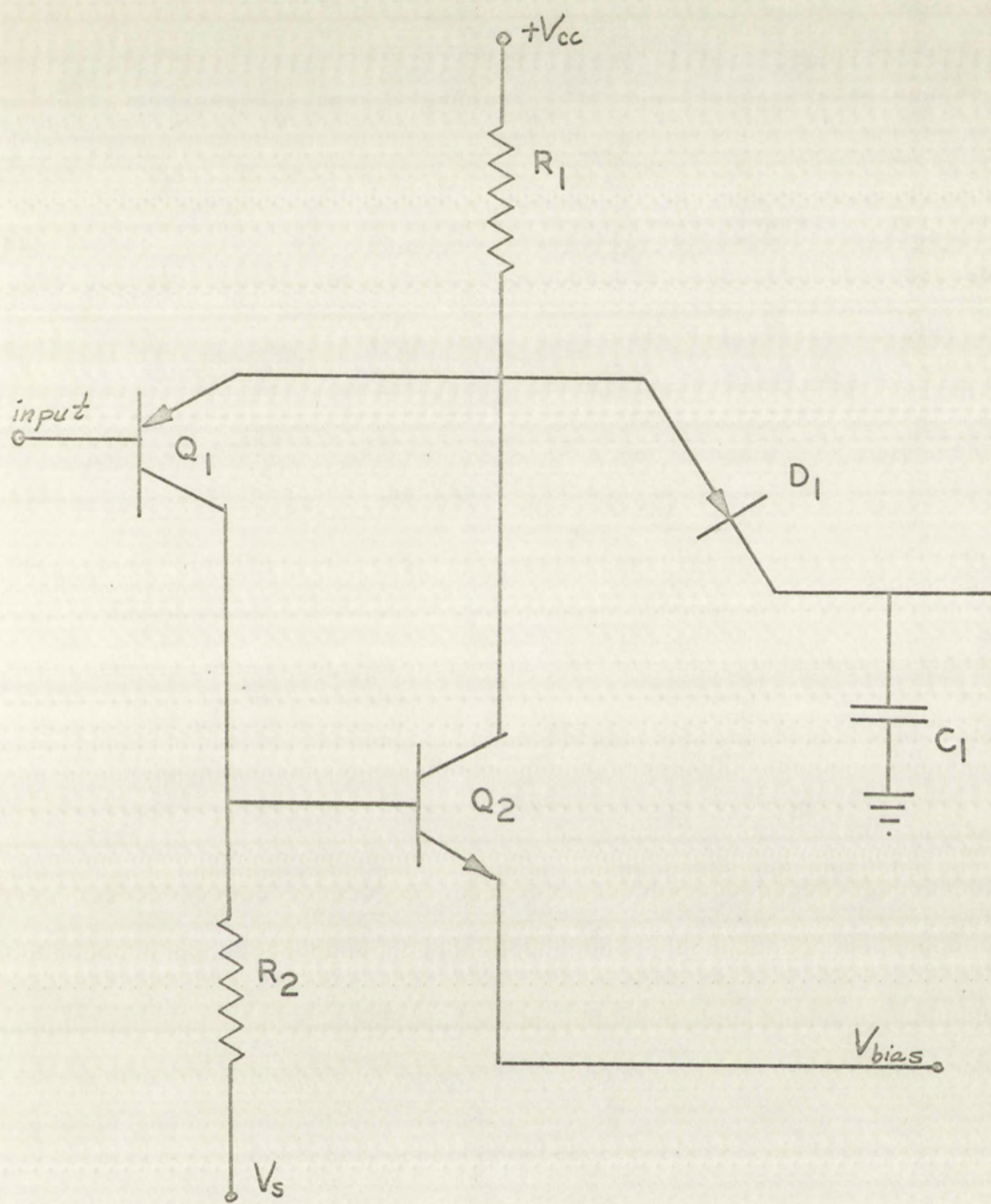


FIGURE 6  
INPUT NETWORK



FIGURE 1  
DIFFERENTIAL AMPLIFIER



from the storage capacitor, and the input terminal presents a relatively high impedance to the signal source.

The circuit of Fig. 6 is incorporated in the model conversion network that is designed in the next chapter.

Methods of discharging. The requirements to be met by the discharge circuit are :

1. The circuit must be capable of generating and transmitting an approximation of an impulse of discharge current to the storage capacitor.
2. The discharge circuit must generate or transmit equal increments of charge without variation due to voltage changes on the capacitor.
3. The circuit must not contribute to leakage from the capacitor.

As mentioned in the previous chapter, a grounded-base transistor can be used to transmit a current pulse to the storage capacitor. The required current pulse can be generated by discharging a small metering capacitor, previously charged to a precise voltage, through the emitter of the grounded-base transistor. One possible circuit for doing this is shown in Fig. 7.

The metering capacitor is shown to be driven by a free-running multivibrator [2a]. The functional requirement is

The circuit of Fig. 2 is identical to the circuit

shown in Fig. 1, except that the capacitor is connected

to the output of the amplifier instead of to the input.

The circuit of Fig. 3 is identical to the circuit

shown in Fig. 2, except that the capacitor is connected

to the input of the amplifier instead of to the output.

The circuit of Fig. 4 is identical to the circuit

shown in Fig. 3, except that the capacitor is connected

to the input of the amplifier instead of to the output.

The circuit of Fig. 5 is identical to the circuit

shown in Fig. 4, except that the capacitor is connected

to the input of the amplifier instead of to the output.

The circuit of Fig. 6 is identical to the circuit

shown in Fig. 5, except that the capacitor is connected

to the input of the amplifier instead of to the output.

The circuit of Fig. 7 is identical to the circuit

shown in Fig. 6, except that the capacitor is connected

to the input of the amplifier instead of to the output.

The circuit of Fig. 8 is identical to the circuit

shown in Fig. 7, except that the capacitor is connected

to the input of the amplifier instead of to the output.



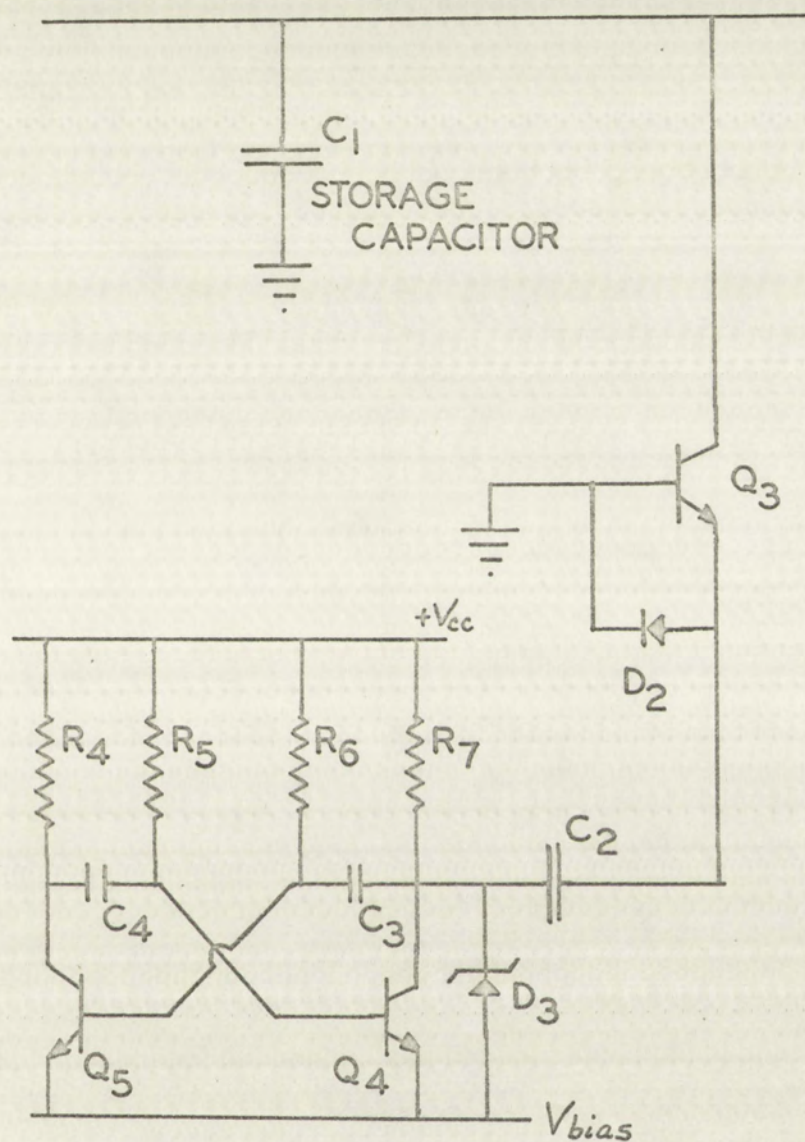


FIGURE 7  
DISCHARGE GENERATOR





for the metering capacitor to be driven by a rectangular pulse generator. Besides the multivibrator, a blocking oscillator [ 2b ] [ 6a ] [ 11 ] [ 13 ], a Base-Emitter class C oscillator [ 20 ], or a complementary multivibrator may be used. Of these, the Base-Emitter class C oscillator has the best frequency stability and the blocking oscillator is the simplest.

Diode  $D_2$  conducts during the second half of the multivibrator cycle, allowing  $C_2$  to recharge after having discharged through the emitter-base diode of  $Q_3$ . Diode  $D_3$  is a breakdown diode (Zener diode) that acts as the regulator of  $V_R$ .

Zero detector. The requirements to be met by the zero detector are :

1. The zero detector must not contribute to leakage from the storage capacitor.
2. The zero detector should contain few components.
3. The zero detector should be sensitive and stable.

Numerous circuits can be used to meet the above requirements to some degree. A few of the possible circuits are the Schmitt trigger and the Multiar [ 6b ], a complementary monostable multivibrator [ 4 ], and a gated d.c. amplifier type of comparator [ 12 ]. The basic principle of most of the types best suited to this application is that they are regenerative circuits that regenerate at very low input currents. The

the circuit is designed to be used as a detector of the presence of a signal in a noisy environment.

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simplest of all known circuits meeting this description is the blocking oscillator connected as shown in Fig. 8.

The input to the zero detector shown in Fig. 8 is a back-biased transistor base junction. An earlier discussion applies here. The simplicity of this zero detector is self-evident. The stability and sensitivity are determined by the two choices of components and are discussed further in chapter four.

Control circuit. The requirements to be met by the control circuit are :

1. The control circuit must control the input switch and discharge generator.
2. The conversion interval must be started on receipt of an externally supplied pulse.
3. The conversion interval must stop when the zero detector pulses.

Nearly any flip-flop type of circuit can meet the above requirements. The flip-flop that is the most "off" when turned off is the simple complementary flip-flop shown in Fig. 9.

Additional circuitry. The complete conversion network is shown in Fig. 10 on page 36. Although the preceding circuits perform all of the required functions, a

the input to the wave detector shown in Fig. 2 is the

most desired frequency band.

...

The stability and sensitivity are determined by

the two phases of components and are discussed further in

Chapter Four.

Control elements. The requirements to be met by the

control elements are:

1. The control element must control the input

...

...

2. The conversion interval must be started on

...

3. The conversion interval must stop when the

...

...

Nearly any flip-flop type of circuit can meet the above

requirements. The flip-flop that is the most "all" when this

of all is the simple complementary flip-flop shown in Fig. 3.

...

Additional elements. The complete conversion set-

...

...

...

...



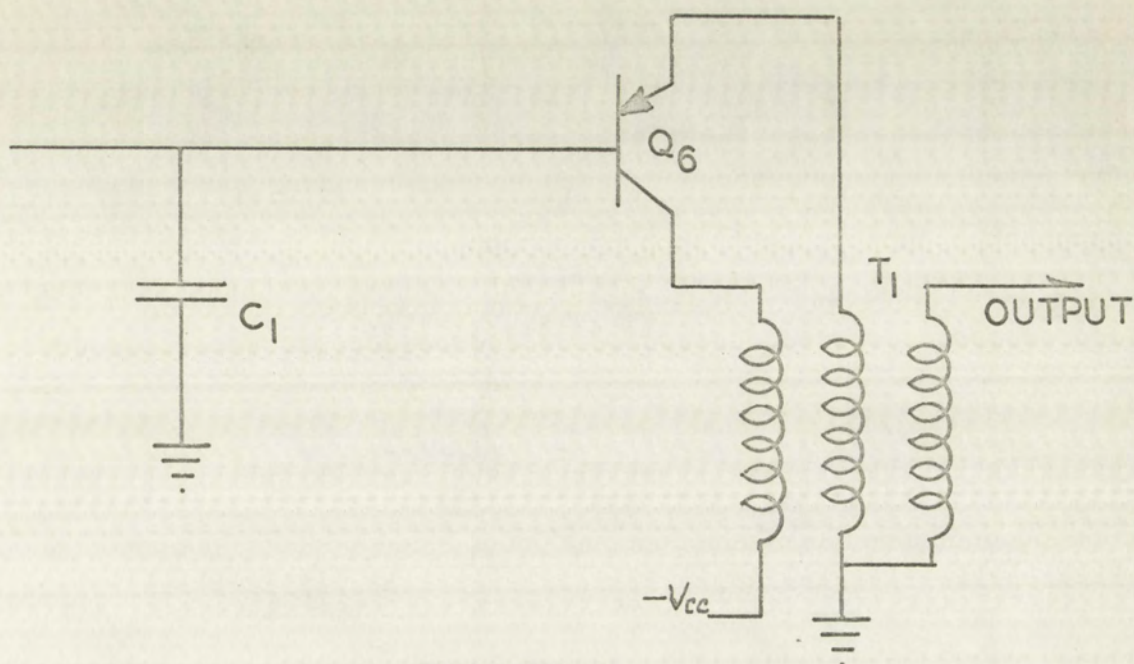


FIGURE 8  
ZERO DETECTOR

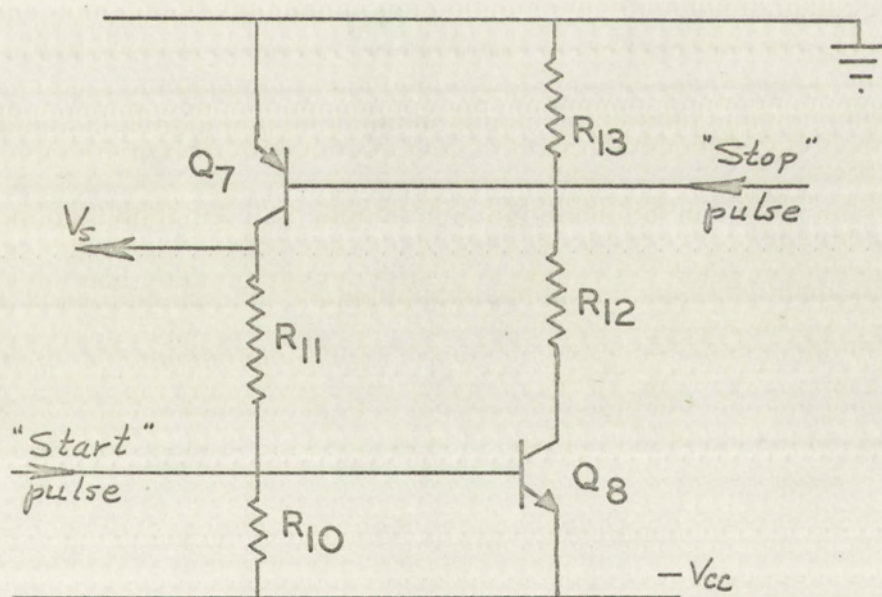


FIGURE 9  
CONTROL FLIP-FLOP CIRCUIT



FIGURE 8  
ZERO DETECTOR



FIGURE 9  
CONTROL FLIP-FLOP CIRCUIT



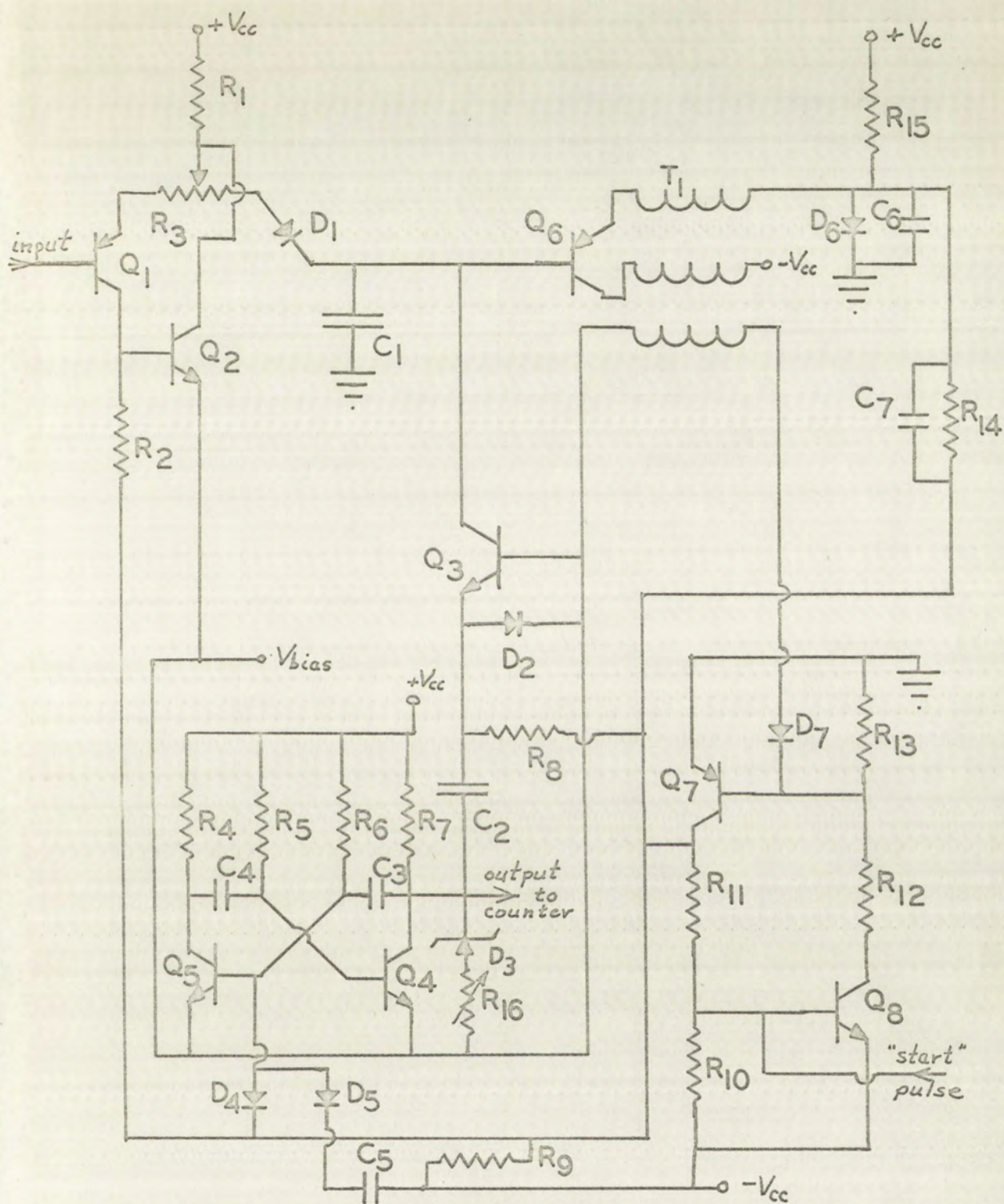


FIGURE 10  
CONVERSION NETWORK

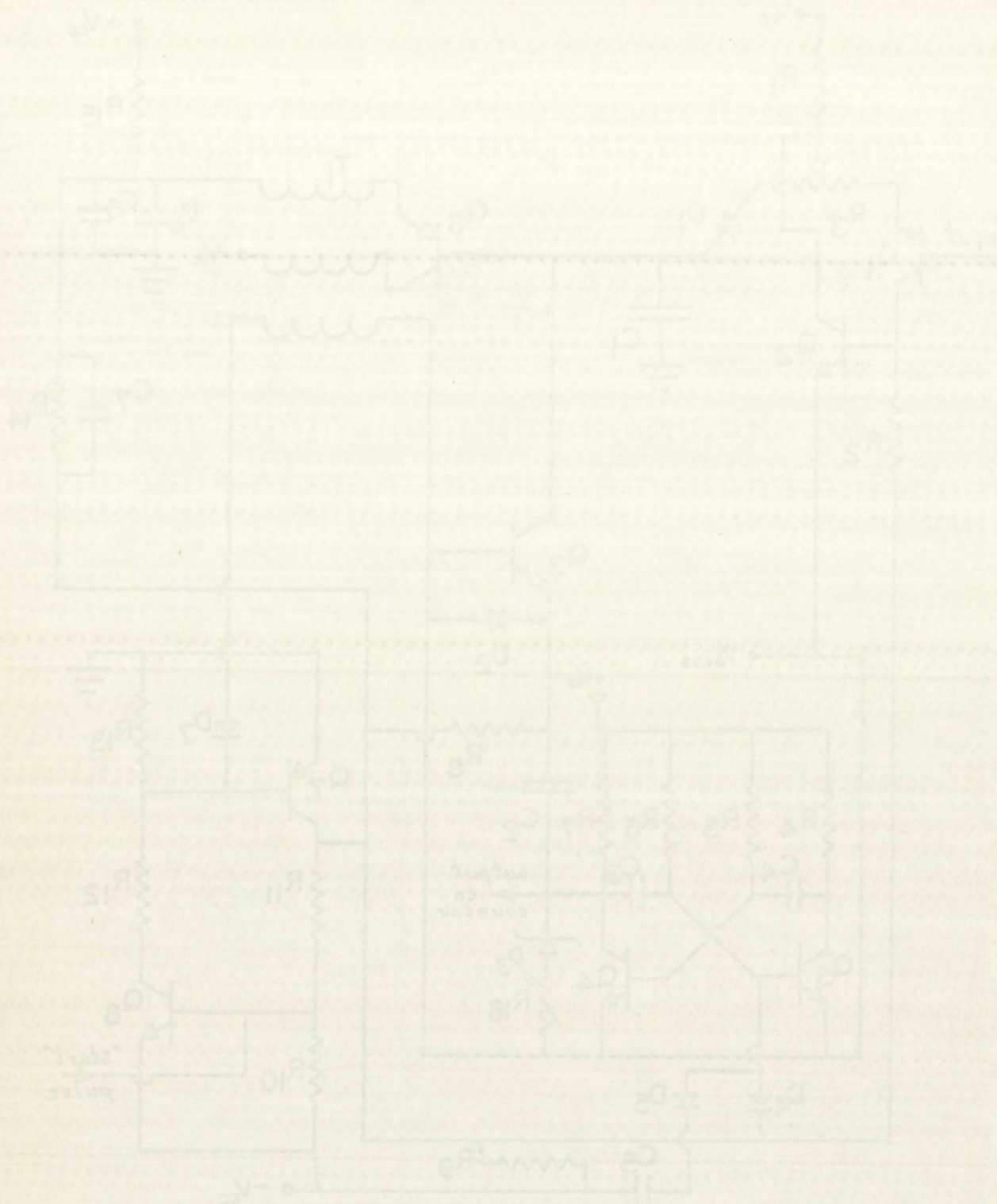


FIGURE 10  
CONVERSION NETWORK



few minor additions are shown in Fig. 10 to either improve the performance of the network or aid in testing the network. These additions are as follows :

$R_8$  is connected as shown so that the grounded-base impedance converter will act as a constant current generator during the charge interval. This is done to keep a forward bias current flowing through  $D_1$  to reduce the time required to fully charge  $C_1$ . In addition, this bias current allows the voltage on  $C_1$  to decrease if the input voltage decreases during the charge interval.

The combination  $D_5$ ,  $R_9$ , and  $C_5$  is added to delay the start of the conversion process so that leakage can be evaluated. This is discussed further in the chapter on testing.

A diode,  $D_7$ , is added between the zero detector and the control circuit to prevent the backswing of the zero detector output from resetting the control flip-flop.

The potentiometer,  $R_3$ , is added to allow "zero" adjustment. The variable resistance,  $R_{16}$ , is added to allow fine adjustment of  $\Delta Q$ .

Summary. The input switch circuit provides the necessary switching functions and, in addition, affords light loading of the signal source and "zero" adjustment.

The discharge generator is selected to provide a simple means of discharging the storage capacitor in the required manner with the added feature of having enough flexibility to

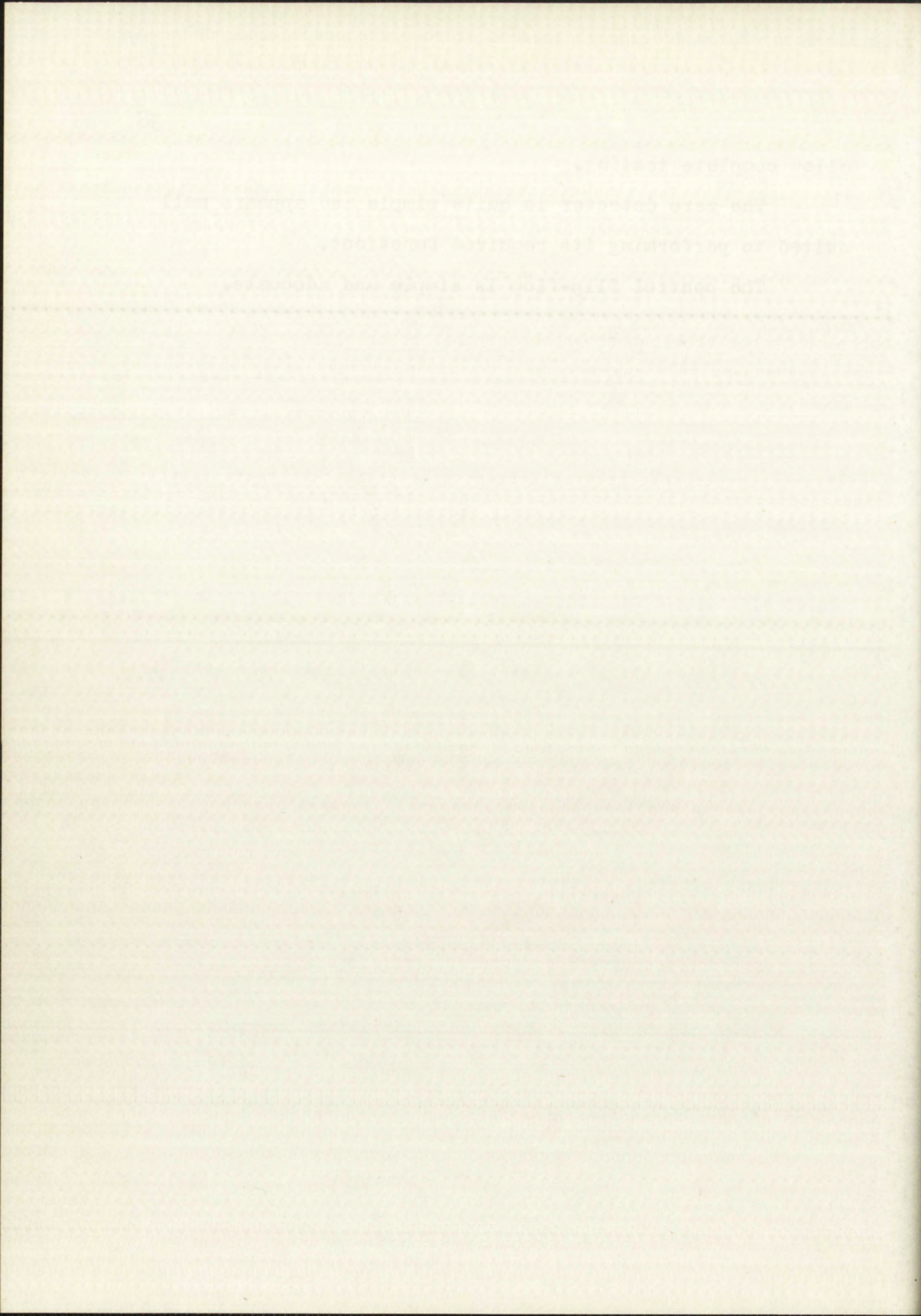




allow complete testing.

The zero detector is quite simple and appears well suited to performing its required functions.

The control flip-flop is simple and adequate.





## CHAPTER IV

### CIRCUIT DESIGN FOR A MODEL CONVERSION NETWORK

The purpose of this chapter is to present the derivation of component values to be used in a model analog-to-digital conversion network. The design considerations are concentrated on questions of accuracy and stability. Estimates and approximations are used when exact design information is not available. The model is described.

#### I. GENERAL ASSUMPTIONS AND SELECTIONS

The following are the initial assumptions and selections affecting the over-all network design.

$+V_{cc}$	=	+6.0 volts
$-V_{cc}$	=	-6.0 volts
$V_{bias}$	=	-3.0 volts
$V_s$	=	-5.0 volts (charging)
		-0.5 volts (discharging)

All transistors must be planar silicon surface passivated types for low leakage and high stability [19]. All signal diodes must be low leakage types. Commercial components will be used throughout.

The clock frequency will be 0.5 megacycles per second.

## CIRCUIT DESIGN FOR A MODEL

### CONVERTING NETWORK

The purpose of this chapter is to present the design of a component which is to be used in a model. The design considerations are concentrated on questions of accuracy and stability. The design considerations are used when exact design information is not available. The model is described.

### 1. GENERAL ASSUMPTIONS AND DEFINITIONS

The following are the initial assumptions and definitions affecting the over-all network design.

- $V_{CC} = +5.0$  volts
- $V_{EE} = -5.0$  volts
- $V_{bias} = -5.0$  volts
- $V_{in} = -5.0$  volts (charging)
- $V_{out} = -0.5$  volts (discharging)

All transistors must be planar silicon surface passivated types for low leakage and high stability. All signal diodes must be low leakage types. Constant current sources will be used throughout.

The clock frequency will be 0.5 megacycles per second.



The voltage resolution will be three millivolts per count.  
Full scale output will be 999 counts.

## II. THE INPUT CIRCUIT

The complete input circuit is shown in Fig. 11.  
The combination  $Q_1$ ,  $Q_2$ ,  $R_1$ , and  $R_2$  is a feedback amplifier that tends to stabilize the collector current of  $Q_1$ . The emitter current of  $Q_1$  should be approximately the same as the constant current drawn through  $D_1$  so that the voltage rise from the input terminal to the emitter of  $Q_1$  is approximately matched by the voltage drop across  $D_1$ . The emitter current and constant current are selected to be 0.15 ma. If  $Q_1$  is assumed to have an  $H_{FE}$  of 15 at  $I_C = 0.15$  ma., the current through the input terminal is  $0.15/15 = 0.01$  ma.  $Q_1$  is a PNP transistor and was previously specified to be a planar silicon surface passivated unit.  $Q_1$  is chosen to be a 2N869.

The collector current of  $Q_1$  is approximately  $0.15 - 0.01 = 0.14$  ma. If  $Q_2$  is assumed to draw 0.04 ma. and the voltage drop across  $R_2$  is 2.7 volts (approximating  $V_{eb}$  of  $Q_2$  at 0.7 volts), then

$$R_2 = \frac{2.7}{0.14 - 0.04} = 27 \text{ k}\Omega$$

The current through  $R_1$  must split between the constant current (0.15 ma.), the emitter current of  $Q_1$  (0.15 ma.), and

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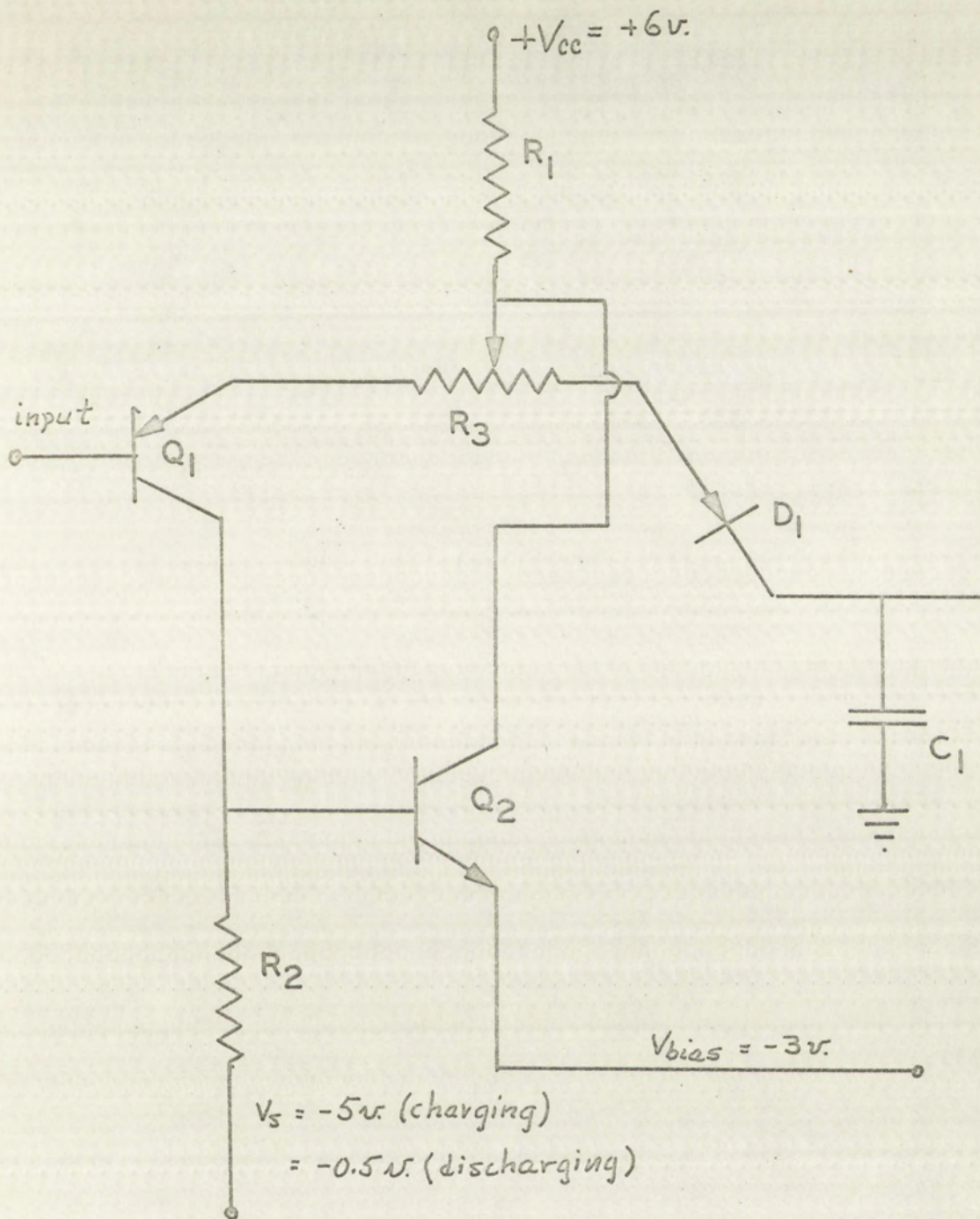
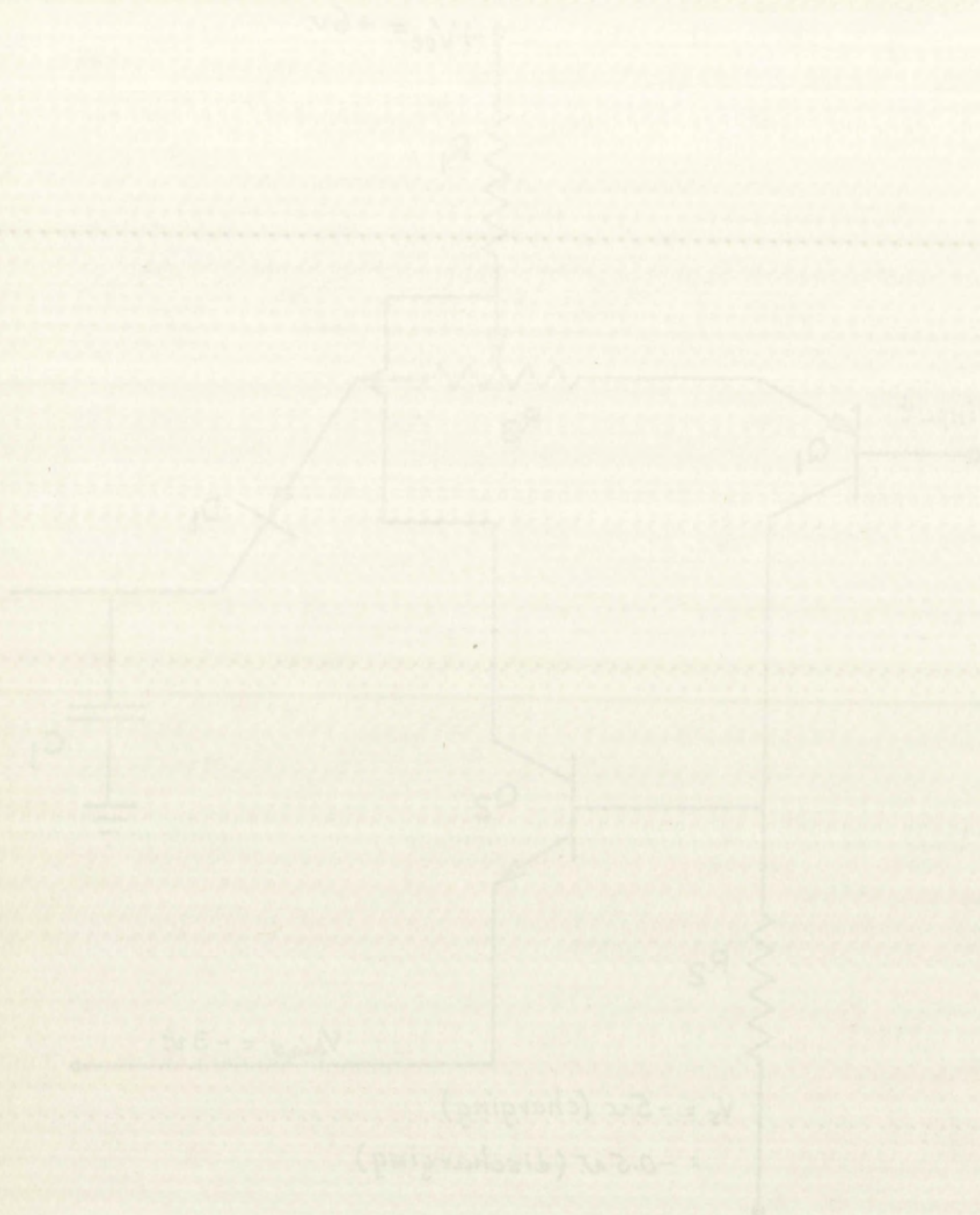


FIGURE II  
COMPLETE INPUT NETWORK



COMPLETE INPUT NETWORK



the collector current of  $Q_2$ . The current available for the collector of  $Q_2$  is minimum when the input voltage is highest. If the minimum collector current in  $Q_2$  is specified as 0.20 ma., minimum current through  $R_2$  is  $0.15 + 0.15 + 0.20 = 0.50$  ma. Full scale output is 999 counts so full scale input is 3.0 volts. Assuming  $V_{eb}$  of  $Q_1$  is 0.7 volts and neglecting the drop across the zero adjust potentiometer, the minimum voltage drop across  $R_1$  is  $6.0 - (3.0 + 0.7) = 2.3$  volts. Therefore,

$$R_1 = \frac{2.3}{0.5} \approx 4.7 \text{ K}\Omega$$

When the input switch is "open", the base current of  $Q_2$  is

$$I_{b2} = \frac{3.0 - 0.7 - 0.5}{27} = 0.066 \text{ ma.}$$

and  $Q_2$  collector current is approximately

$$I_{C2sat} = \frac{9.0}{4.7} \approx 2 \text{ ma.}$$

Then the  $H_{FEsat}$  (at  $I_c = 2 \text{ ma.}$ ) of  $Q_2$  must be

$$\frac{I_{C2sat}}{I_{b2}} = \frac{2.0}{0.066} = 30$$

A silicon planar surface passivated transistor meeting this requirement is the 2N708.

The expected error in zero setting is dependent on





unspecified parameters so the value of  $R_3$  is arbitrarily chosen as 50 ohms.

$D_1$  should be a low leakage diode. The RD 669 is used.

The selection of circuit values for the input network is now complete. The values chosen are shown on the complete schematic diagram, Fig. 16 on page 60.

### III. DISCHARGE CIRCUIT

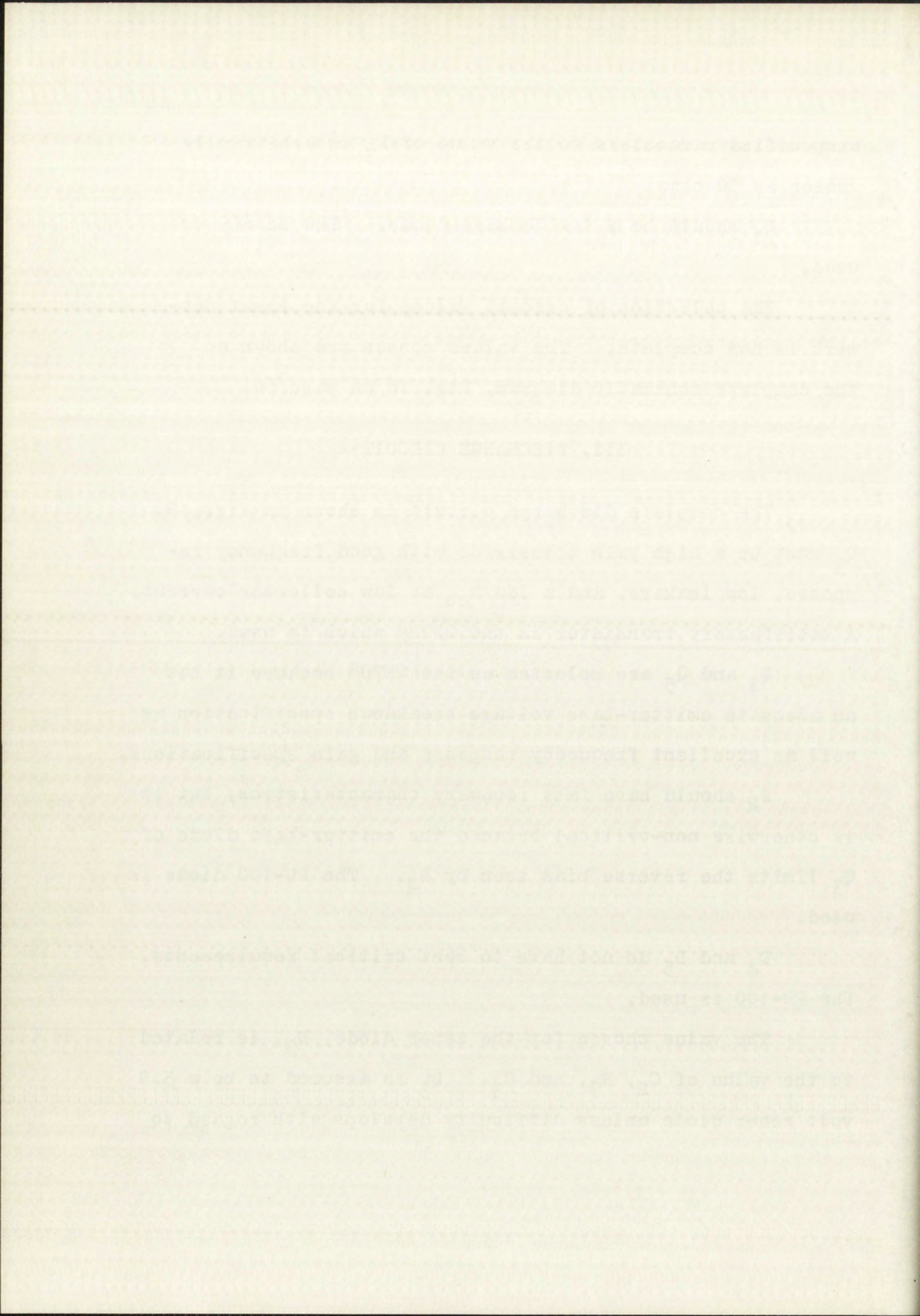
The complete discharge circuit is shown in Fig. 12.  $Q_3$  must be a high gain transistor with good frequency response, low leakage, and a low  $h_{ob}$  at low collector current. A satisfactory transistor is the 2N929 which is used.

$Q_4$  and  $Q_5$  are selected as the 2N708 because it has an adequate emitter-base voltage breakdown specification as well as excellent frequency response and gain specifications.

$D_2$  should have fast recovery characteristics, but it is otherwise non-critical because the emitter-base diode of  $Q_3$  limits the reverse bias seen by  $D_2$ . The FD-100 diode is used.

$D_4$  and  $D_5$  do not have to meet critical requirements. The FD-100 is used.

The value chosen for the zener diode,  $D_3$ , is related to the value of  $C_2$ ,  $R_7$ , and  $C_3$ .  $D_3$  is assumed to be a 5.0 volt zener diode unless difficulty develops with regard to





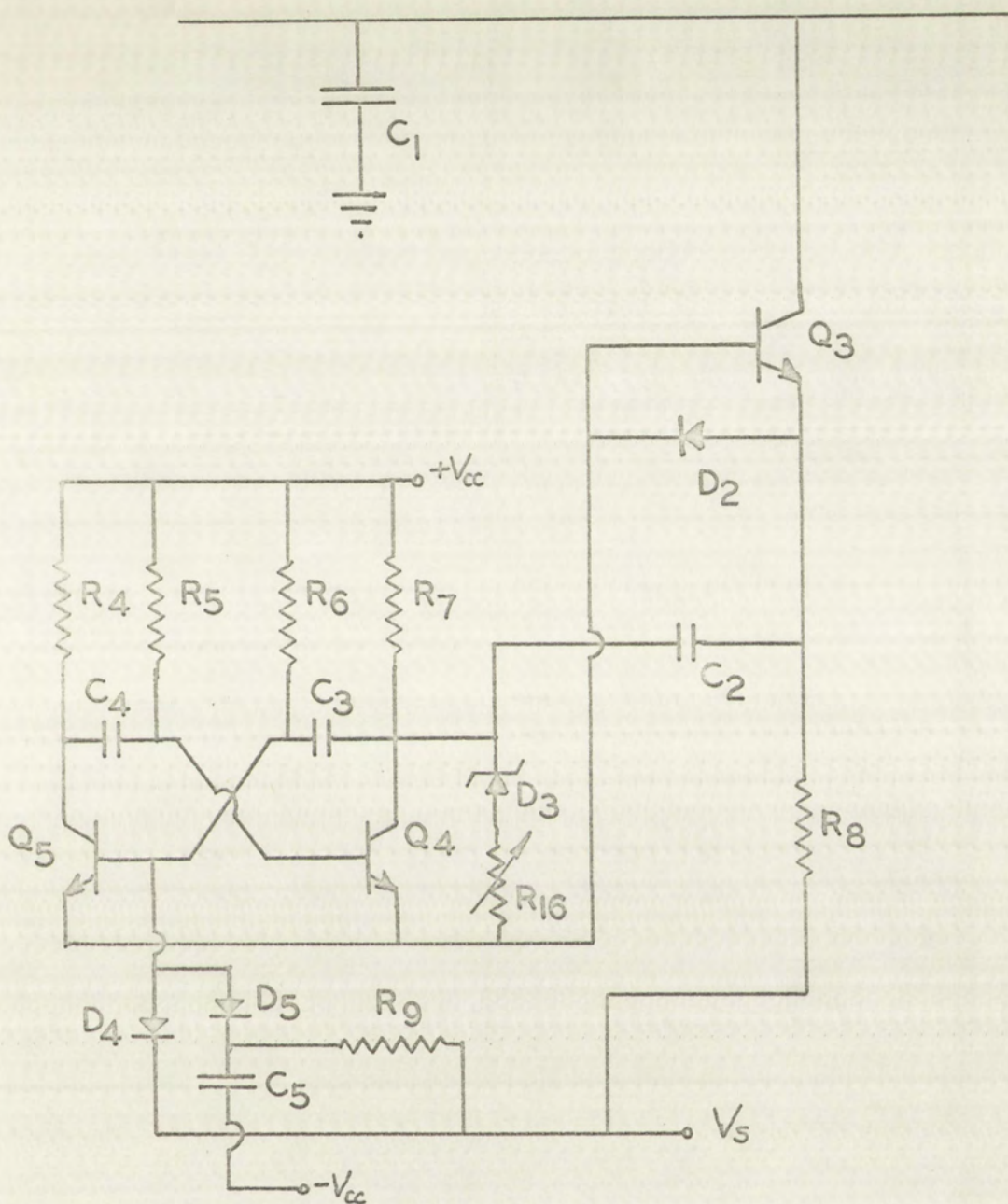


FIGURE 12

COMPLETE DISCHARGE CIRCUIT



FIGURE 15  
COMPLETE DISCHARGE CIRCUIT



the selection of other components. When  $D_3$  is conducting, the conduction current is selected at 4.0 ma. as the best compromise between achieving low zener impedance and low internal heating. The zener current flows through  $R_7$  which drops 4.0 volts at 4 ma.; therefore,  $R_7 = 1 \text{ K } \Omega$ .

If  $Q_4$  is assumed to have a saturated Beta of 15,

$$R_5 = 15 R_7 = 15 \text{ K } \Omega$$

If  $R_9$  is assumed to be comparatively large, the starting delay between the time the control flip-flop is "set" and the time the discharge generator starts pulsing is the time required for  $R_6$  to charge  $C_5$ , thereby bringing  $Q_5$  into conduction. The  $V_{eb}$  of  $Q_5$  must reach + 0.7 volts for  $Q_5$  to conduct. While  $C_5$  is charging, the drop across  $D_5$  is approximately 0.7 volts.  $C_5$  is initially charged to  $V_s$  which is - 5 volts before switching; therefore, the charge on  $C_5$  must change by 2.0 volts to bring  $Q_5$  into conduction.

If  $R_4$  is chosen to have the same change in current that occurs in  $R_7$  in order to keep the supply current constant and reduce ground noise,

$$R_4 = 1.8 \text{ K } \Omega$$

Using a saturated Beta of 15 for  $Q_5$ ,

$$R_6 = 15 \times 1.8 = 27 \text{ K } \Omega$$





The mean voltage drop across  $R_6$  during the starting delay interval is 9.3 volts, so the mean charging current into  $C_5$  from  $R_6$  ( $i_{m6}$ ) is

$$i_{m6} = \frac{9.3}{27} = 0.34 \text{ ma.}$$

Assuming 0.06 ma. flows into  $C_5$  from  $R_9$ , the total mean charging current is 0.40 ma. and  $R_9$  is

$$R_9 = \frac{3.5}{0.06} \cong 60 \text{ K}\Omega$$

If the delay time is selected to be 25 microseconds, from the relation

$$C = \frac{\Delta Q}{\Delta V} = \frac{it}{\Delta V} \quad (17)$$

$$C_5 = \frac{0.4 \times 10^{-3} \times 25 \times 10^{-6}}{2} = 0.005 \text{ mfd.}$$

$C_4$  must hold  $Q_4$  in back bias for one microsecond after  $Q_5$  completes a 9.0 volt switch.  $Q_5$  will switch rapidly enough that the change can be called instantaneous, and the full 9 volt change should appear at the base of  $Q_4$ ; however,  $V_{eb}$  of  $Q_4$  will exhibit a zener breakdown in the region of 7 - 10 volts so the change at the base of  $Q_4$  is assumed to be 8.0 volts, which will depress the base of  $Q_4$  7.3 volts below  $V_{bias}$ . From this level of voltage depression,  $C_4$  will be recharged toward +6 volts through  $R_5$  until  $Q_4$  conducts when  $V_{eb} = +0.7$  volts. This is shown graphically in Fig. 13.

The main subject of this paper is the study of the

properties of the function  $f(x)$  defined by

$$f(x) = \sum_{n=0}^{\infty} \frac{a_n}{n!} x^n$$

where  $a_n$  are the coefficients of the power series

$$A(z) = \sum_{n=0}^{\infty} a_n z^n$$

which is analytic in the region  $|z| < R$ .

It is known that the function  $f(x)$  is analytic in the region

$|x| < R$  and that the function  $f(x)$  is bounded in the region

$|x| < R$  if and only if the function  $A(z)$  is bounded in the region

$|z| < R$ .

The function  $f(x)$  is called the function of the type  $(A)$  if

the function  $A(z)$  is of the type  $(A)$ .

The function  $f(x)$  is called the function of the type  $(B)$  if

the function  $A(z)$  is of the type  $(B)$ .

The function  $f(x)$  is called the function of the type  $(C)$  if

the function  $A(z)$  is of the type  $(C)$ .

The function  $f(x)$  is called the function of the type  $(D)$  if

the function  $A(z)$  is of the type  $(D)$ .

The function  $f(x)$  is called the function of the type  $(E)$  if

the function  $A(z)$  is of the type  $(E)$ .

The function  $f(x)$  is called the function of the type  $(F)$  if

the function  $A(z)$  is of the type  $(F)$ .

The function  $f(x)$  is called the function of the type  $(G)$  if

the function  $A(z)$  is of the type  $(G)$ .

The function  $f(x)$  is called the function of the type  $(H)$  if

the function  $A(z)$  is of the type  $(H)$ .

The function  $f(x)$  is called the function of the type  $(I)$  if

the function  $A(z)$  is of the type  $(I)$ .

The function  $f(x)$  is called the function of the type  $(J)$  if

the function  $A(z)$  is of the type  $(J)$ .



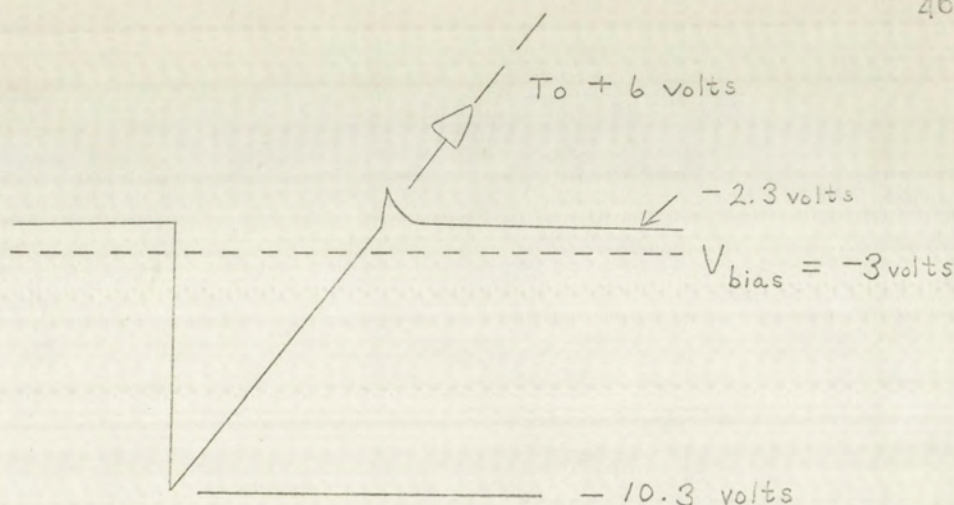


FIGURE 13  
EMITTER-BASE WAVEFORM,  $Q_4$

The voltage changes by 8 volts on a 16.3 volt exponential charging curve, a change that will occur in approximately two-thirds of one time constant. Therefore,

$$\frac{2}{3} R_5 C_4 = 10^{-6} \text{ seconds}$$

but  $R_5 = 15 \times 10^3 \Omega$

Therefore,

$$C_4 = \frac{3}{2} \frac{10^{-6}}{15 \times 10^3} = \frac{10^{-6}}{10^4} \\ = 10^{-10} = 100 \text{ mmfd.}$$

$C_3$  is switched through a change of only 5.0 volts because of the limiting action of  $D_3$ . Therefore, the base of  $Q_5$  will only change by 5 volts on a 13.3 volt exponential





waveform. This corresponds to a 37% change which will occur in approximately 0.47 time constants, so

$$0.47 R_6 C_3 = 10^{-6} \text{ seconds}$$

Therefore, since  $R_6 = 27 \text{ K } \Omega$

$$C_3 = \frac{10^{-6}}{0.47 \times 27 \times 10^3} = 78 \text{ mmfd}$$

$C_2$  is alternately charged through  $D_2$  and discharged through  $Q_3$ . One end of  $C_2$  is switched through 5.0 volts and the opposite terminal changes between the clamping level of  $D_2$  and the clamping level of the emitter-base diode of  $Q_3$  for a total change of 1.4 volts. The voltage change,  $\Delta V_2$ , across the terminals of  $C_2$  is

$$\Delta V_2 = 5.0 - 1.4 = 3.6 \text{ volts}$$

Several factors enter into the choice of  $C_1$  and  $C_2$ . As was previously discussed,  $C_1$  should be as large as possible to minimize leakage effects. The pulse of current through  $Q_3$  should be large compared to  $I_{FE} \times I_{cbo}$ , the leakage of  $Q_3$ , while it is conducting. The voltage resolution is  $\Delta V_2 C_2 / C_1$  which means that for the assumed resolution of 3 mv/count

$$\frac{C_2}{C_1} = \frac{3 \times 10^{-3}}{3.6} = \frac{1}{1.2 \times 10^3}$$





The best capacitors to use for  $C_1$  do not come in sizes larger than 0.01 mfd. If  $C_1$  is assumed to be made up of three of these capacitors, the total value of  $C_1$  is 0.03 mfd; therefore,

$$C_2 = \frac{30 \times 10^3}{1.2 \times 10^3} = 25 \text{ mmfd}$$

The emitter current ( $i_e$ ) of  $Q_3$  can be estimated from the relation

$$i_e = C_2 \frac{de_c}{dt}$$

where  $\frac{de_c}{dt}$  equals the rate of change of collector voltage.

The manufacturer's specifications indicate that the 2N708 will exhibit a rise time of approximately  $10 \times 10^{-9}$  seconds under ideal circuit conditions. This corresponds to a

$$\frac{de}{dt} = \frac{4}{10 \times 10^{-9}} = 4 \times 10^8 \text{ volts per second}$$

in the circuit under discussion, which gives

$$i_e = 25 \times 10^{-12} \times 4 \times 10^8 = 10 \text{ ma.}$$

A rise time of 0.1 microseconds would correspond to an emitter current of 1.0 ma. The true rise time can be expected to be between the above times, so  $i_e$  will be satisfactory.

The first part of the paper is devoted to a discussion of the general principles of the theory of the effect of the magnetic field on the conductivity of a semiconductor.

In the second part the results of the calculations are presented, and in the third part the results of the experiments are discussed.

The calculations show that the effect of the magnetic field on the conductivity of a semiconductor is of the order of  $10^{-4}$  to  $10^{-5}$ .

The experiments show that the effect of the magnetic field on the conductivity of a semiconductor is of the order of  $10^{-4}$  to  $10^{-5}$ .

The results of the calculations and the experiments are in good agreement.

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The results of the calculations and the experiments are in good agreement.



$R_8$  limits the emitter current of  $Q_3$  to 0.15 ma. when the voltage across  $R_8$  is  $(3.0 - 1.0 - 0.7) = 1.3$  volts, so

$$R_8 = \frac{1.3}{0.15} \cong 8.6 \text{ K}$$

Examining the effect of the presence of  $R_8$  on  $\Delta Q$ , it is seen that the current through  $R_8$  significantly alters the current into the emitter of  $Q_3$  if the rise time of  $Q_4$  is long. Should this prove to be a problem,  $R_{11}$  in the control flip-flop can be divided into two resistors of such values that their junction will be at the same potential as the base of  $Q_3$  during the discharge interval. This will reduce the voltage across  $R_8$  to less than one volt, thereby eliminating any significant disturbance !

The value of  $R_{16}$  is determined empirically since it is used to correct for variations in component values.

This completes the specifying of values for the discharge circuit. The selected values are shown on Fig. 16 on the fold-out page numbered 60.

#### IV. THE ZERO DETECTOR

The complete zero detector circuit is shown in Fig. 14. The exciting waveform into this circuit is a 0.5 Mcs sawtooth superimposed on a linear ramp. The Fourier analysis of a sawtooth results in the following equation [ 8a ] .





$$e = \frac{E}{\pi} \left( \sin \omega t - \frac{1}{2} \sin 2\omega t + \frac{1}{3} \sin 3\omega t - \frac{1}{4} \sin 4\omega t + \dots \right) \quad (18)$$

where

$E$  = peak-to-peak amplitude  
 $\omega$  = repetition rate in  
radians/sec

This shows that strong harmonics of the fundamental frequency are present. The transformer should efficiently pass signals in the frequency range from less than 0.5 Mcs to greater than 10 Mcs. It would be desirable to thoroughly analyze this circuit under the assumed conditions of excitation, but that problem is outside the scope of this thesis.

The commercial listings on pulse transformers do not give detailed design information other than rise time and droop related to a standard circuit. If the rise time and droop figures are assumed to be determined only by the transformer characteristics, a 10 Mcs upper cut-off frequency corresponds to a 0.035 microsecond rise time.

Since little choice exists, the transformer is selected on the basis of having a rise time of less than 0.035 microseconds. The UTC-H-64 blocking oscillator transformer has a specified rise time of 0.034 microseconds. It is used.





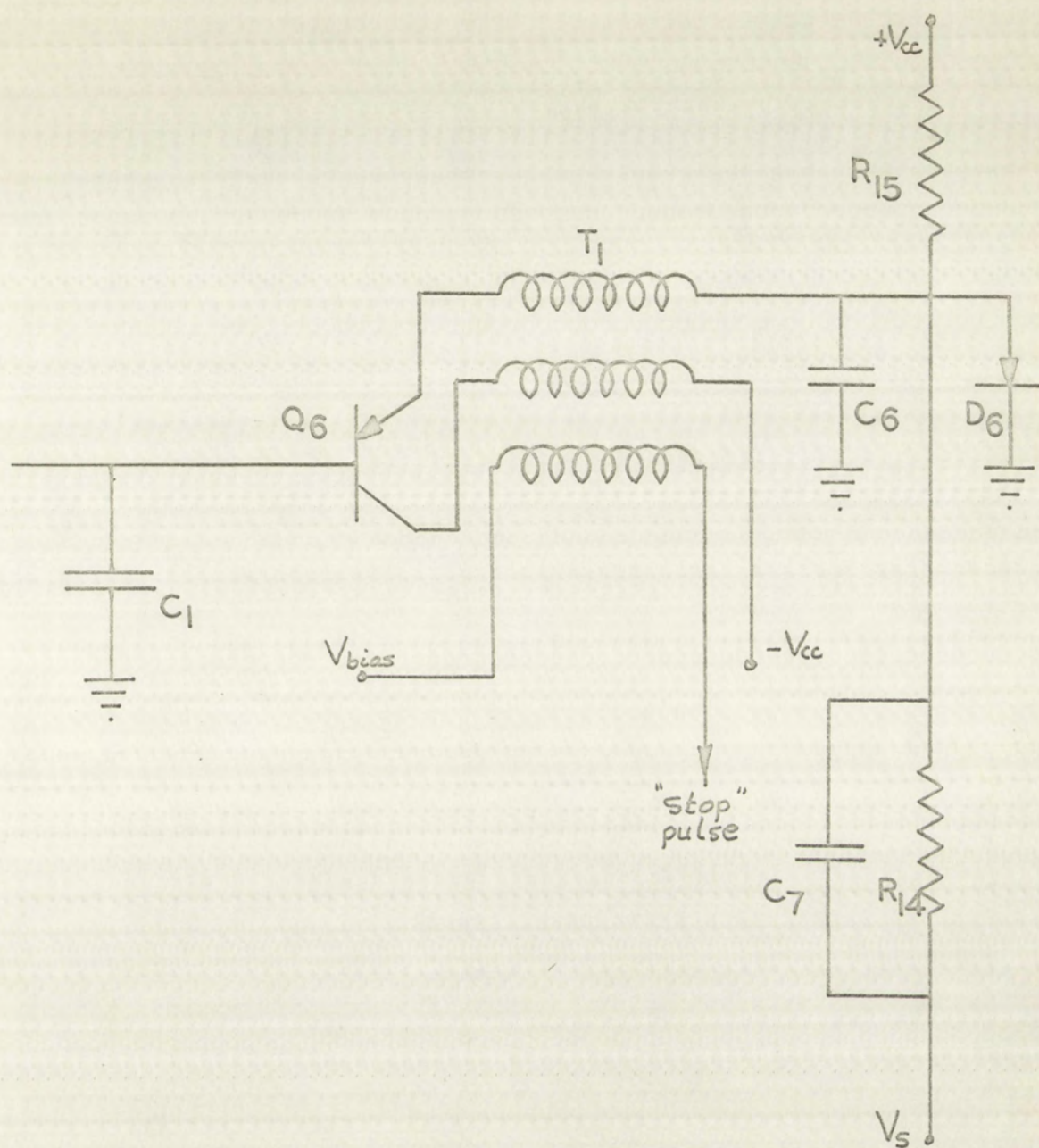


FIGURE 14  
COMPLETE ZERO DETECTOR



FIGURE 4  
COMPLETE ZERO DETECTOR



The transistor must have good frequency response and very low leakage in back bias. The 2N869 meets these requirements.

The diode should match  $D_1$  and operate at approximately the same forward current as is passed through  $D_1$  (0.15 ma.). The forward current comes from  $R_{15}$  so

$$R_{15} = \frac{5.3}{0.15} \cong 36 \text{ K}\Omega$$

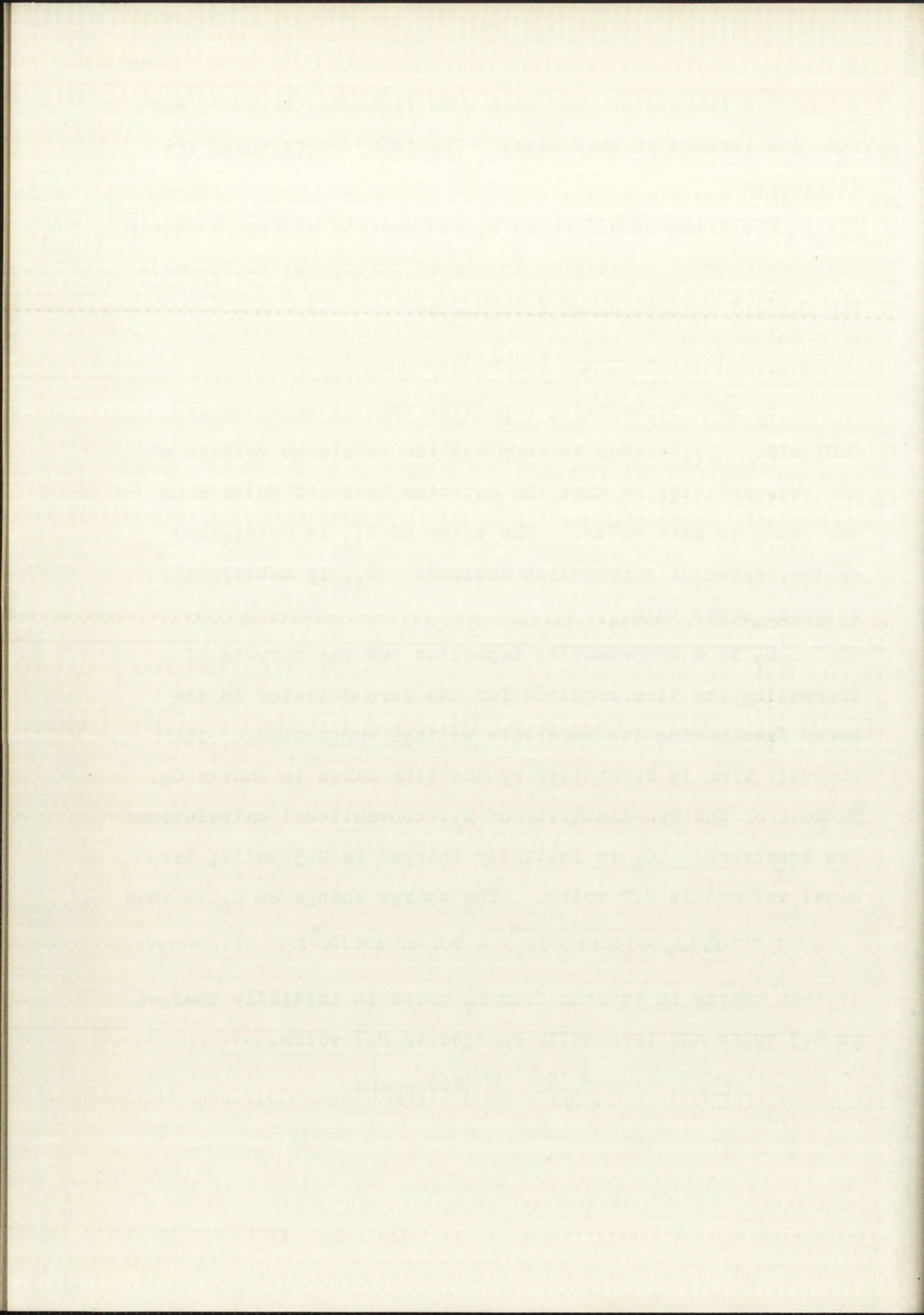
$C_6$  is a stabilizing capacitor that is selected as 0.01 mfd.  $R_{14}$  serves to suppress the reference voltage of the zero detector so that the detector does not pulse when the input is zero volts. The value of  $R_{14}$  is determined by the degree of suppression desired.  $R_{14}$  is arbitrarily selected equal to  $R_{15}$ .

$C_7$  is a compensating capacitor for the purpose of decreasing the time required for the zero detector to recover from having its reference voltage suppressed. The recovery time is determined by the time taken to charge  $C_6$ . Because of the non-linearity of  $D_6$ , conventional calculations are incorrect.  $C_6$  is initially charged to 0.5 volts; terminal voltage is 0.7 volts. The charge change on  $C_6$  is then

$$\Delta Q_6 = (0.01 \times 10^{-6}) \times 0.2 = 2 \times 10^{-9} \text{ C}$$

If this charge is to come from  $C_7$  which is initially charged to 5.5 volts and terminally charged to 0.7 volts,

$$C_7 = \frac{2 \times 10^{-9}}{4.8} \cong 400 \text{ mmfd}$$





The derived value of  $C_7$  will have to be experimentally verified because, if  $C_7$  is too large, the resulting overshoot of the zero detector reference voltage will cause improper operation at very low input voltages.

This completes the specifying of components for the zero detector. The selected values are shown on Fig. 16 on the fold-out page numbered 60.

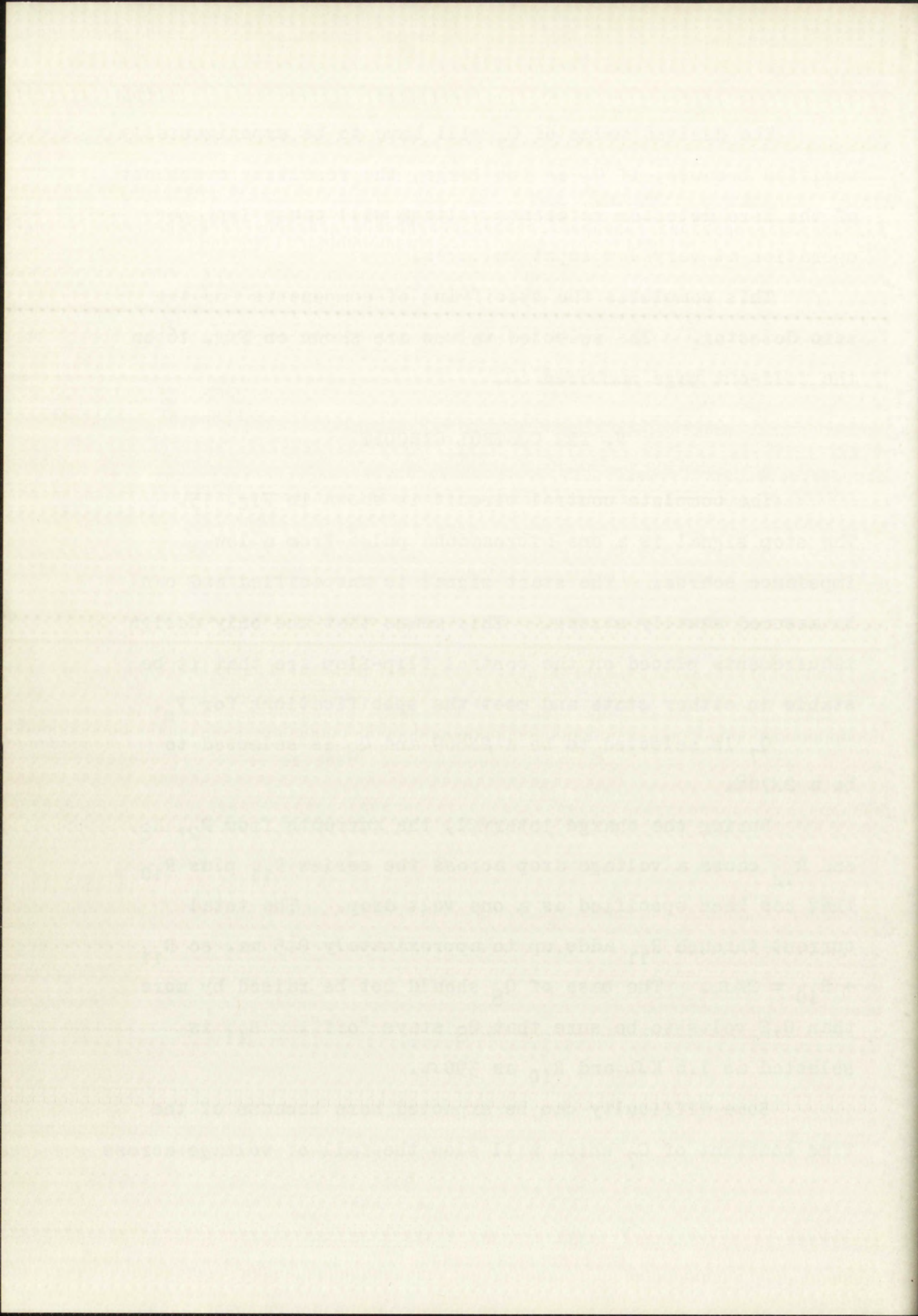
## V. THE CONTROL CIRCUIT

The complete control circuit is shown in Fig. 15. The stop signal is a one microsecond pulse from a low impedance source. The start signal is unspecified and can be assumed equally strong. This means that the only design requirements placed on the control flip-flop are that it be stable in either state and meet the specifications for  $V_S$ .

$Q_7$  is selected to be a 2N869 and  $Q_8$  is selected to be a 2N708.

During the charge interval, the currents from  $R_2$ ,  $R_8$ , and  $R_{14}$  cause a voltage drop across the series  $R_{11}$  plus  $R_{10}$  that has been specified as a one volt drop. The total current through  $R_{11}$  adds up to approximately 0.5 ma. so  $R_{11} + R_{10} = 2K\Omega$ . The base of  $Q_8$  should not be raised by more than 0.2 volts to be sure that  $Q_8$  stays "off".  $R_{11}$  is selected as 1.6  $K\Omega$  and  $R_{10}$  as 390 $\Omega$ .

Some difficulty can be expected here because of the time constant of  $C_7$  which will slow the fall of voltage across





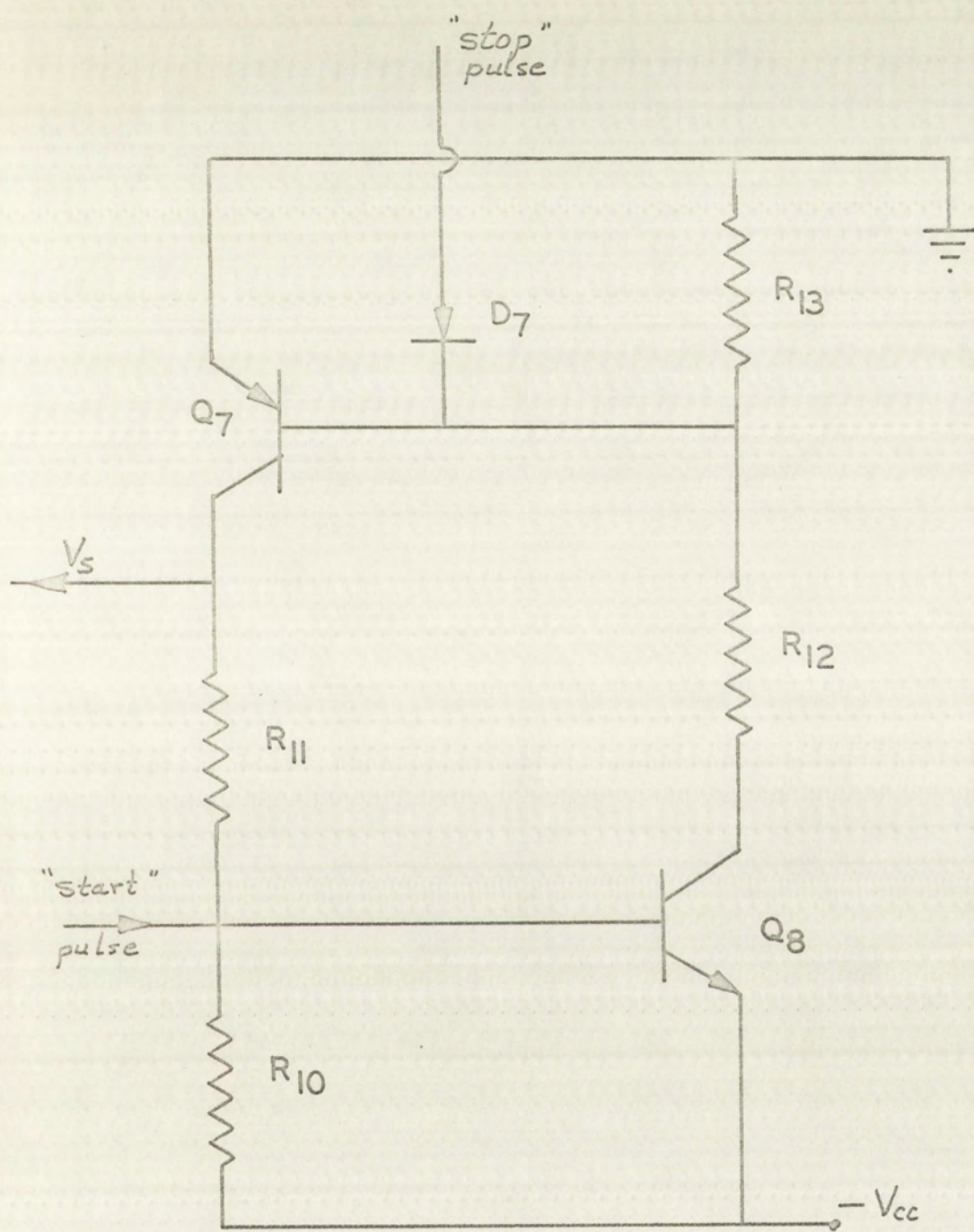


FIGURE 15

COMPLETE CONTROL CIRCUIT



FIGURE 15

COMP. CTE CONTROL CIRCUIT



$R_{11}$  and  $R_{10}$ . This problem can be resolved by decreasing  $C_7$  which, as was discussed earlier, may be necessary anyway. If it is undesirable to decrease  $C_7$  and a problem does exist, the third winding of the pulse transformer may be connected to turn off  $Q_8$  which would, through  $R_{11}$ , discharge  $C_7$  faster.

$Q_7$  has a collector current of approximately 3.2 ma. If  $R_{13}$  is arbitrarily selected as 2 K $\Omega$ , the value of  $R_{12}$  can be 6.8 K $\Omega$ .

$D_7$  is not critical. An FD-100 will be used.

This completes the specifying of components for the control flip-flop. The selected values are shown on Fig. 16 on the fold-out page numbered 60.

## VI. TEMPERATURE VERSUS ACCURACY

Temperature changes can be expected to affect both the zero adjustment and the value of each count. In addition, leakage of an ohmic nature will affect the linearity of the input - output relation.

The zero stability is determined by how well the drop across  $D_1$  is matched by the drop across  $D_6$  and how well the  $V_{eb}$  of  $Q_1$  is matched by the  $V_{eb}$  of  $Q_6$ . If these components do not "track" with temperature changes, temperature sensitive resistors can be used in appropriate places to cause the current through  $Q_1$ ,  $D_1$ , or  $D_6$  to change such as to achieve temperature stability of the zero point.





The emitter-base voltage of  $Q_3$  and the forward voltage of  $D_3$  will change by  $2.0 \text{ mv}/^\circ\text{C}$  temperature change. If the voltage drop across  $D_3$  is assumed constant and the value of  $C_2$  is assumed constant, the  $\Delta Q$  available from  $C_2$  will increase by  $4/3600$  or  $0.11\%$  for every  $^\circ\text{C}$  increase in temperature. This change will be partially offset by the fact that the capacitors chosen for use as  $C_1$  exhibit a  $0.015\%$  per  $^\circ\text{C}$  increase in capacitance leaving a net increase of  $0.095\%$  per  $^\circ\text{C}$  change which does not include contributions from the temperature dependent characteristics of  $D_3$ . The net change of  $0.095\%$  per  $^\circ\text{C}$  can be partially offset by using a capacitor for  $C_2$  that exhibits a negative temperature coefficient. Capacitors such as the Spague 10TCU type exhibit a negative temperature coefficient of  $0.075\%$  per  $^\circ\text{C}$ . Such a capacitor is used to reduce the temperature dependence of  $Q_2$  to  $0.02\%$  per  $^\circ\text{C}$ . The remaining error must be compensated by selecting the value and operating current of  $D_3$  to give the required temperature coefficient.

## VII. THE MODEL

The specified components were assembled and a model of the conversion network was built. For convenience in testing, the components in the model are arranged in the same relative location as in the drawing of Fig. 18 on page 83. The model is assembled on a printed wiring board with most of





the connections being completed by printed wiring. Top and bottom views of the completed model are shown in Plates 1 and 2.

The detailed tests of the model are reported in the next chapter. During the preliminary tests of the network, it was found that it was desirable to change  $R_{11}$  to two resistors as discussed on page 49.\*

The H-64 blocking oscillator transformer was chosen for use in the zero detector circuit because it was designed for use with transistors and it has the short rise time required in this application.\*\* However, the manufacturer's recommended connection of the H-64 transformer is specified as a 4:1 ratio of primary turns to secondary turns. Preliminary experimentation disclosed that the best blocking oscillator transformer turns ratio for stable operation of the zero detector is 2:1; therefore, the H-64 transformer was replaced by an H-48 transformer.\*\*\*

---

\*The revised connection is shown in Fig. 18 on page 83. The change can be seen in Plate 1.

\*\*Discussed on page 50.

\*\*\*The H-48 transformer has a 0.03 microsecond rise time. It was not selected originally because it was designed for use with vacuum tube circuits; however, it works well in this application. The revised connection is shown in Fig. 18 on page 83. The change can be seen in Plate 1.

R7  
IK



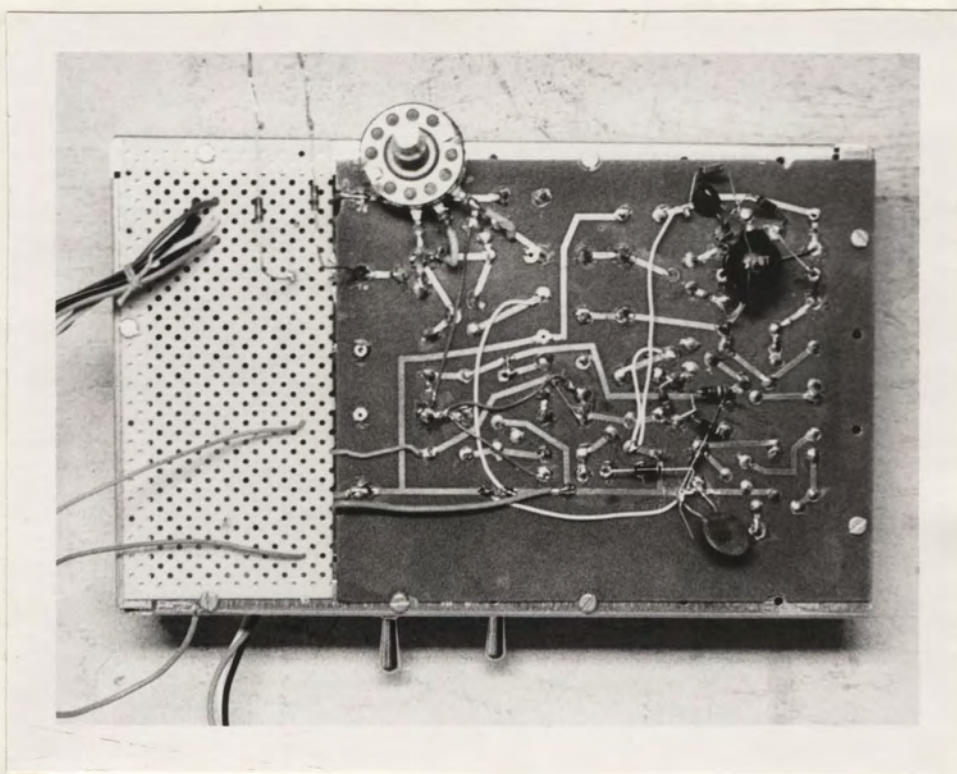


PLATE 1

TOP VIEW OF THE MODEL ANALOG-TO-DIGITAL  
VOLTAGE CONVERSION NETWORK

R7  
IK



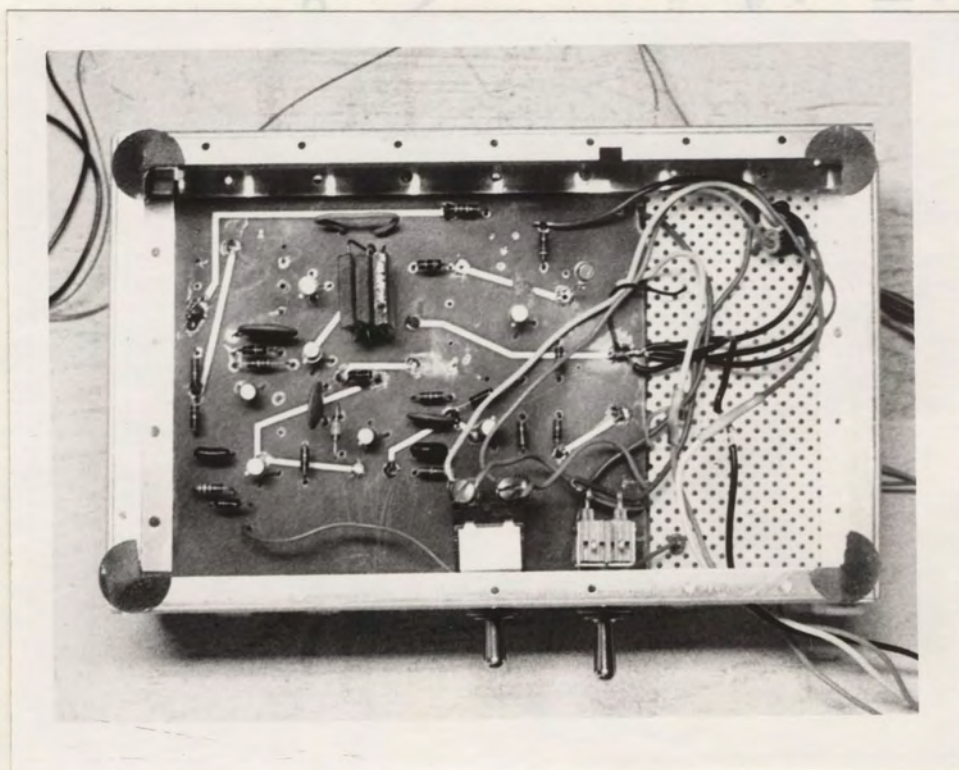


PLATE 2  
 BOTTOM VIEW OF THE MODEL ANALOG-TO-DIGITAL  
 VOLTAGE CONVERSION NETWORK

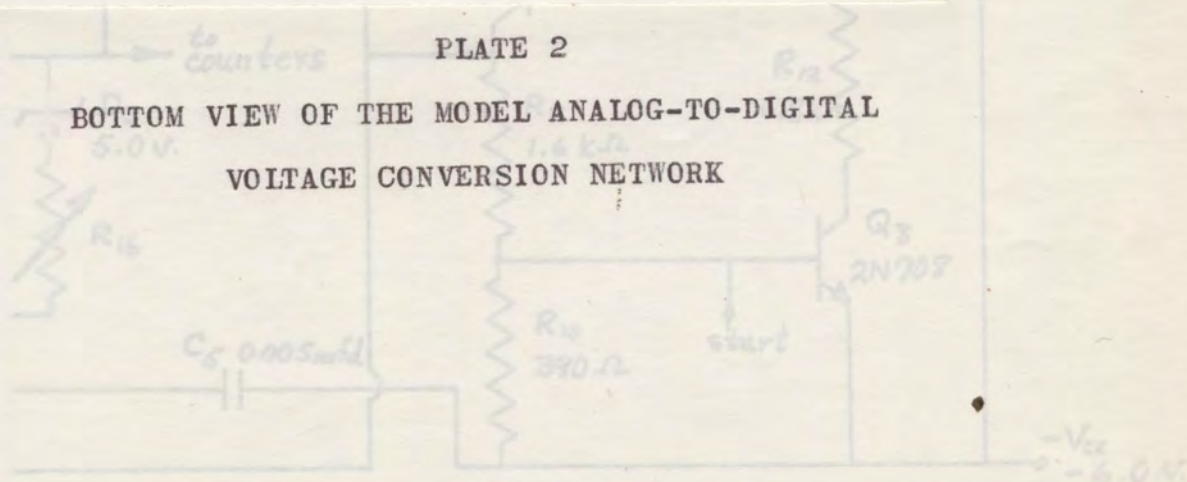


FIGURE 16

R7  
IK



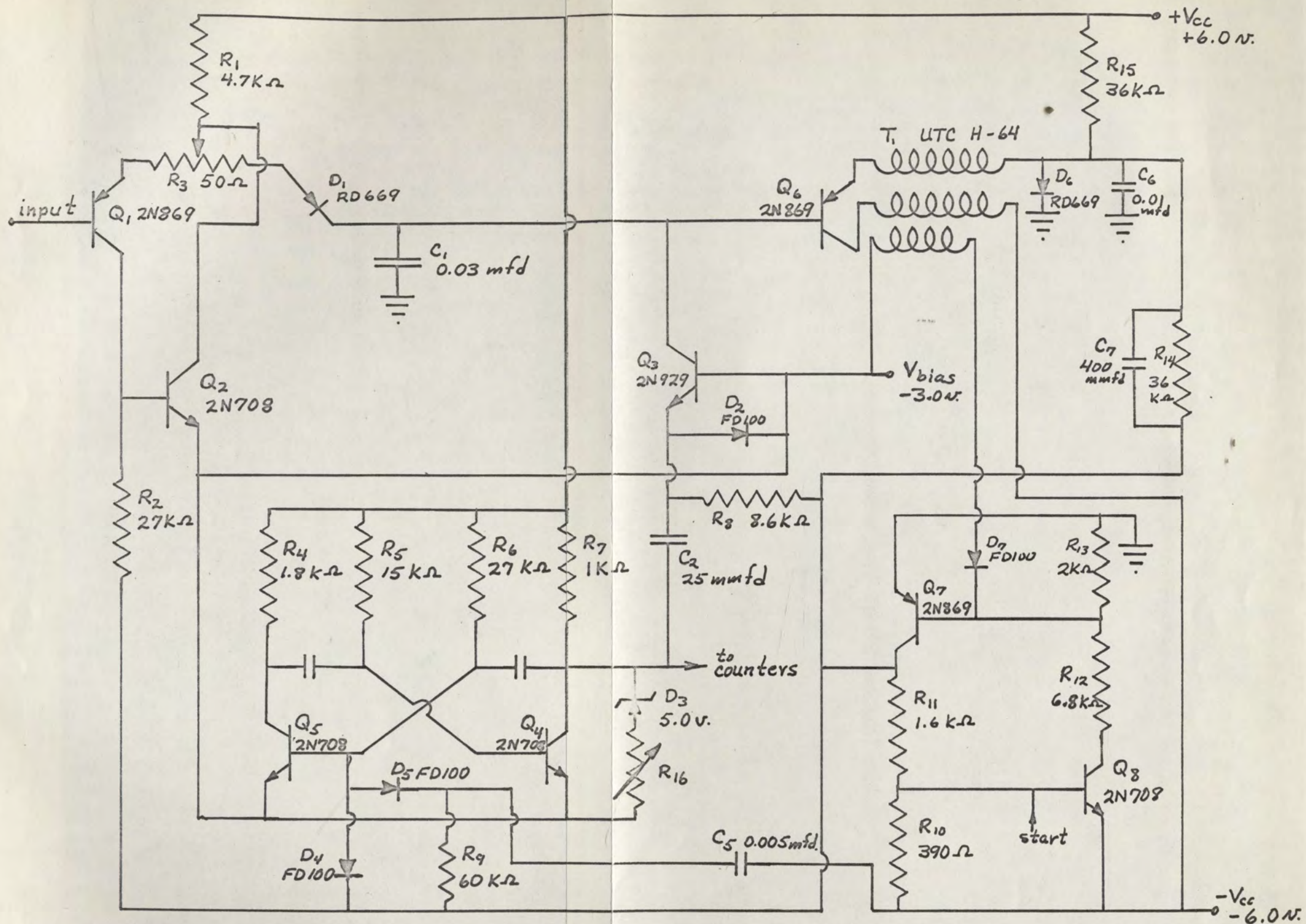


FIGURE 16

SCHEMATIC DIAGRAM -- ANALOG-TO-DIGITAL  
CONVERSION NETWORK



R7  
IK



## CHAPTER V

### TESTING THE MODEL NETWORK

The purpose of this chapter is to report the results of tests conducted on the model network designed in chapter four. The first series of tests is a check on the quiescent behaviour of the network. The second series of tests measures the dynamic performance of the network. The third series of tests determines the effect of temperature on input - output relations.

The test equipment is itemized and described on page 62. Prior to each test report, the test equipment is referenced, and the experimental procedure is described.

The test reports are presented in tabular form where appropriate. The reports contain the previous predictions, the corrected predictions (that include the effects of disturbances caused by the measuring equipment), and the measured values. Each test is interpreted and evaluated.

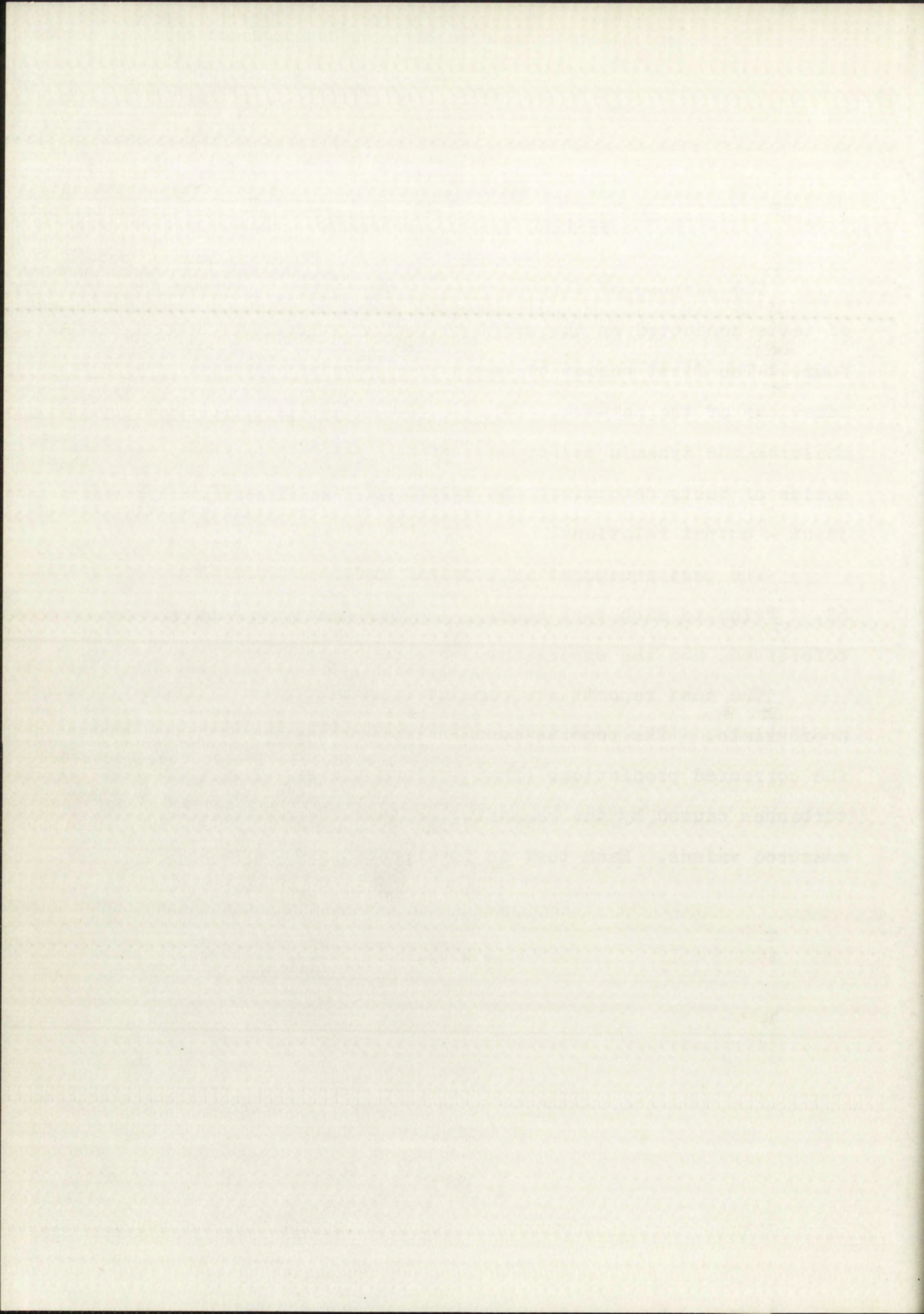
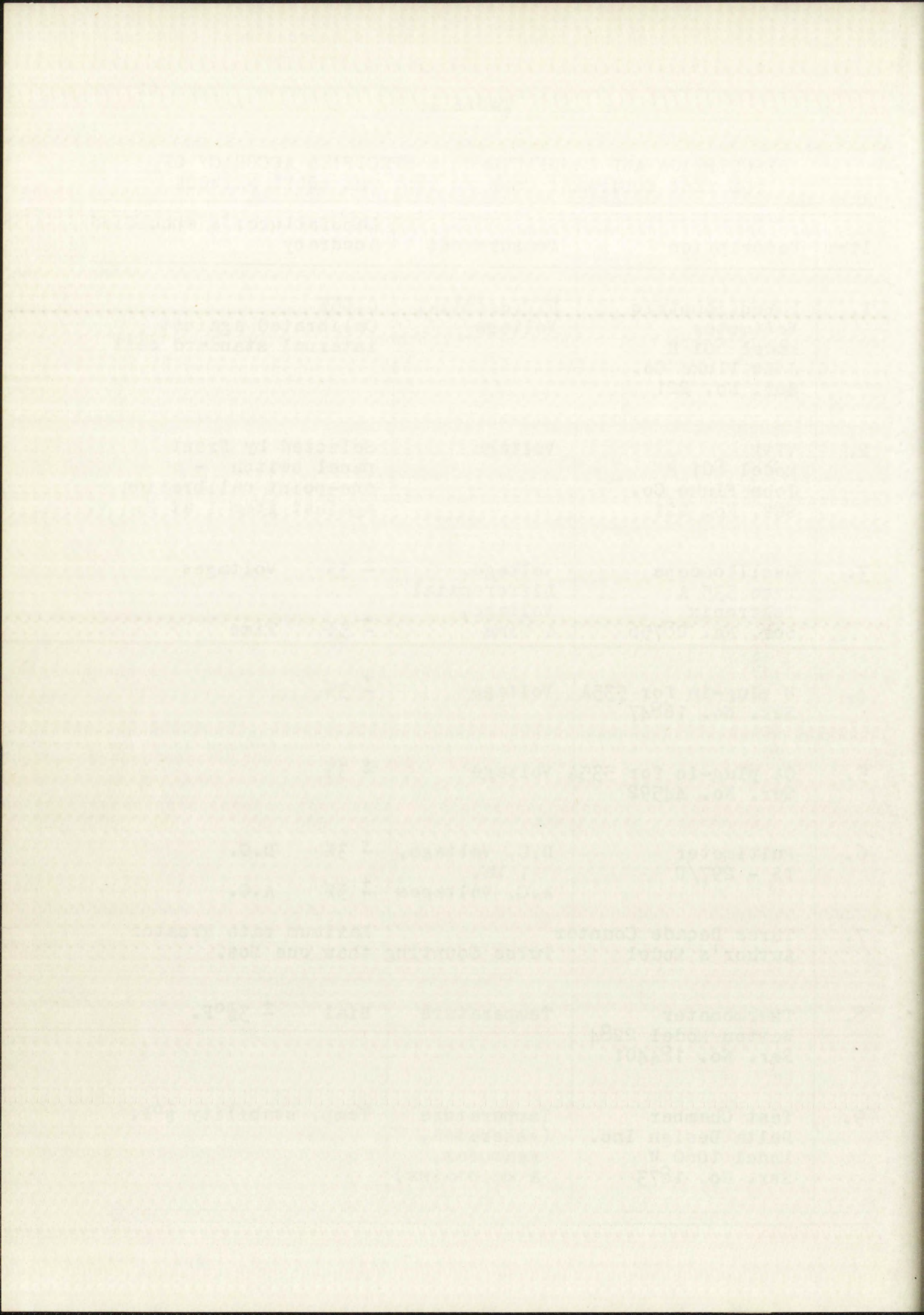




TABLE I

DESCRIPTION AND MANUFACTURER'S SPECIFIED ACCURACY OF  
THE TEST EQUIPMENT USED TO TEST THE MODEL NETWORK

Item	Description	Measurement	Manufacturer's specified Accuracy
1.	Potentiometric Voltmeter Model 801 H John Fluke Co. Ser. No. 221	Differential Voltage	0.05% Calibrated against internal standard cell
2.	VTVM Model 801 H John Fluke Co. Ser. No. 221	Voltage	Selected by front panel switch - one-point calibration against item 1 at 2.6 v.
3.	Oscilloscope Type 535 A Tektronix Ser. No. 28756	Voltage, Differential Voltage, & Time	$\pm 3\%$ Voltages $\pm 5\%$ Time
4.	D plug-in for 535A Ser. No. 16847	Voltage	$\pm 3\%$
5.	CA plug-in for 535A Ser. No. 44592	Voltage	$\pm 3\%$
6.	Multimeter TS - 297/U	D.C. Voltage, , Ma. A.C. Voltages	$\pm 3\%$ D.C. $\pm 5\%$ A.C.
7.	Three Decade Counter Author's Model	Pulse Counting	Maximum rate greater than one Mcs.
8.	Thermometer Weston Model 2284 Ser. No. 184401	Temperature	Dial $\pm 3\frac{1}{2}^{\circ}\text{F.}$
9.	Test Chamber Delta Design Inc. Model 1060 W Ser. No. 1873	Temperature (generates, measures, & maintains)	Temp. stability $\frac{1}{2}^{\circ}\text{F.}$





# I. THE QUIESCENT TESTS

Test procedure. The model network was connected to batteries to provide  $+V_{cc}$ ,  $-V_{cc}$ , and  $V_{bias}$ . A 1000 ohm, 10 turn potentiometer was connected across  $V_{cc}$  to ground and the center-tap was connected to the input terminal to supply the input voltage. After preliminary checks, the d.c. voltages present during the charge interval were measured with a VTVM, item 2, page 62. All the voltages were measured with respect to circuit ground.

Test results. The following measurements were taken.

- ① \* + 0.12 volts ; input potentiometer at minimum setting
- ② + 0.74 volts ;  $R_3$  set full CCW
- ③ + 0.76 volts
- ④ + 0.18 volts ; drop across  $D_1$  is less than was expected,  
( 0.76 - 0.18 = 0.58 volts )
- ⑤ + 0.23 volts ; less than predicted value of 0.50 volts,  
but accounted for by the error in  $V_s$  ( ⑪ )
- ⑥ + 6.1 volts ;  $+V_{cc}$
- ⑦ - 6.2 volts ;  $-V_{cc}$

---

\*The test points are indicated by encircled numbers on Fig. 18 on the fold-out page 83.





- ⑧ - 3.1 volts ;  $V_{bias}$
- ⑨ - 2.8 volts
- ⑩ - 2.4 volts ; as predicted
- ⑪ - 5.4 volts ; 0.2 volts low when corrected for error in  $-V_{CC}$  (⑦)
- ⑫ - 4.8 volts ;  $Q_5$  back-bias = 1.7 volts, which is 0.7 volts greater than predicted
- ⑬ - 2.3 volts ;  $V_{eb}$  of  $Q_4$  = 0.8 volts
- ⑭ - 3.7 volts ;  $V_{eb}$  of  $Q_3$  = 0.6 volts
- ⑮ - 5.8 volts
- ⑯ - 6.0 volts ;  $V_{eb}$  of  $Q_8$  = 0.2 volts as predicted
- ⑰ - 5.2 volts
- ① The input current at test point ① is 30 microamps.

Test conclusions. The drop across  $D_1$  is lower than expected. It would appear that the value of  $R_3$  is lower than the value necessary to accomplish zero correction. The measurement of the base current of  $Q_1$  (30 microamps) indicates that the  $H_{FE}$  is five at its selected operating point. The low  $H_{FE}$  of  $Q_1$  does not seriously disturb the operating characteristics of the input network because of the feedback connection of  $Q_1$  and  $Q_2$ . The measurements indicate that the d.c. voltages are essentially as predicted.

indicates that the d.c. voltages are essentially as predicted.

The feedback connection of  $G_1$  and  $G_2$ . The parameters:

existing characteristic of the input network because of

point. The low  $H_{11}$  of  $G_1$  does not seriously disturb the

indicated that the  $H_{11}$  is five at the selected operating

The measurement of the base current of  $G_1$  (30 microamps)

than the value necessary to accomplish zero correction.

expected. It would appear that the value of  $H_{11}$  is lower

these connections. The drop across  $D_1$  is lower than

① The input current at test point ① is 50 microamps

②  $V_{D_1} = 0.5$  volts

③  $V_{D_2} = 0.5$  volts ;  $V_{D_3} = 0.2$  volts as predicted

④  $V_{D_4} = 0.2$  volts

⑤  $V_{D_5} = 0.1$  volts ;  $V_{D_6} = 0.0$  volts

⑥  $V_{D_7} = 0.2$  volts ;  $V_{D_8} = 0.8$  volts

⑦  $V_{D_9} = 0.7$  volts ;  $V_{D_{10}} = 0.7$  volts

⑧  $V_{D_{11}} = 0.7$  volts ;  $V_{D_{12}} = 0.7$  volts

⑨  $V_{D_{13}} = 0.7$  volts ;  $V_{D_{14}} = 0.7$  volts

⑩  $V_{D_{15}} = 0.7$  volts ;  $V_{D_{16}} = 0.7$  volts

⑪  $V_{D_{17}} = 0.7$  volts ;  $V_{D_{18}} = 0.7$  volts

⑫  $V_{D_{19}} = 0.7$  volts ;  $V_{D_{20}} = 0.7$  volts

⑬  $V_{D_{21}} = 0.7$  volts ;  $V_{D_{22}} = 0.7$  volts

⑭  $V_{D_{23}} = 0.7$  volts ;  $V_{D_{24}} = 0.7$  volts

⑮  $V_{D_{25}} = 0.7$  volts ;  $V_{D_{26}} = 0.7$  volts



## II. DYNAMIC TESTS

The dynamic tests include general tests (measurement of noise, voltage change during the delay interval, waveforms, etc.), a linearity test at room temperature, a test to determine the amount of leakage present, and a test to determine the conversion stability with respect to frequency.

Test procedure common to all the dynamic tests. The power connections and the input voltage connections for the dynamic tests were the same as those for the quiescent tests. In addition, the required start pulse was derived from the "+ B Gate" binding post of the oscilloscope. The oscilloscope was adjusted so that the B sweep would free-run, thereby generating a repetitive sweep that automatically resulted in synchronization between the oscilloscope sweep and the cycling of the network.

The potentiometric voltmeter was connected between the input terminal and ground with isolating resistors in both voltmeter leads to prevent interaction between the voltmeter and the model network.\*

All of the waveforms and voltages were referenced to circuit ground unless otherwise indicated.

The general tests. The purpose of the following tests was to check the gross operating characteristics of the network.

---

\*The isolating resistors do not disturb the measurement because the input impedance of the voltmeter is essentially infinite at null balance.

## 11. EXPERIMENTAL TESTS

The dynamic tests were performed in the following manner:

At first, voltage drops across the motor terminals, current

flow, etc., were measured at room temperature, a test

to determine the model of the motor was made.

During the operation of the motor with respect to frequency,

the frequency was varied from 50 to 60 Hz.

Power connections and the input voltage connections for the

dynamic tests were the same as those for the permanent test.

In addition, the recorded data were derived from the

"2.5 A-10" bridge part of the oscilloscope. The oscilloscope

scope was adjusted so that the wave would be linear.

When power was applied to the motor, the oscilloscope

resulted in synchronization between the oscilloscope wave

and the output of the motor.

The potentiometer voltage was connected between

the input terminals and ground with isolating resistors in

both voltmeter leads to prevent interaction between the

voltmeter and the motor network.

All of the waveforms and voltages were referenced

to a common ground unless otherwise indicated.

The results of the tests are given in the following table.

The results of the tests are given in the following table.

was to check the gross operating characteristics of the motor.

The isolating resistors do not disturb the results

because the input impedance of the voltmeter is

very high at all times.



Measurements were taken of the noise present during the discharge interval. The noise was observed on the oscilloscope; the CA plug-in was used. The measurements were :

1. At test point (6), the noise on  $+V_{cc} = 0.3$  volts peak-to-peak.
2. At test point (7), the noise on  $-V_{cc} = 0.1$  volts peak-to-peak.
3. At test point (8), the noise on  $V_{bias} = 0.8$  volts peak-to-peak.

The noise consisted of approximately three cycles of a ten megacycle per second decaying transient that occurs every half cycle of the discharge generator.

During the discharge interval, the following measurements were taken so the operating values could be compared to the values assumed or predicted when the network was being designed in chapter four.

1. The positive value of  $V_s$  (at test point (11) ) equals  $-0.25$  volts. The assumed value was  $-0.5$  volts. The difference is not significant.
2. The voltage change on  $C_5$  (at (17) ) during the delay interval was  $2.5$  volts rather than the expected  $2.0$  volts. The delay period was  $36$  microseconds. The voltage on  $C_5$  was observed

Measurements were taken at the three pressure points

the discharge interval. The noise was observed on the

oscilloscope. The first was at the beginning of the

1. The positive value of  $V_p$  (at test point 1)

voice peak-to-peak

2. The negative value of  $V_n$  (at test point 2)

voice peak-to-peak

3. The value of  $V_{avg}$  (at test point 3)

voice peak-to-peak

The noise consisted of approximately three cycles of a tone

frequency and second harmonic component that occurs every

half cycle of the discharge generator.

During the discharge interval, the following results

were taken so the operating values could be compared

to the values assumed or predicted when the network was

being designed in Chapter Four.

1. The positive value of  $V_p$  (at test point 1)

equals -0.55 volts. The assumed value was

-0.5 volts. The difference is not significant.

2. The negative value of  $V_n$  (at test point 2)

delay interval was 2.5 volts rather than the

expected 2.0 volts. The delay period was 25

microseconds. The voltage on C was observed



to change by 2.0 volts in 28 microseconds.  
The predicted time for a 2.0 volt change was 25 microseconds.

3. The peak-to-peak amplitude of the square wave at the collector of  $Q_4$  (at ⑨) equals 4.3 volts. The assumed amplitude was 5.0 volts.
4. The peak-to-peak amplitude at the emitter of  $Q_3$  (at ⑭) equals 1.45 volts which is essentially the assumed value.

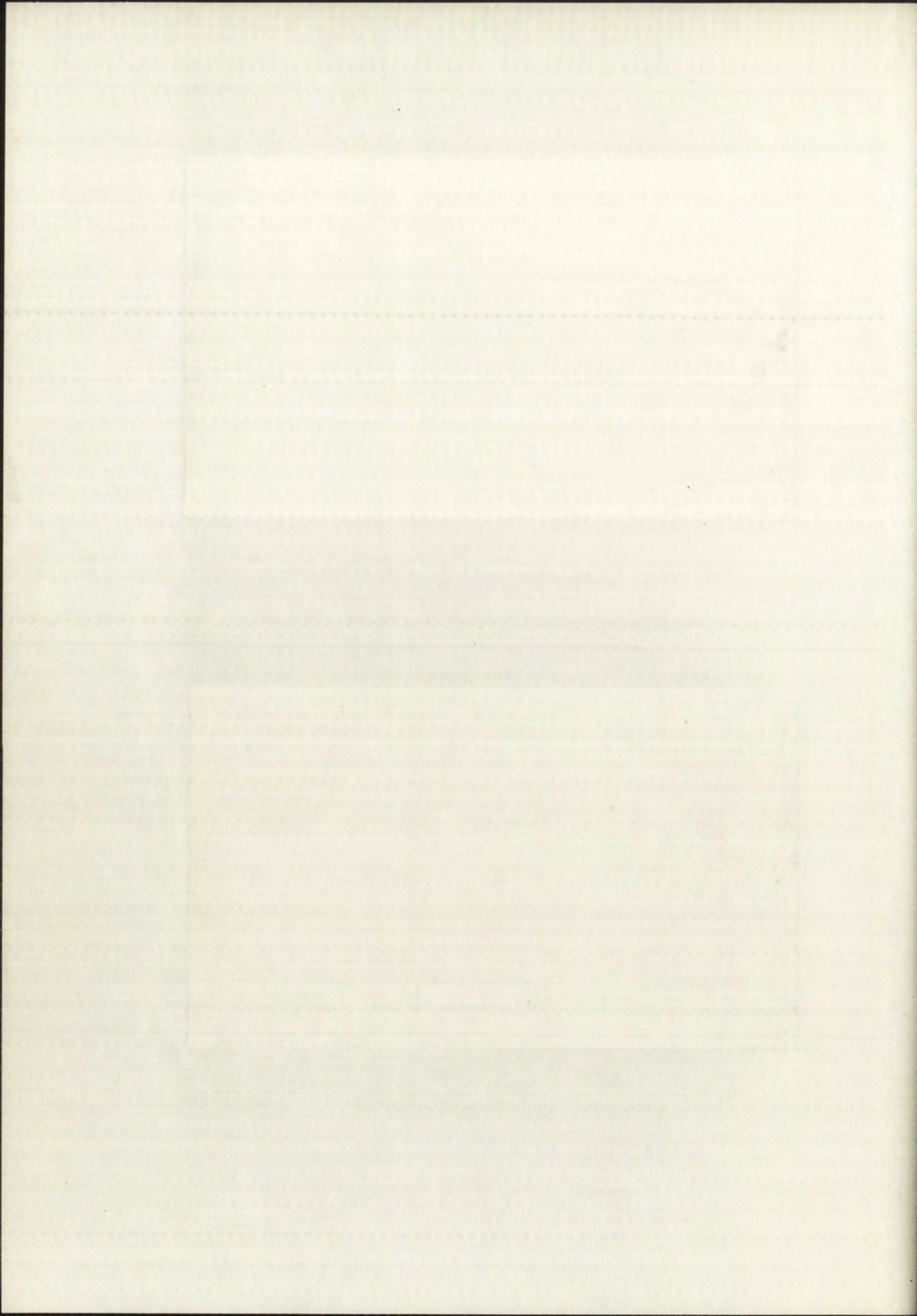
The last two measurements show that the charge voltage on  $C_2$  was approximately 2.9 volts instead of the predicted value of 3.6 volts. This means that the resolution is approximately 2.4 millivolts per count.

Plate 3 shows a portion of the voltage on  $C_1$  (at test point ④). An expanded view of the same waveform is shown in Plate 4.

The behaviour of the emitter of  $Q_6$  ( ⑱ ) is shown in Plate 5. The waveform terminates due to the switching of the zero detector. The behaviour of the voltage across  $D_6$  is shown in Plate 6.

The output of the zero detector ( ⑲ ) is shown in Plate 7, and an expanded view of the same waveform is shown in Plate 8. Plate 7 and Plate 8 have the same time relations.

The wavetrain at the collector of  $Q_4$  ( ⑨ ) is shown in Plate 9; an expanded view is shown in Plate 10; Plate 11





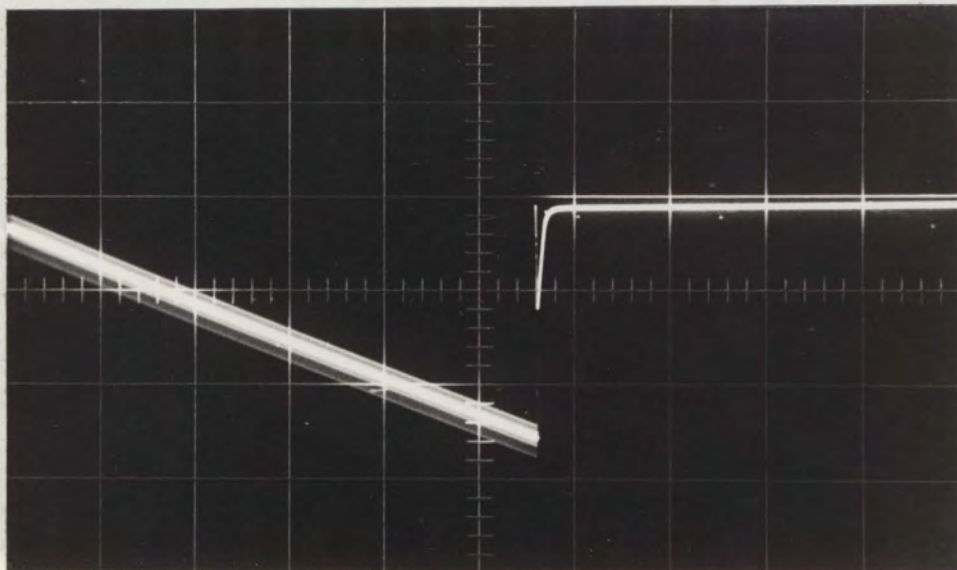


PLATE 3

DISCHARGE AND RECOVERY OF  $C_1$   
 (D plug-in; 0.5 v/cm; 200  $\mu$ s/cm)

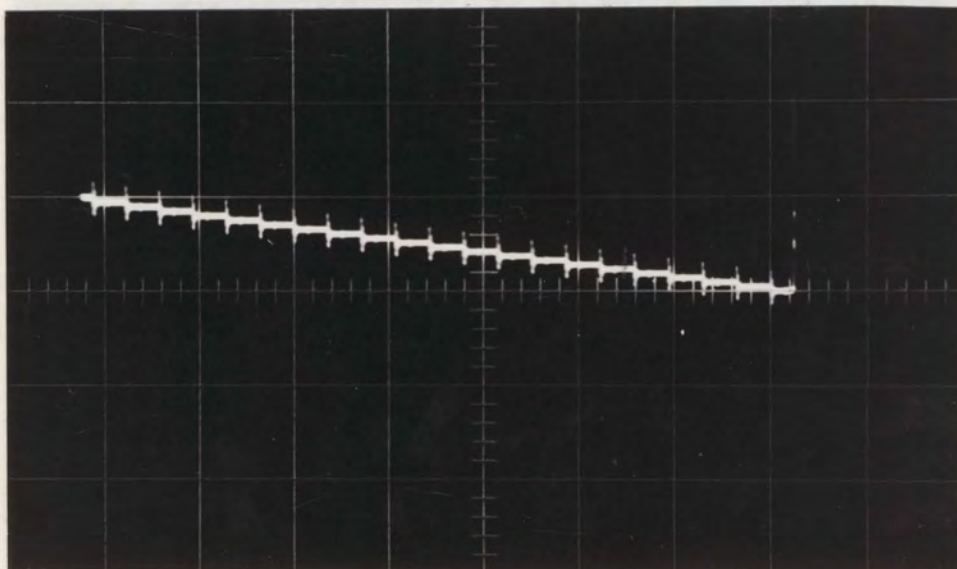
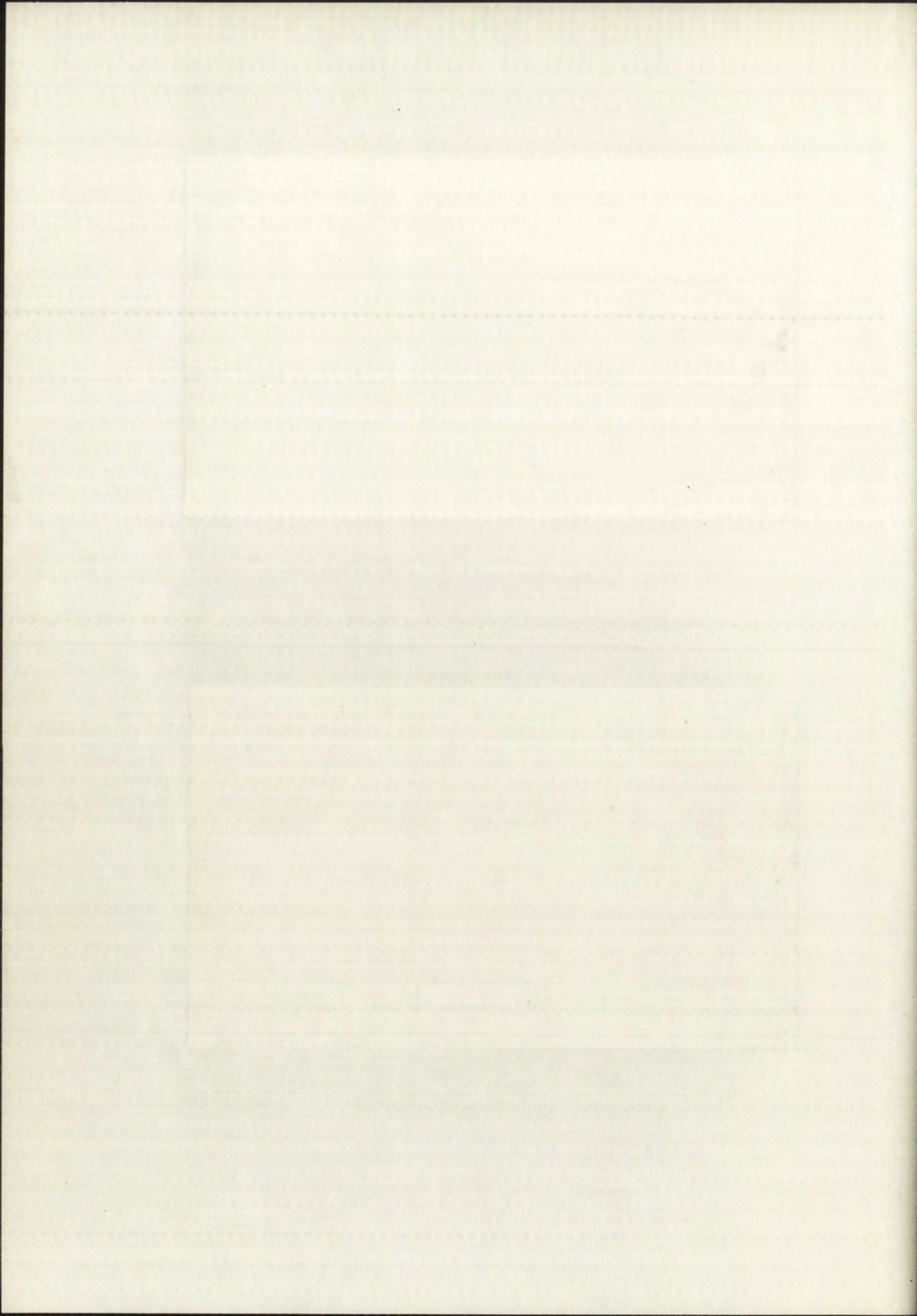


PLATE 4

EXPANDED VIEW OF THE DISCHARGE AND RECOVERY OF  $C_1$   
 (CA plug-in; 50 mv/cm; 5  $\mu$ s/cm)





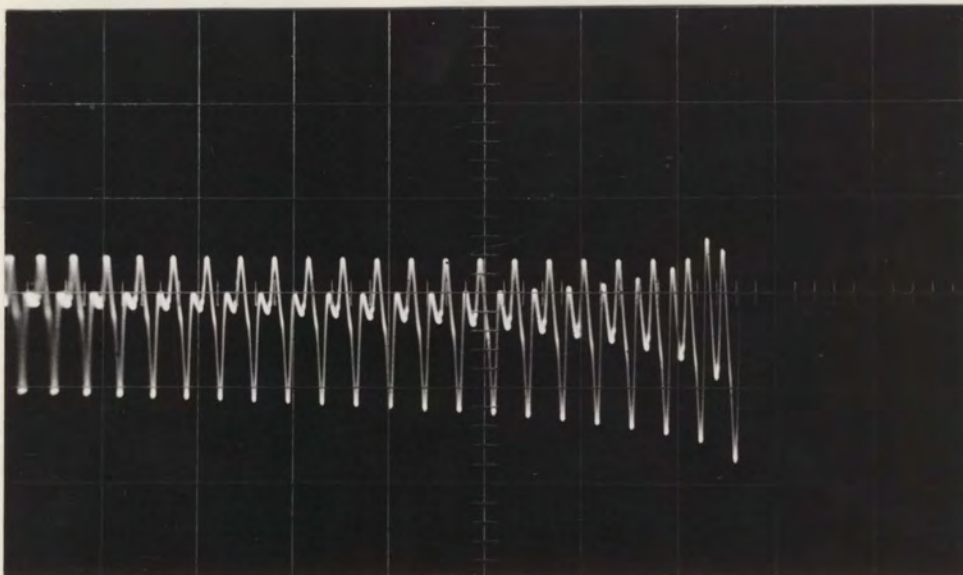


PLATE 5

WAVEFORM AT THE EMITTER OF  $Q_6$

(D plug-in; 50 mv/cm; 5  $\mu$ s/cm)

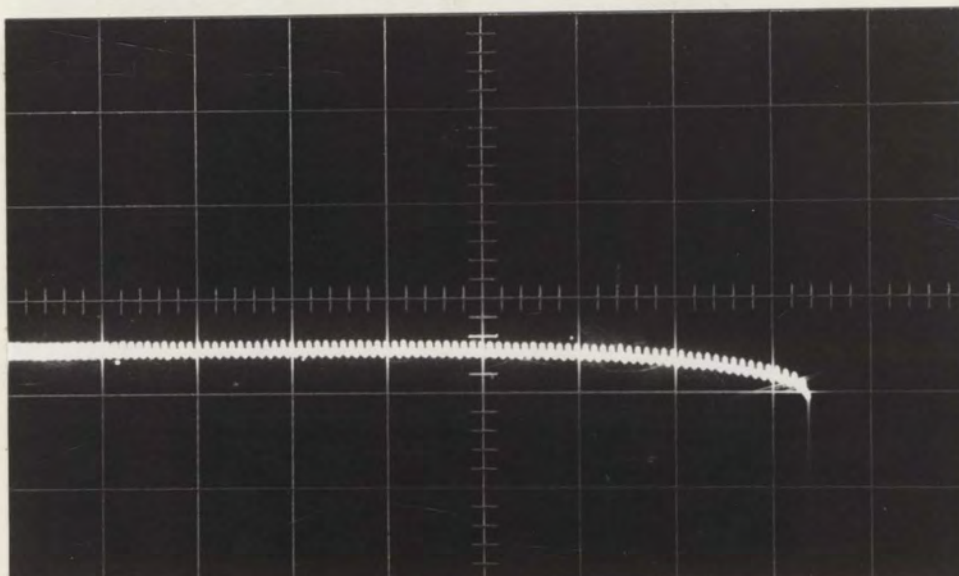
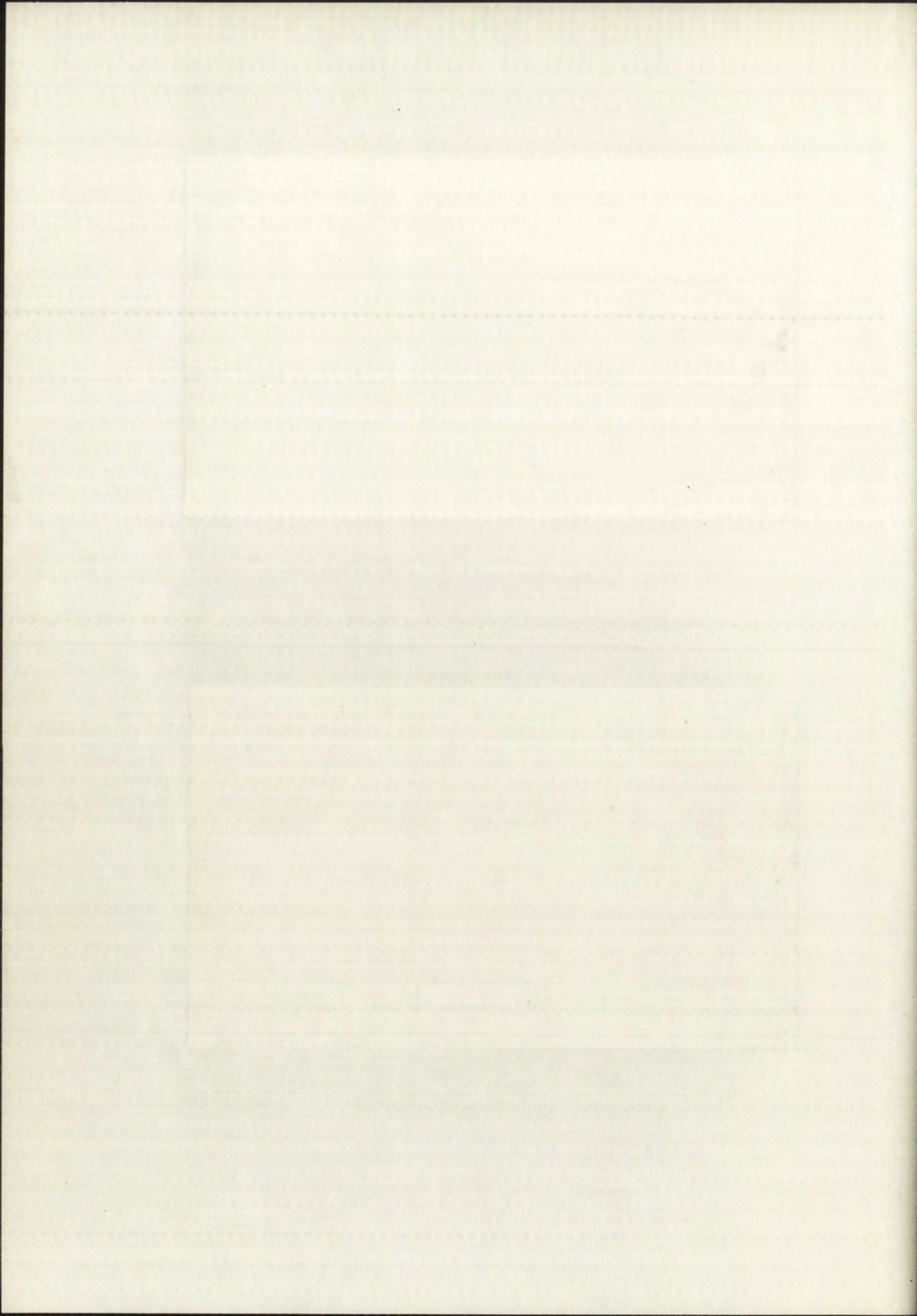


PLATE 6

WAVEFORM OF THE VOLTAGE ACROSS  $D_6$

(D plug-in; 10 mv/cm; 20  $\mu$ s/cm)





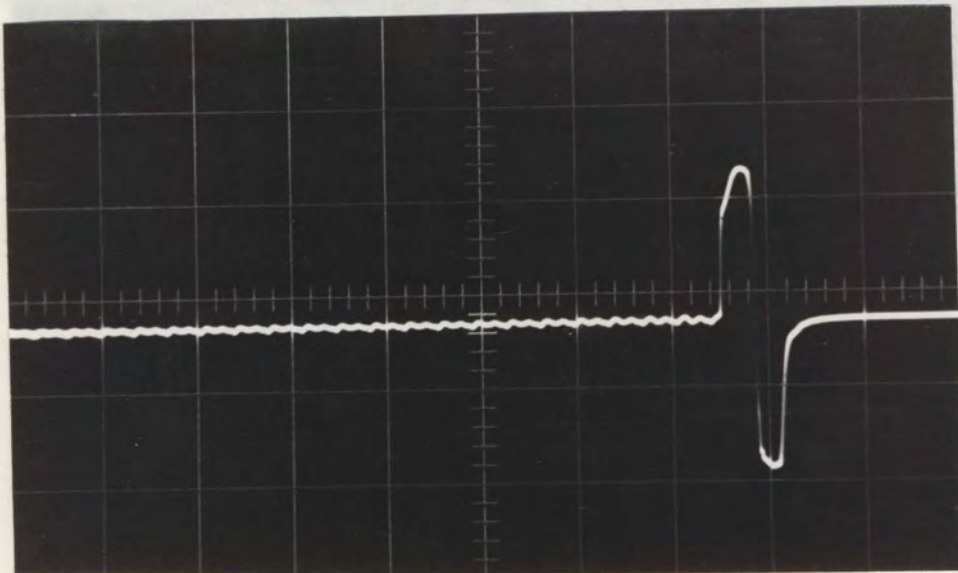


PLATE 7

WAVEFORM AT THE OUTPUT OF THE ZERO DETECTOR

(D plug-in; 5 v/cm; 5  $\mu$ s/cm)

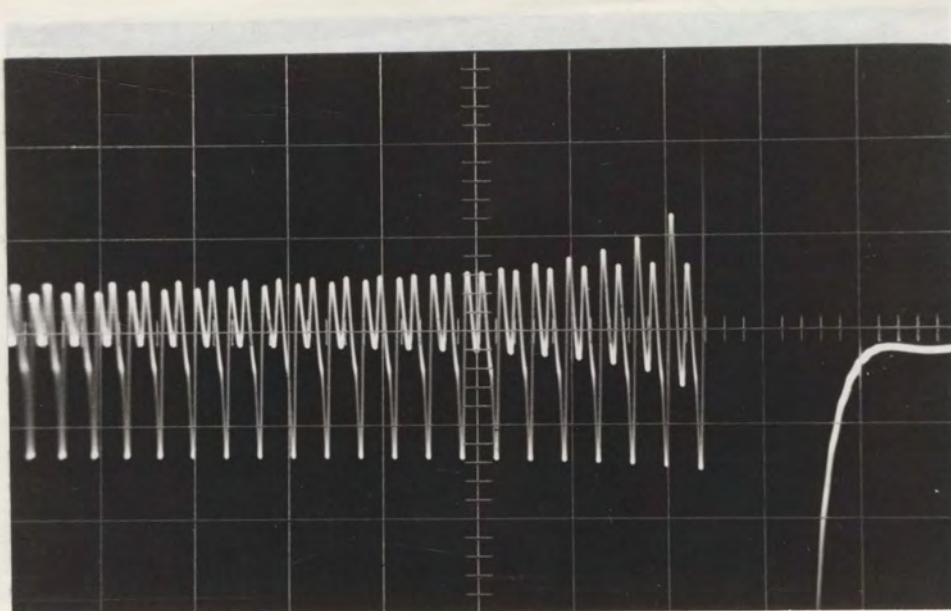
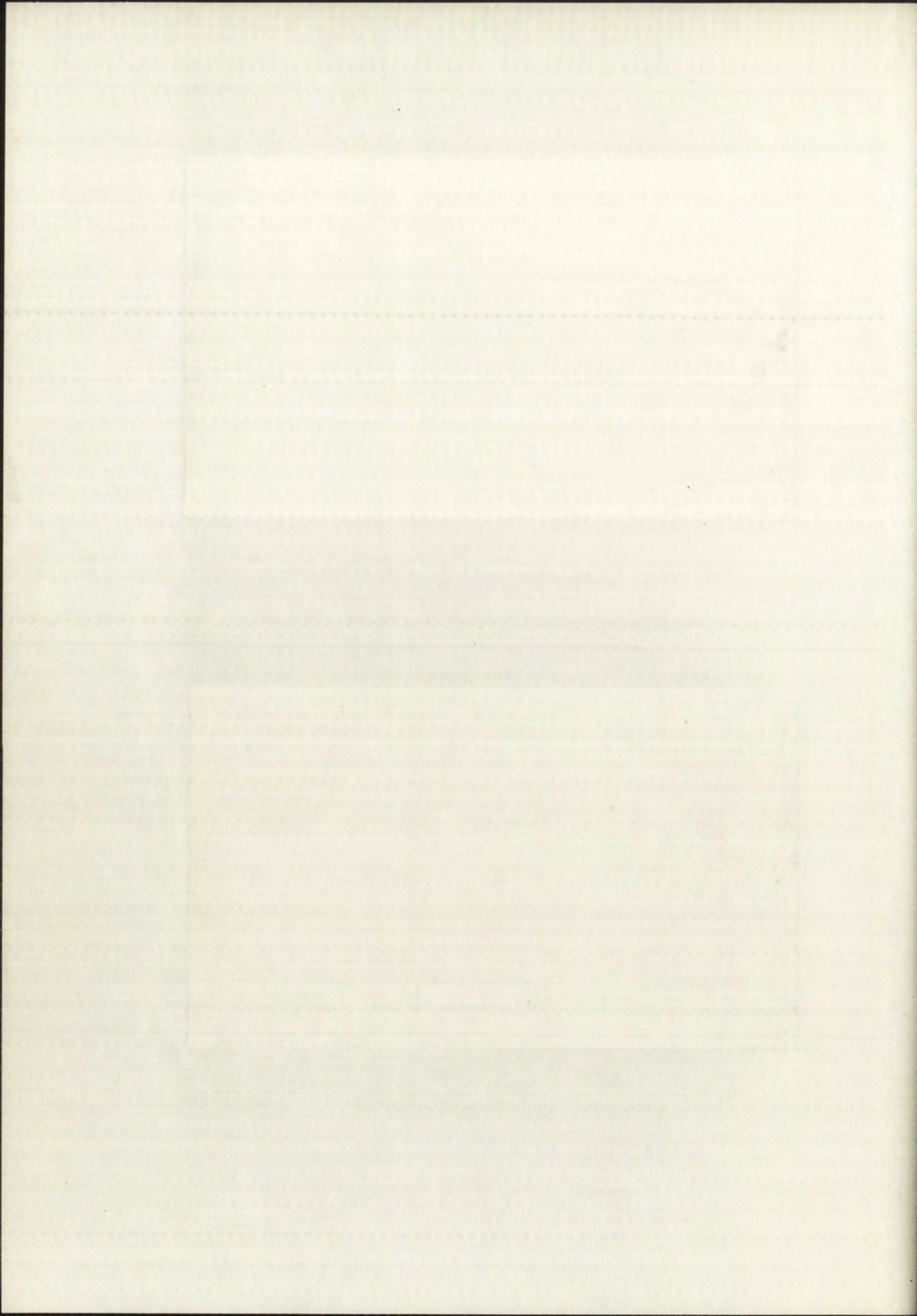


PLATE 8

EXPANDED VIEW OF THE WAVEFORM

AT THE ZERO DETECTOR OUTPUT

(D plug-in; 50 mv/cm; 5  $\mu$ s/cm)





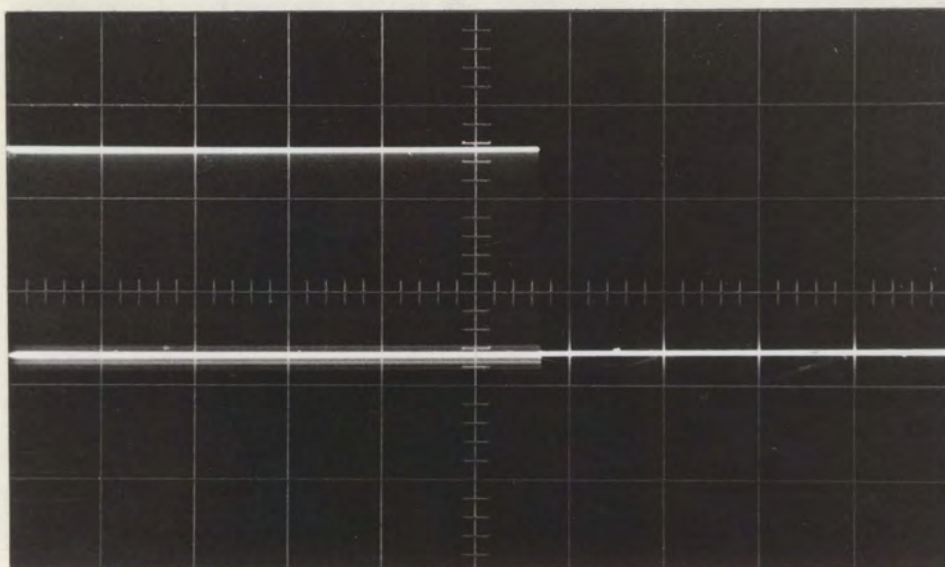


PLATE 9

THE COUNT BURST AT THE COLLECTOR OF  $Q_4$   
 (CA plug-in; 2 v/cm; 200  $\mu$ s/cm)

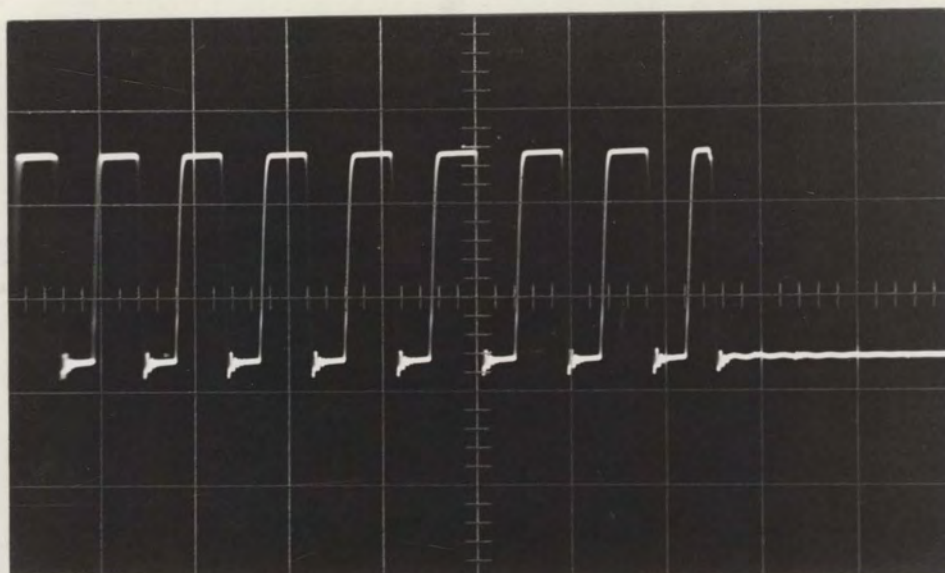
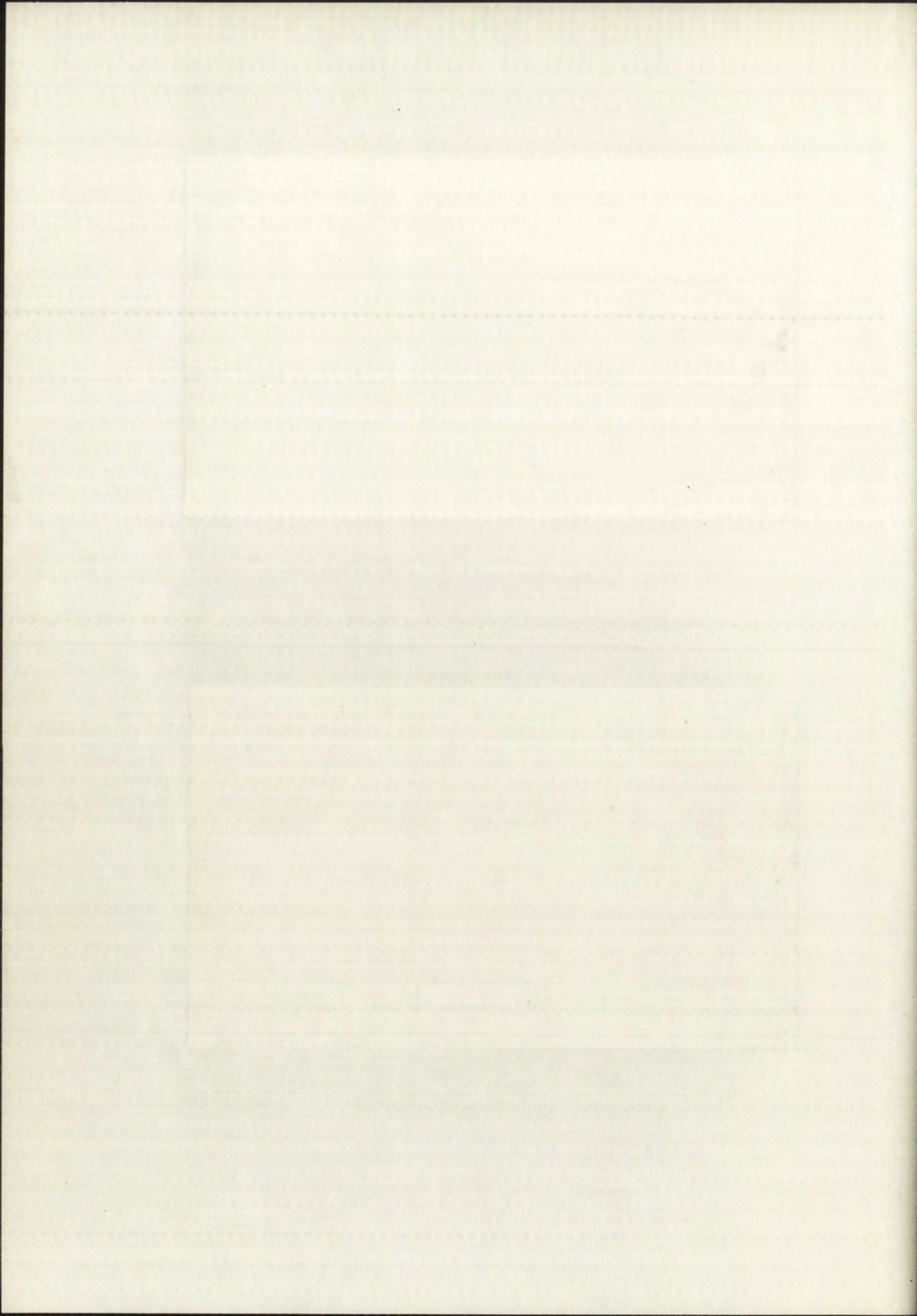


PLATE 10

EXPANDED VIEW OF THE COUNT BURST AT THE COLLECTOR OF  $Q_4$   
 (CA plug-in; 2 v/cm; 2  $\mu$ s/cm)





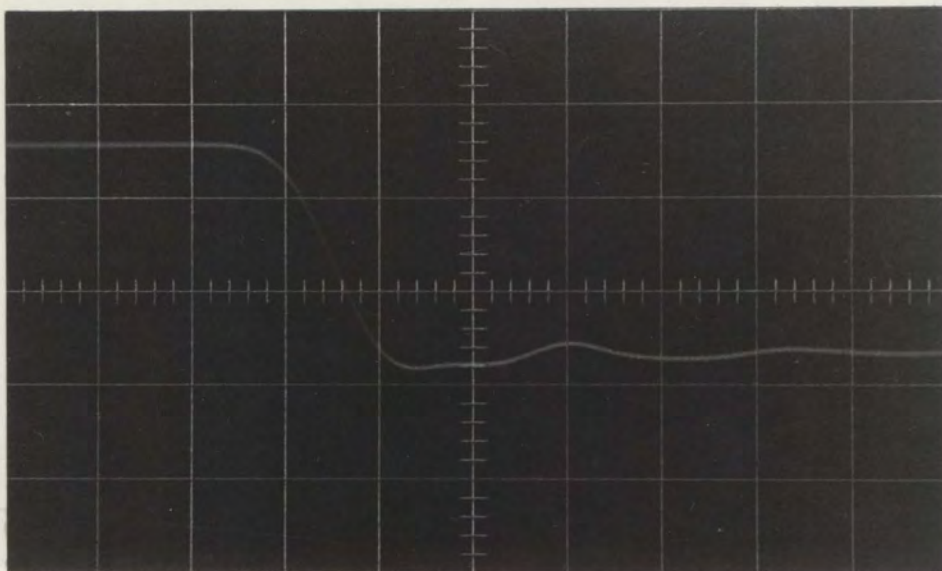


PLATE 11

DETAIL OF THE COUNT BURST AT THE COLLECTOR OF  $Q_4$   
 (CA plug-in; 2 v/cm; .04  $\mu$ s/cm)

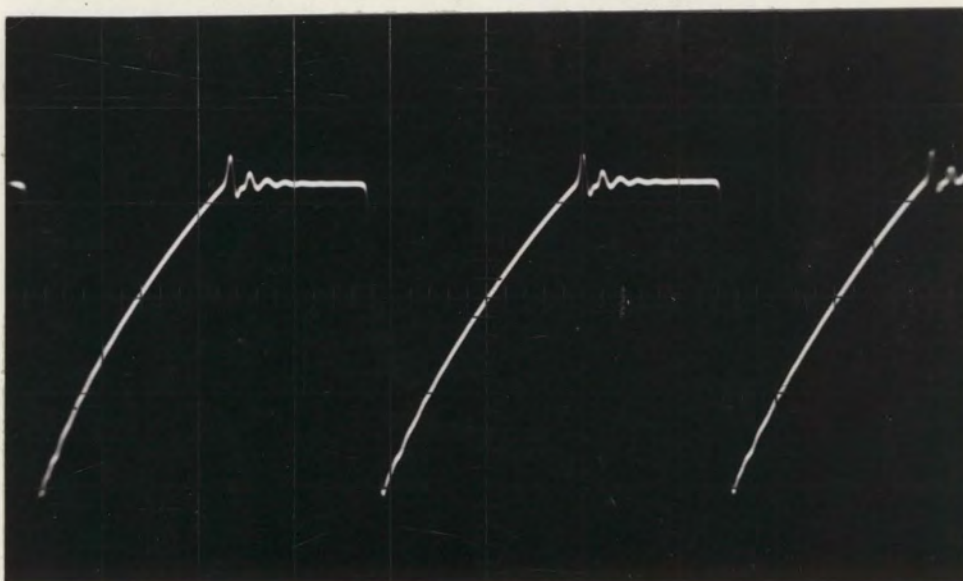
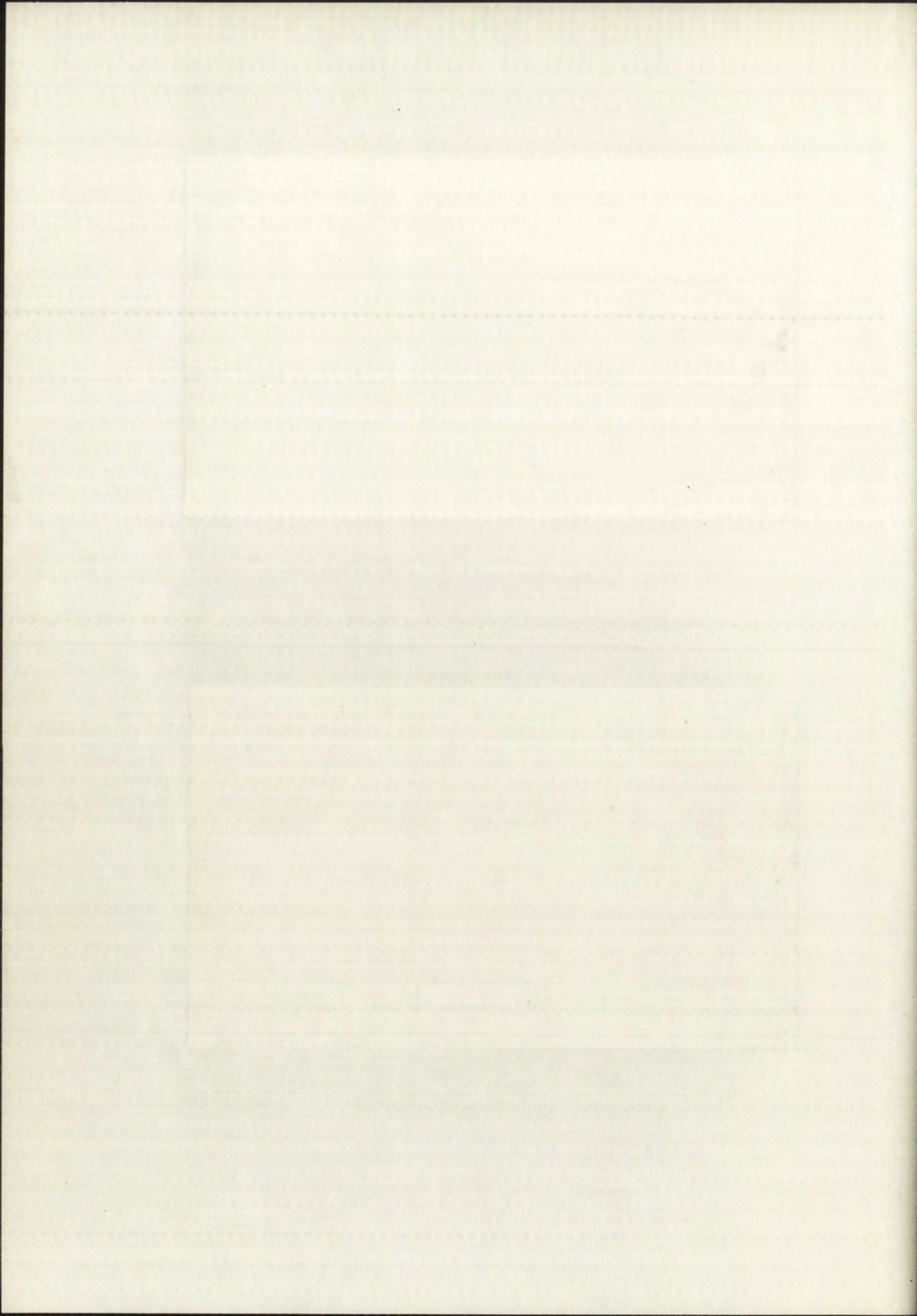


PLATE 12

WAVEFORM AT THE BASE OF  $Q_4$   
 (D plug-in; 2 v/cm; 0.5  $\mu$ s/cm)





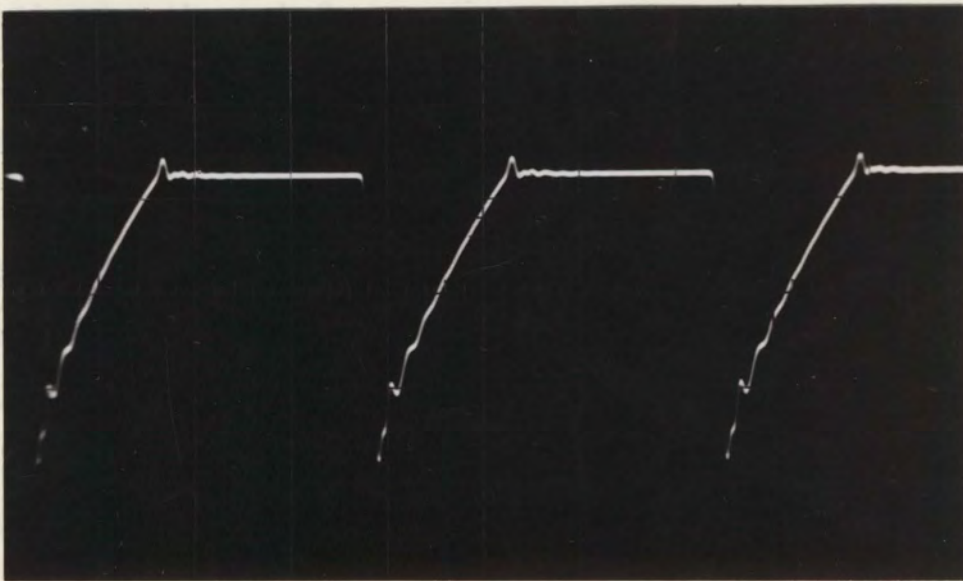


PLATE 13

WAVEFORM OF THE BASE OF  $Q_5$

(D plug-in; 1 v/cm; 0.5  $\mu$ s/cm)

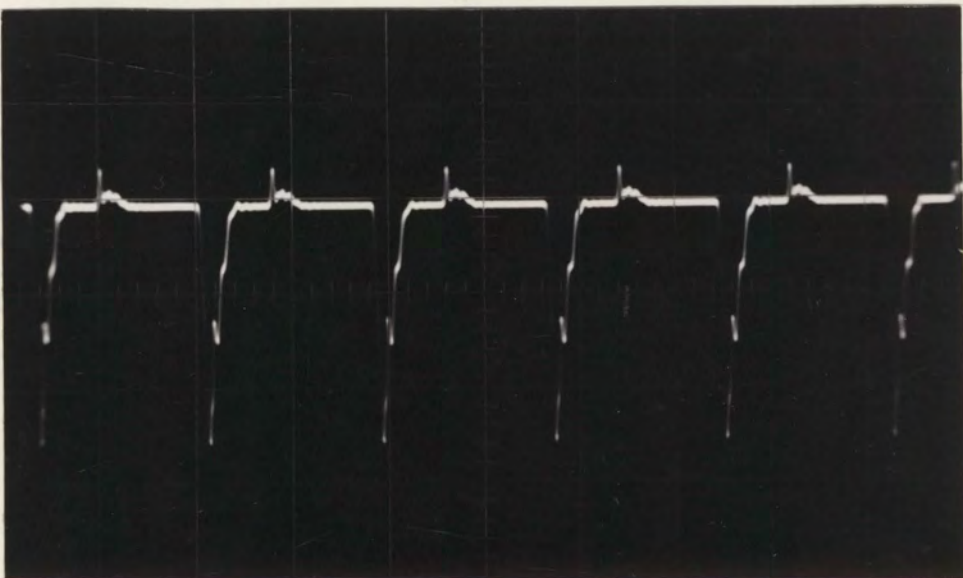
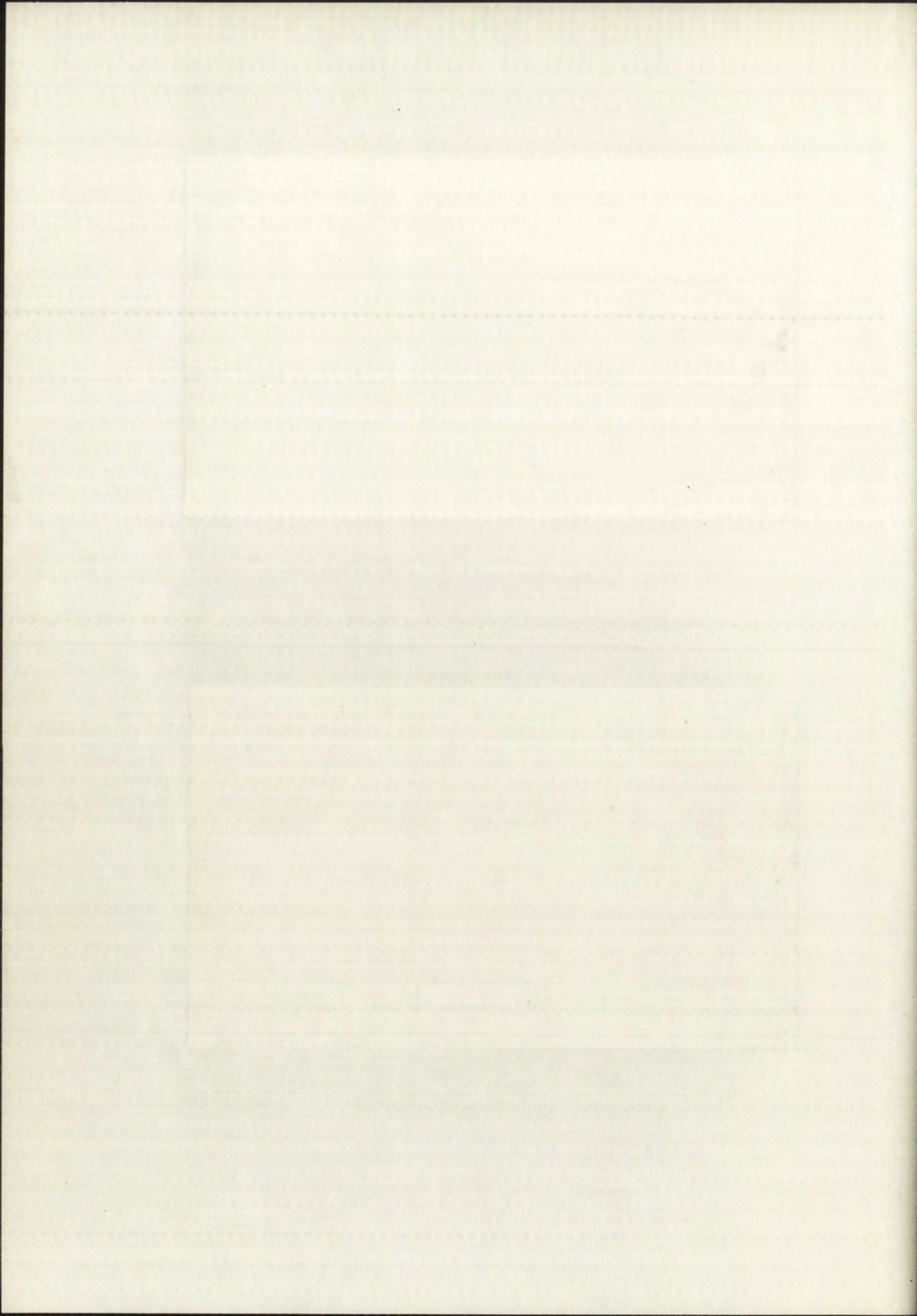


PLATE 14

WAVEFORM AT THE EMITTER OF  $Q_3$

(CA plug-in; 0.5 v/cm; 1  $\mu$ s/cm)





is a detail of the turn-on of  $Q_4$ , during which a pulse of current goes through  $Q_3$ .

Plate 12 is the base waveform of  $Q_4$  ( 13 ). Plate 13 is the base waveform of  $Q_5$  ( 12 ).

The emitter waveform of  $Q_3$  in Plate 14 shows that  $C_2$  charges for approximately one microsecond and discharges for approximately 0.8 microsecond. The period of one cycle is 1.8 microseconds instead of the predicted 2.0 microseconds. This is partially due to the value of  $C_3$  having been 75 mmfd  $\pm 20\%$  instead of the derived value of 78 mmfd. (Plate 14 is referred to again in the report on conversion stability with respect to frequency.)

Conclusions from the general tests. The first series of measurements of noise level show that it might be desirable to filter the supply voltages to hold down the noise level.

The measurements and waveforms taken during the discharge interval show that the model network is performing essentially as expected. None of the minor discrepancies noted here between the actual values and the predicted values should materially affect the operation of the network.

Linearity test procedure. The equipment used was the oscilloscope, the CA plug-in, the potentiometric voltmeter, the counter, and the thermometer. The output of the network was connected to the input of the counter through approximately 18 inches of hook-up wire. The + B Gate pulse from the oscilloscope was used to reset the counter in synchronism

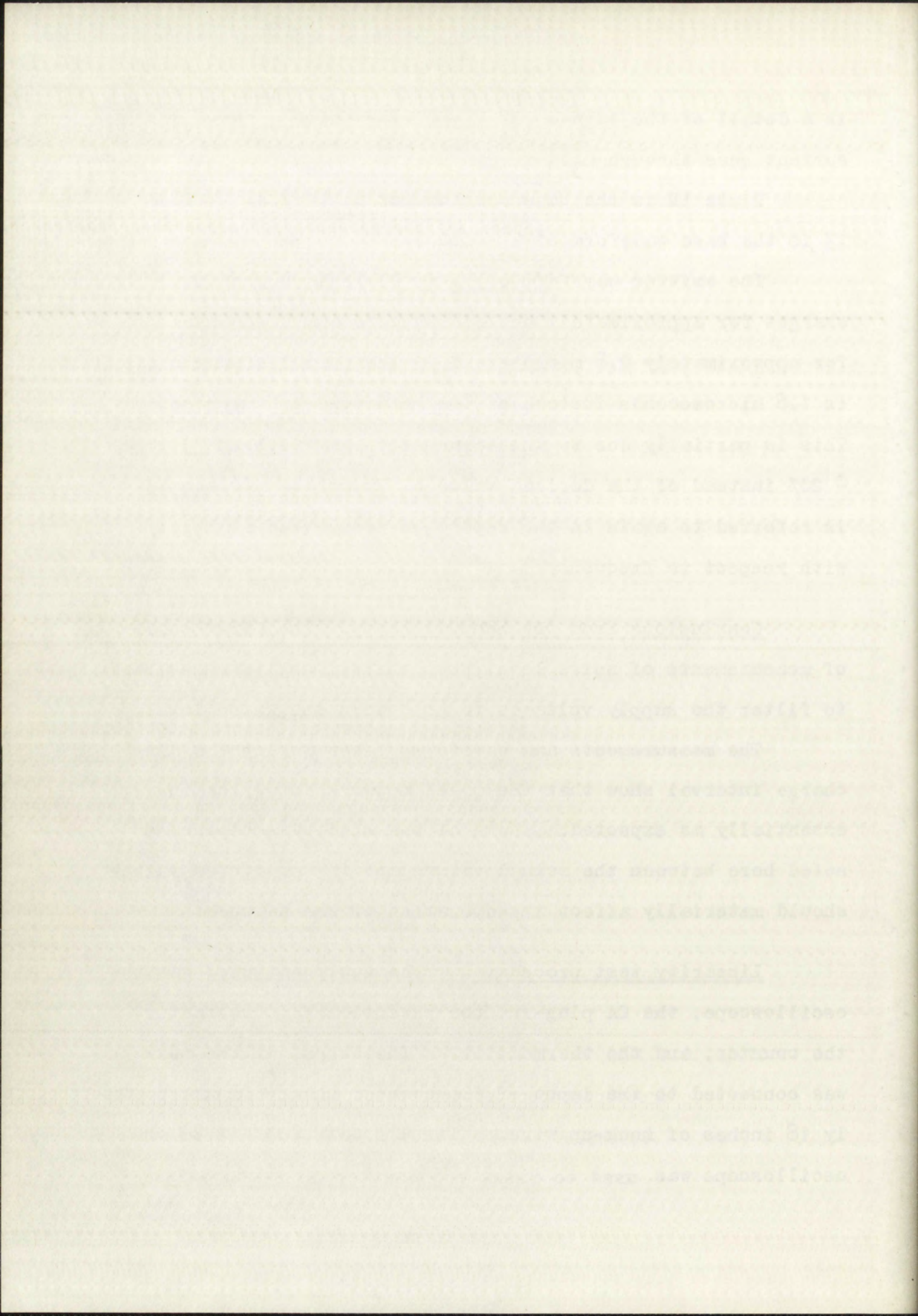




TABLE II

## ROOM TEMPERATURE LINEARITY TEST DATA

Input Voltage *	Count	Input Voltage	Count
0.120	093	1.300	575
0.200	125	1.400	616
0.300	166	1.500	657
0.400	207	1.600	698
0.500	248	1.700	739
0.600	288	1.800	780
0.700	329	1.900	821
0.800	370	2.000	862
0.900	411	2.100	904
1.000	542	2.200	945
1.100	493	2.300	986
1.200	534	2.330	999

\*All voltage settings were within  $\frac{1}{2}$  millivolt of the indicated value.





with the network operation.

The room temperature was 33° centigrade. The repetition rate was 500 cycles per second.

Linearity test results. The linearity test results are shown in Table II. The differential count was consistently 41 counts for every 100 millivolts increase of the input voltage with two exceptions: when the voltage was changed from 0.500 volts to 0.600 volts, the differential count was 40 counts; when the input voltage was changed from 2.000 volts to 2.100 volts, the differential count was 42 counts.

Linearity test conclusions. Fig. 17 is a plot of the count deviation from a straight line versus input voltage over the range of 0.200 to 2.3 volts.

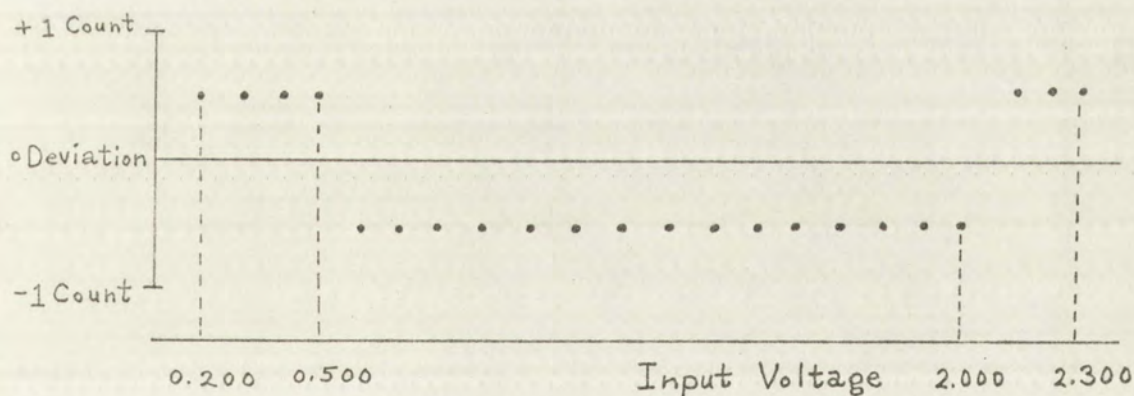


FIGURE 17

#### COUNT DEVIATION FROM STRAIGHT LINE LINEARITY

The maximum deviation from perfect linearity is then  $\pm\frac{1}{2}$  count

with the network operated.  
 The room temperature was 20°C.  
 The input rate was 200 cycles per second.  
 The frequency test results.  
 The results in Table II. The differential count rate  
 counts per second for every 100 millivolts increase of the  
 input voltage with two exceptions: when the voltage was  
 changed from 0.200 volts to 0.300 volts, the differential  
 count was 40 counts; when the input voltage was changed  
 from 0.300 volts to 0.400 volts, the differential count was  
 40 counts.

Linearity test results. The results in Table III.  
 The count deviation from a straight line versus input voltage  
 also over the range of 0.200 to 0.400 volts.

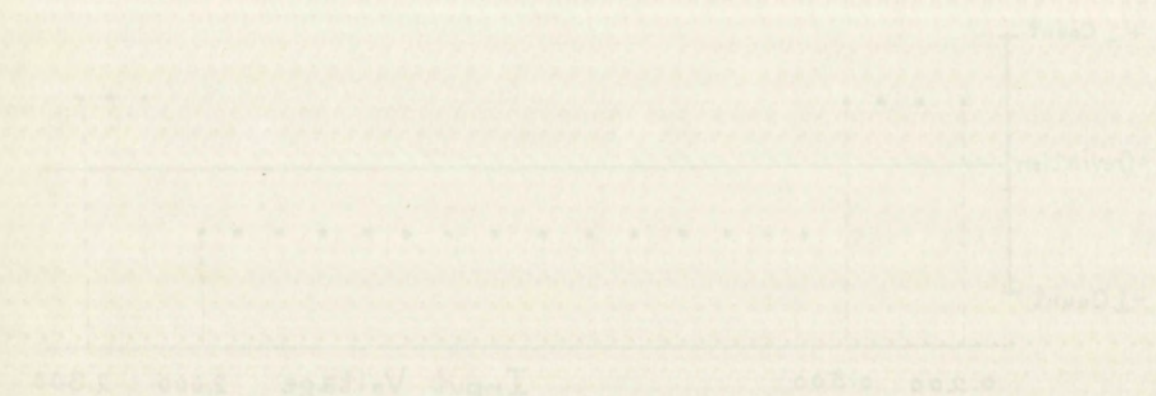


FIGURE 17

COUNT DEVIATION FROM STRAIGHT LINE LINEARITY

The count deviation from perfect linearity is then 40 counts



which corresponds to 0.05% of full scale.

Leakage test procedure and test results. To determine if any significant leakage was present, the delay time was increased and the output count was observed. The initial attempt showed no change when the output was 999 counts and the delay time was increased by 120 microseconds. It was then determined that the transition between counts of 998 and 999 occurred over an input voltage change of 0.20 millivolts. The input voltage was adjusted to the center of this transition range and the delay time was again increased by 120 microseconds while the model network was operating at approximately ten conversions per second. Again, no change could be observed; the counts of 998 and 999 continued to occur with equal frequency. This was done several times with extreme care being exercised to be sure no compensating effects were being introduced.

Leakage test conclusions. The above test gave no apparent indication of leakage effects being present. The test was capable of clearly indicating a change of 0.10 millivolt on the storage capacitor, had leakage occurred during the 120 microsecond increase in delay. From the relation

$$\Delta V = \frac{i \Delta t}{C}$$

the leakage was less than  $25 \times 10^{-9}$  amperes.

which corresponds to 2.5% of full scale.

Initial test conditions and test results.

It was anticipated that the delay time was

increased and the output time was observed. The initial

delay time was observed by the microsecond. It was

then determined that the transition between counts of 500 and

599 occurred over an input voltage change of 0.50 millivolts.

The input voltage was adjusted to the center of this transition

and the delay time was again increased by 150

microseconds while the model network was operating at approx-

imately 100 conversions per second. Again, no change could

be observed. The count of 599 was then adjusted to occur with

equal frequency. This was done several times with extreme

care being exercised to be sure no compensating effects were

being introduced.

Leakage test conditions. The above test gave no

apparent indication of leakage effects being present. The

test was capable of clearly indicating a change of 0.10

millivolt on the storage capacitor, had leakage occurred.

During the 150 microsecond increase in delay, from the

rotation

$$\Delta V = \frac{Q}{C}$$

the leakage was less than  $25 \times 10^{-9}$  coulombs.



Conversion stability with respect to frequency. The

stability of conversion with respect to frequency was tested by changing the values of  $C_3$  and  $C_4$ . The input voltage was initially adjusted to give an output of 999 counts. When  $C_3$  was increased from 100 mmfd to 175 mmfd, the conversion time changed from 1800 microseconds to 2400 microseconds, and the output count changed from 999 to 989. The increase in  $C_4$  caused the charge time of  $C_2$  to increase, which may account for the change. The waveform of Plate 14 (on page 73) indicates that  $C_2$  reached essentially full charge during the original charge period. Another explanation of the cause of the change may be that the increase in  $C_4$  changed the rise time of the signal at the collector of  $Q_4$ , and, because of the effect of  $R_8$  in "bleeding off" some of the charge from  $C_2$ , a decrease in rise time caused a decrease in count due to less charge being lost through  $R_8$ . The apparent change in  $\Delta Q$  is approximately  $7.5 \times 10^{-13}$  coulombs. While  $Q_3$  is conducting,  $R_8$  is conducting 0.2 ma. If the current impulse through  $Q_3$  lasts 0.1 microseconds, during that time,  $R_8$  will bleed off approximately  $2 \times 10^{-11}$  coulombs. From this it is apparent that only a 4% decrease in the duration of the current pulse is necessary to account for the observed change in the output count. The rise time of the square wave was observed closely when  $C_4$  was increased and a small change was evident.

Comparison of results with respect to frequency.

Stability of the system with respect to frequency was tested

by measuring the output of the system at various frequencies.

Results are shown in Figure 1. The output of the system

is shown to be constant over the frequency range of 0 to 100 Hz.

It is noted that the output of the system is constant over the frequency range of 0 to 100 Hz.

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The output of the system is shown to be constant over the frequency range of 0 to 100 Hz.



## III. TEMPERATURE TESTS

Temperature test procedure. The temperature test procedure was similar to the procedure of the linearity test, except that for these tests the model network was placed inside the temperature chamber (item 9 page 62) during the tests. Dry ice was placed inside the temperature chamber to cool the chamber for the tests of the model at  $-5^{\circ}$  centigrade. The model was also tested inside the chamber at  $25^{\circ}$  centigrade and  $55^{\circ}$  centigrade.

Temperature test results. The test results consist of two sets of input - output data. The first set, shown in Table III, relates the input voltages and the output counts at  $-5^{\circ}$  centigrade,  $25^{\circ}$  centigrade, and  $55^{\circ}$  centigrade using a zero temperature coefficient capacitor (NPO) for  $C_2$ . The second set, shown in Table IV, was recorded with the same conditions except that  $C_2$  was a minus 750 ppm/ $^{\circ}$  C temperature coefficient capacitor (NPZ).

The output readings at 0.500 volts input and 2.000 volts input were used to compute the average resolution for each set of data and to compute the input voltage required to give zero count. The results of the computations are given in Table V on page 81.

Temperature test conclusions. The test results show that the zero point is reasonably stable, having changed approximately 4 counts over a range of  $60^{\circ}$  centigrade. The difference in average temperature coefficients





TABLE III

TEMPERATURE TEST DATA OF MODEL NETWORK  
USING A NPO CAPACITOR FOR  $C_2$

INPUT VOLTAGE	-5°C	25°C	55°C
0.120	75	75	75
0.200	111	108	108
0.300	158	154	152
0.400	205	197	192
0.500	245	236	229
0.800	366	351	340
1.100	486	467	452
1.400	607	582	563
1.700	728	698	675
2.000	850	813	787
2.300	971	929	899
2.368	999		
2.483		999	
2.569			999

TABLE IV

TEMPERATURE TEST DATA OF MODEL NETWORK  
USING A NPZ CAPACITOR FOR  $C_2$

INPUT VOLTAGE	-5°C	25°C	55°C
0.120	76	78	81
0.200	112	114	116
0.300	161	163	164
0.400	209	209	206
0.500	250	249	248
0.800	373	371	369
1.100	496	493	490
1.400	620	616	611
1.700	744	738	732
2.000	867	860	852
2.300	991	983	973
2.318	999		
2.340		999	
2.366			999

TABLE III

TEMPERATURE DATA ON WATER NETWORK  
DURING A TWO EXHAUSTION TEST

TIME, MIN.	TEMPERATURE, °C	TEMPERATURE, °C	TEMPERATURE, °C
0	10.0	10.0	10.0
10	10.0	10.0	10.0
20	10.0	10.0	10.0
30	10.0	10.0	10.0
40	10.0	10.0	10.0
50	10.0	10.0	10.0
60	10.0	10.0	10.0
70	10.0	10.0	10.0
80	10.0	10.0	10.0
90	10.0	10.0	10.0
100	10.0	10.0	10.0
110	10.0	10.0	10.0
120	10.0	10.0	10.0
130	10.0	10.0	10.0
140	10.0	10.0	10.0
150	10.0	10.0	10.0
160	10.0	10.0	10.0
170	10.0	10.0	10.0
180	10.0	10.0	10.0
190	10.0	10.0	10.0
200	10.0	10.0	10.0
210	10.0	10.0	10.0
220	10.0	10.0	10.0
230	10.0	10.0	10.0
240	10.0	10.0	10.0
250	10.0	10.0	10.0
260	10.0	10.0	10.0
270	10.0	10.0	10.0
280	10.0	10.0	10.0
290	10.0	10.0	10.0
300	10.0	10.0	10.0

TABLE IV

TEMPERATURE DATA ON WATER NETWORK  
DURING A TWO EXHAUSTION TEST

TIME, MIN.	TEMPERATURE, °C	TEMPERATURE, °C	TEMPERATURE, °C
0	10.0	10.0	10.0
10	10.0	10.0	10.0
20	10.0	10.0	10.0
30	10.0	10.0	10.0
40	10.0	10.0	10.0
50	10.0	10.0	10.0
60	10.0	10.0	10.0
70	10.0	10.0	10.0
80	10.0	10.0	10.0
90	10.0	10.0	10.0
100	10.0	10.0	10.0
110	10.0	10.0	10.0
120	10.0	10.0	10.0
130	10.0	10.0	10.0
140	10.0	10.0	10.0
150	10.0	10.0	10.0
160	10.0	10.0	10.0
170	10.0	10.0	10.0
180	10.0	10.0	10.0
190	10.0	10.0	10.0
200	10.0	10.0	10.0
210	10.0	10.0	10.0
220	10.0	10.0	10.0
230	10.0	10.0	10.0
240	10.0	10.0	10.0
250	10.0	10.0	10.0
260	10.0	10.0	10.0
270	10.0	10.0	10.0
280	10.0	10.0	10.0
290	10.0	10.0	10.0
300	10.0	10.0	10.0



TABLE V  
SUMMARY OF TEMPERATURE TEST RESULTS

TEMPERATURE	-5°C		25°C		55°C	
C <sub>2</sub>	NPO	NPZ	NPO	NPZ	NPO	NPZ
MAXIMUM DEVIATION FROM A STRAIGHT LINE (COUNTS)	$\pm\frac{1}{2}$	$\pm\frac{1}{2}$	$\pm\frac{1}{2}$	$\pm\frac{1}{2}$	$\pm 1$	$\pm\frac{1}{2}$
ZERO POINT (VOLTS)	-.105	-.106	-.114	-.110	-.115	-.116
RESOLUTION (MV/COUNT)	2.479	2.431	2.600	2.455	2.688	2.483
AVERAGE TEMP. COEFF. (%/°C)			.134	0.034		

TABLE V  
SUMMARY OF TEMPERATURE TEST RESULTS

TEMPERATURE	-8°C		-25°C		-55°C	
	WFO	WIX	WFO	WIX	WFO	WIX
MAXIMUM DEVIATION FROM A STRAIGHT LINE (COUNTS)	25	25	25	15	25	25
ZERO POINT (VOLTS)	-1.05	-1.05	-1.15	-1.10	-1.15	-1.15
SENSITIVITY (REV/COUNT)	2.475	2.431	2.400	2.457	2.325	2.457
AVERAGE TEMP. CORP. (°C)			1.38	0.031		



caused by charging  $C_2$  is 1000 parts per million per degree centigrade, which is larger than the expected change of 750 parts per million per degree centigrade. The linearity of conversion was quite satisfactory over the temperature range.

#### IV. SUMMARY OF TEST CONCLUSIONS

The results of all of the tests indicate that the model network performs essentially as was expected. The differences between the predicted values and the measured values of the delay time and the resolution can be accounted for as a result of errors in the assumed values of  $V_S$  and  $V_R$ . The linearity tests gave excellent results; the observed error is within the linearity specification of the test equipment. The temperature tests show that temperature compensation of the network can be readily accomplished; a higher value of  $V_R$  would simplify that procedure.

## CHAPTER VI

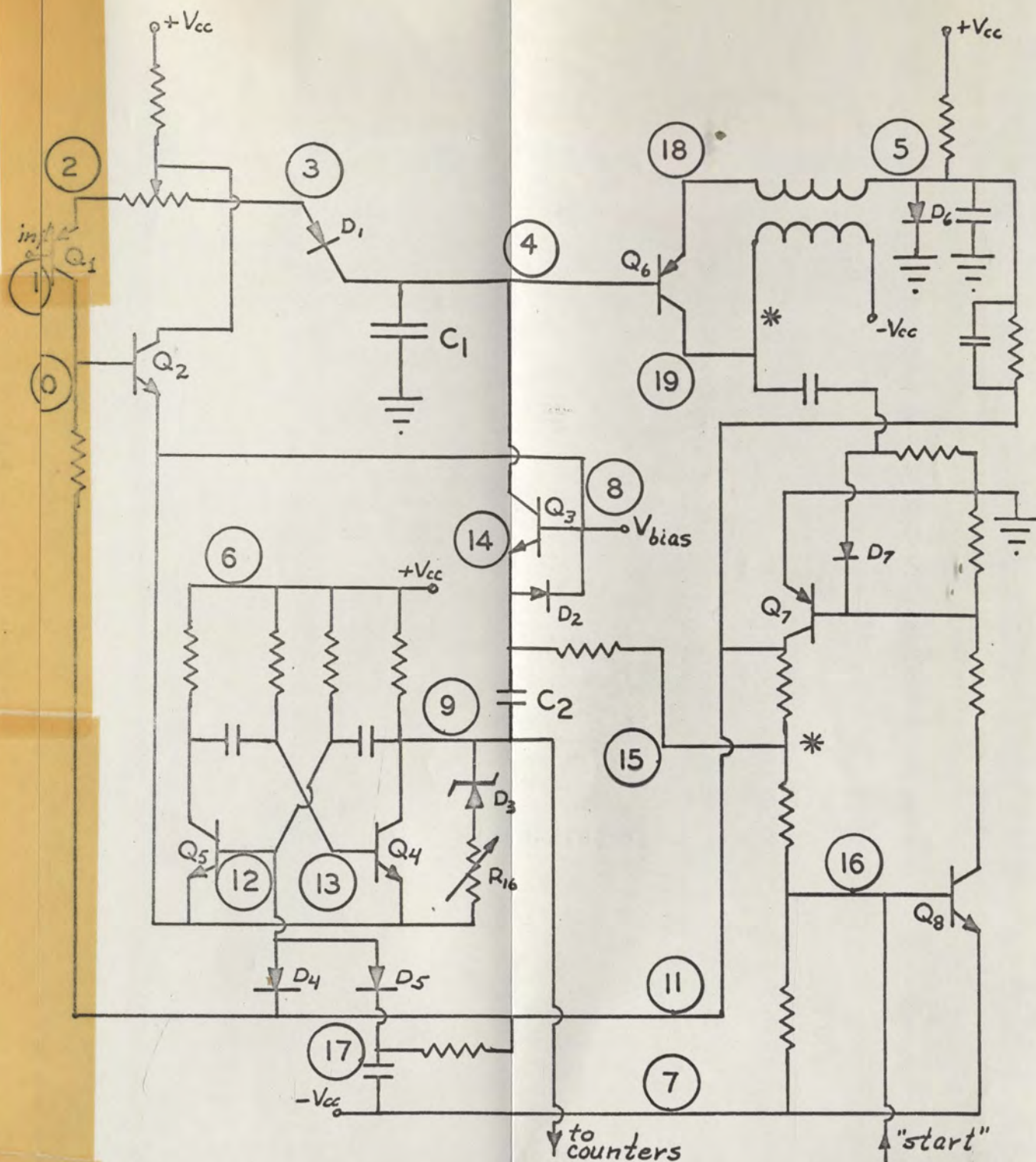
### CONCLUSIONS

The purpose of this chapter is to summarize the results of the study and to discuss the implications of the findings. The study was designed to investigate the effects of various factors on the performance of the system. The results show that the system is capable of performing the required tasks under a wide range of conditions. The findings suggest that the system is robust and reliable, and that it can be used in a variety of applications.

### 1. EVALUATION

The approach to analog-to-digital conversion and digital-to-analog conversion is evaluated in this chapter. The results show that the approach is effective and efficient, and that it can be used in a variety of applications. The evaluation is based on a comparison of the results of the study with the results of other studies. The results of the study show that the approach is superior to other approaches in terms of accuracy, speed, and reliability. The results also show that the approach is easy to use and that it can be adapted to a wide range of applications. The findings suggest that the approach is a valuable tool for the design and implementation of analog-to-digital and digital-to-analog conversion systems.





\* changes - see  
page 57

FIGURE 18

CIRCUIT TEST POINTS

-- ANALOG-TO-DIGITAL CONVERSION NETWORK





## CHAPTER VI

### CONCLUSIONS

The purpose of this chapter is to summarize the principle advantages and limitations of the new approach to conversion and the network designed and tested in the preceding chapters and to propose research problems for future investigations.

#### I. EVALUATION

The approach to analog-to-digital conversion. The approach to analog-to-digital conversion can produce a simple conversion network with creditable specifications as was demonstrated by the model network.

Utilization of this approach can yield converters that are mechanically strong. The implementation of this approach does not require fragile components.

The test results reported in chapter five show that the model network using this approach has good resolution and excellent linearity. Accuracy is dependent on zero stability, linearity, and the constancy of the resolution. Future studies to improve the zero stability are necessary if high accuracy is to be achieved.





The conversion network. The conversion network contains a small number of components and is simple to build, test, and align. The network contains no fragile parts. The tests of the model network showed that the network was operating approximately as expected. The linearity of the model network was 0.05%. The resolution was approximately 2.5 millivolts per count. Tests on the definition of the edge of each count showed that it would be possible to achieve a resolution of less than one millivolt. Another advantage of this network, as shown in some of the waveform plates, is that the output count represents the voltage that was present when the conversion started.

A limiting factor in the network is the zero detector. As the resolution is decreased, the time during which the zero detector contributes current to the storage capacitor before triggering is increased; this feature limits the practical sensitivity that is attainable. Any radical increase in sensitivity will require a radical change in the zero detector circuit.

The results of the tests of conversion stability with respect to frequency indicate the need for a change in the bias circuit in the emitter of  $Q_3$ .

Although good temperature compensation was not achieved, the results of the temperature compensation tests did agree essentially with the predictions; consequently,

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the thirtieth is the question of the



it is reasonable to assume that good temperature compensation can be achieved. The work of actually accomplishing the temperature compensation remains to be done.

As can be seen from the above most of the original objectives of the study have been accomplished. To that extent the program has been successful. However, there remains some work that could be done to improve the conversion network.

## II. RESEARCH PROBLEMS FOR FUTURE INVESTIGATION

Improvements on the existing network. The suggestions for future work to further improve the existing network are in the areas of further simplification, increased stability, and increased sensitivity.

Studies of further simplification could be directed toward combining various circuits to perform the same functions with fewer components. One possibility is to use the multivibrator in the discharge circuit to provide the function of a control flip-flop. Another possibility might be to combine the zero detector and the control flip-flop.

To increase stability and sensitivity a study should be made to improve the zero detector. The advantages and disadvantages involved in using a more complex circuit such as the multiar [6b] should be explored. The type of zero detector used in this thesis can be improved by specifically





designing a transistor-transformer combination for this service. If such a design is undertaken, the discharge circuit should be examined to see if the current pulse could be changed to improve the zero detector response.

Related applications. The following research problems utilizing this approach to conversion in other related applications are proposed. This approach to conversion can readily be extended to multiplexed applications. Other programs could include studies using this approach for transient peak detection, voltage sampling, bi-polar voltage measurement, and current measurement.

Although this concludes the program described in chapter one, the results of the program warrant the undertaking of other programs intended to further develop the potentials in this approach to analog-to-digital conversion.

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## APPENDIX

ALPHABET



## APPENDIX

### SELECTED DIGITAL-TO-ANALOG NETWORKS

The known literature on various digital-to-analog networks presents a rigorous and comparatively complex derivation of element values [ 22 ]. The purpose of this appendix is to present simplified methods of deriving element values. Two forms of digital-to-analog networks are discussed. The first form is the series network or ladder adder. The series network relations for a binary adder will be derived from two different approaches. The second form is the shunt network. Only linear networks are considered.

#### I. SERIES NETWORK FORM I

The network shown in Fig. 19 illustrates the series network configuration. The network is assumed to repeat indefinitely on both sides of the figure. The desired operation is such that actuating only  $S_0$  causes a voltage  $E_0$  to appear at the output terminal, and actuating only  $S_n$  will cause a voltage of  $E_0/2^n$  to appear at the output. From the principle of superposition, actuating more than one switch will cause the appearance of the sum of the voltages attributable to the actuation of each switch. Due to the

## APPENDIX

### RELATIONSHIP BETWEEN DIGITAL AND ANALOG NETWORKS

..... has been discussed in various digital-to-analog

networks presents a rigorous and comparatively complex

derivation of element values (22). The purpose of this

appendix is to present simplified methods of deriving

element values. Two forms of digital-to-analog networks

are discussed. The first form is the series network of

ladder stages. The series network relations for a binary

value will be derived from two different approaches. The

second form is the shunt network. Only ladder networks

are considered.

#### 1. SERIES NETWORK FORM

The network shown in Fig. 19 illustrates the series

network configuration. The network is assumed to represent

resistively on both sides of the ladder. The desired

operation is such that actuating only  $S_0$  causes a voltage

$V_0$  to appear at the output terminal, and actuating only  $S_1$

will cause a voltage of  $V_0/2$  to appear at the output. From

the principle of superposition, actuating more than one

switch will cause the appearance of the sum of the voltages

attributable to the actuation of each switch. Due to the



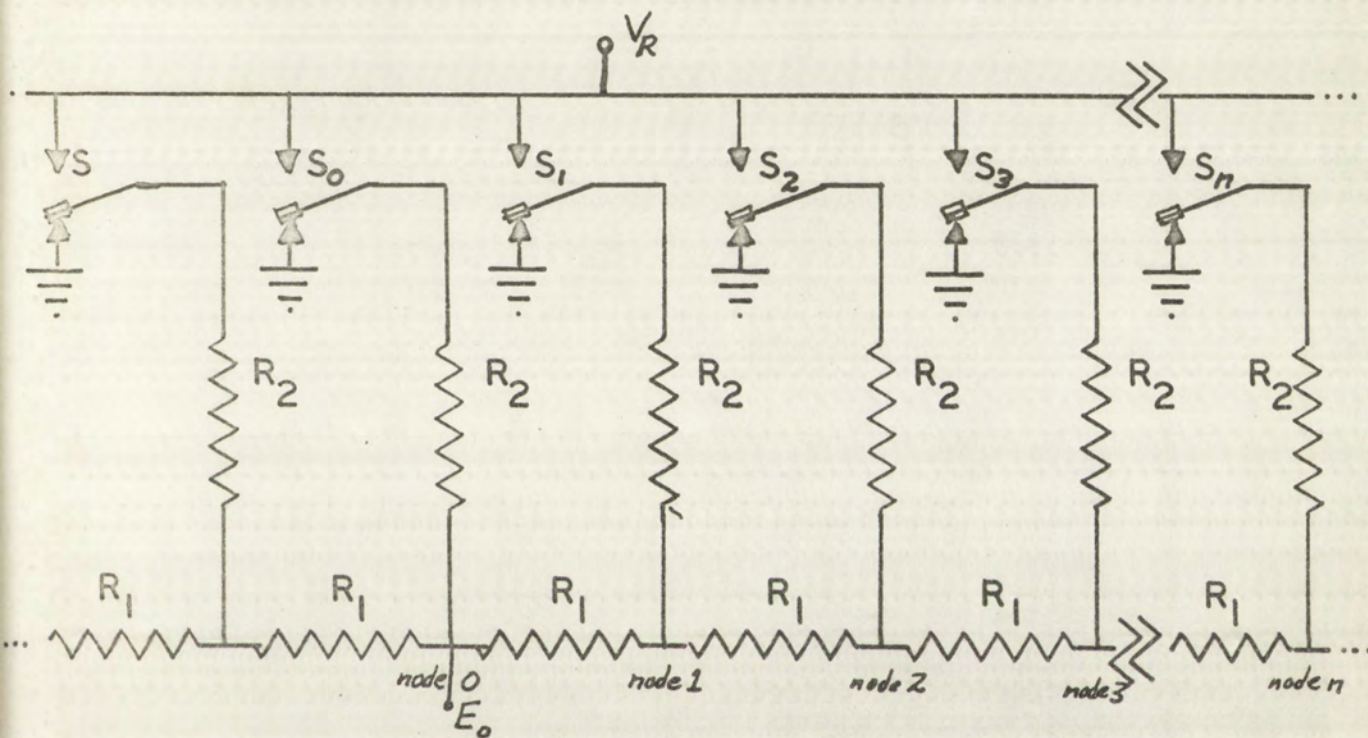


FIGURE 19  
SERIES NETWORK



FIGURE 10  
SERIES NETWORK



symmetry of the network, if a voltage is impressed on only one node of the network, one-half that voltage will appear at the adjacent nodes and the voltage at the  $n^{\text{th}}$  node will be  $\frac{1}{2^n}$  times the voltage at the source node.

Derivation I, form I. The voltage at node zero in Fig. 19 is  $E_0$ . Then  $E_1 = E_0/2$ ,  $E_2 = E_0/4 \dots E_n = E_0/2^n$ . The current that flows through the resistor between node zero and node 1 is equal to the sum of all the currents flowing to ground on the right side of node zero in the figure. The sum of the ground currents ( $I_T$ ) is

$$\begin{aligned}
 I_T &= \frac{E_0}{\frac{2}{R_2}} + \frac{E_0}{\frac{4}{R_2}} + \dots \frac{E_0}{\frac{2^n}{R_2}} & (19) \\
 &= \frac{E_0}{R_2} \left( \frac{1}{2} + \frac{1}{4} + \frac{1}{8} \dots \frac{1}{2^n} + \dots \right) \\
 &= \frac{E_0}{R_2}
 \end{aligned}$$

The voltage drop across this resistor is

$$\begin{aligned}
 E_0 - \frac{E_0}{2} &= \frac{E_0}{2} & (20) \\
 \therefore R_1 &= \frac{\frac{E_0}{2}}{\frac{E_0}{R_2}} = \frac{R_2}{2}
 \end{aligned}$$

$$\text{or } R_2 = 2R_1$$

every node of the network, it is possible to express the voltage at each node in terms of the voltages at the nodes adjacent to it. The voltage at the node will be the average of the voltages at the nodes adjacent to it.

Let us assume that the voltage at the node is  $V_i$ . The voltage at the node will be the average of the voltages at the nodes adjacent to it. The current that flows through the resistor between node  $i$  and node  $j$  is equal to the sum of all the currents flowing to ground on the right side of node  $i$ . The sum of the ground currents ( $I_g$ ) is

$$I_g = \frac{E_0}{R_0} + \frac{E_1}{R_1} + \frac{E_2}{R_2} + \dots + \frac{E_n}{R_n}$$

the voltage drop across this resistor is

$$V_i - V_j = \frac{I_g R_{ij}}{S_{ij}}$$



The voltage at node zero is  $E_0$  and, from Equation 19, the total current flowing into the right side of the network is  $\frac{E_0}{R_2}$ . The Thevenin equivalent resistance ( $R_{Th}$ ) of the network is then

$$R_{Th} = \frac{E_0}{\frac{E_0}{R_2}} = R_2 \quad (21)$$

This means that the network may be terminated at any point on the right side of Fig. 19 if a terminating resistor of value  $R_2$  is connected from the last node to ground.

Derivation 2, form 1. Referring to Fig. 19, because the network is repetitive and infinite, the Thevenin impedance looking into the network to the right of any node is the same regardless of the node chosen. This impedance will be referred to as  $R_{Th}$ . If a voltage,  $E_0$ , is impressed on node zero, the network to the right of node zero can be replaced by the equivalent network of Fig. 20.

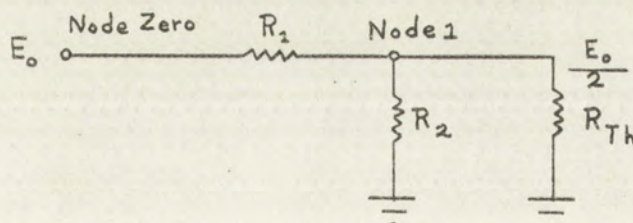


FIGURE 20

EQUIVALENT SERIES NETWORK





In order for the required voltage ratio to exist,

$$\frac{R_2 R_{Th}}{R_2 + R_{Th}} = R_1 \quad (22)$$

and, since the network to the right of node zero must represent an impedance of  $R_{Th}$ ,

$$R_1 + \frac{R_2 R_{Th}}{R_2 + R_{Th}} = R_{Th} \quad (23)$$

Solving for  $R_{Th}$

$$R_{Th} = 2R_1$$

and from Equation 22

$$R_2 = 2R_1$$

as was previously derived.

## II. SHUNT NETWORK FORM 2

The shunt network is shown in Fig. 21. Element values are specified as conductances for algebraic simplicity. The operation of this network is such that actuating switch  $S_n$  causes a voltage equal to  $\frac{E_0}{2^n}$  to appear at the output. The principle of superposition applies here also; therefore, combinations of switches give additive outputs.

If only  $S_0$  is actuated, the output voltage is  $E_0$  and the network is equivalent to Fig. 22.

In order for the network to be able to

(19)

and, since the network is the sum of all the

networks of the network.

It is possible to find a network which is

the sum of all the networks of the network.

It is possible to find a network which is

the sum of all the networks of the network.

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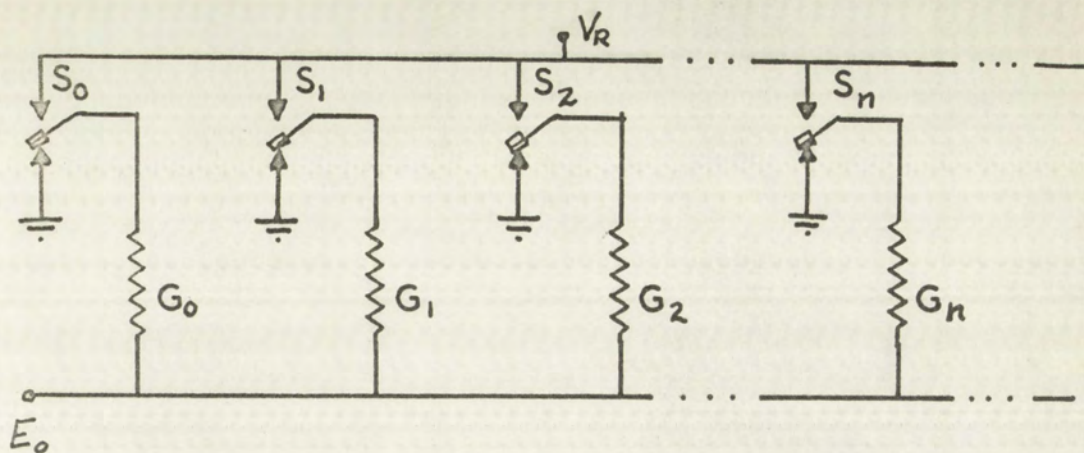


FIGURE 21  
SHUNT NETWORK

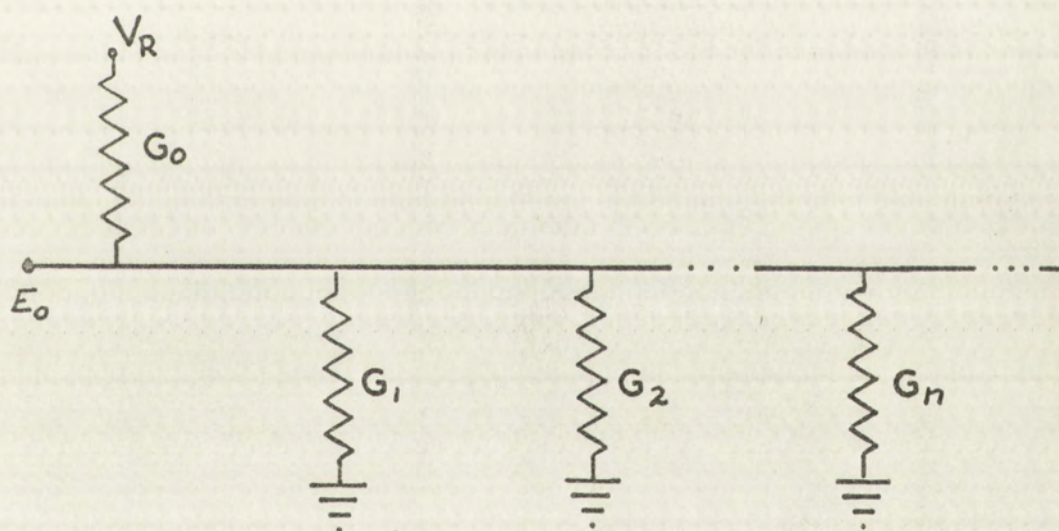


FIGURE 22  
EQUIVALENT SHUNT NETWORK



FIGURE 21  
SHUNT NETWORK



FIGURE 22  
EQUIVALENT SHUNT NETWORK



Defining  $G_T = \sum_{n=0}^{\infty} G_n$

$$E_0 = \frac{V_R G_0}{G_T}$$

If only  $S_1$  is actuated,

$$E_1 = \frac{E_0}{2} = \frac{V_R G_1}{G_T}$$

Combining and solving

$$G_0 = 2G_1 \quad (24)$$

In like manner

$$G_0 = 2^n G_n \quad (25)$$

The resistors to the right of  $G_n$  in Fig. 22 have the values

$$G_{n+1} = \frac{G_n}{2}$$

$$G_{n+2} = \frac{G_n}{4}$$

...

$$G_{n+m} = \frac{G_n}{2^m}$$

If the network is terminated following  $G_n$ , the value of the terminating resistor is

$$\frac{1}{R_T} = G_n \left( \frac{1}{2} + \frac{1}{4} + \dots + \frac{1}{2^m} + \dots \right) \quad (26)$$

$$R_T = R_0 (2^n)$$

$R_0$  = the resistor connected to  $S_0$ , hence  $R_0 = \frac{1}{G_0}$

Letting  $C_1 = \frac{1}{s}$

It only  $Z_1$  is required.

$$Z_1 = \frac{C_1}{1 + C_1 Z_2}$$

Combining and solving

$$C_1 = \frac{1}{s}$$

in like manner

$$C_2 = \frac{1}{s} \quad C_3 = \frac{1}{s} \quad C_4 = \frac{1}{s}$$

The resistors to the right of  $C_1$  in Fig. 23 have the values

$$\begin{aligned} R_1 &= \frac{C_1}{C_1 + 1} \\ R_2 &= \frac{C_2}{C_2 + 1} \\ &\dots \\ R_n &= \frac{C_n}{C_n + 1} \end{aligned}$$

is the network is terminated following  $C_n$ , the value

of the terminating resistor is

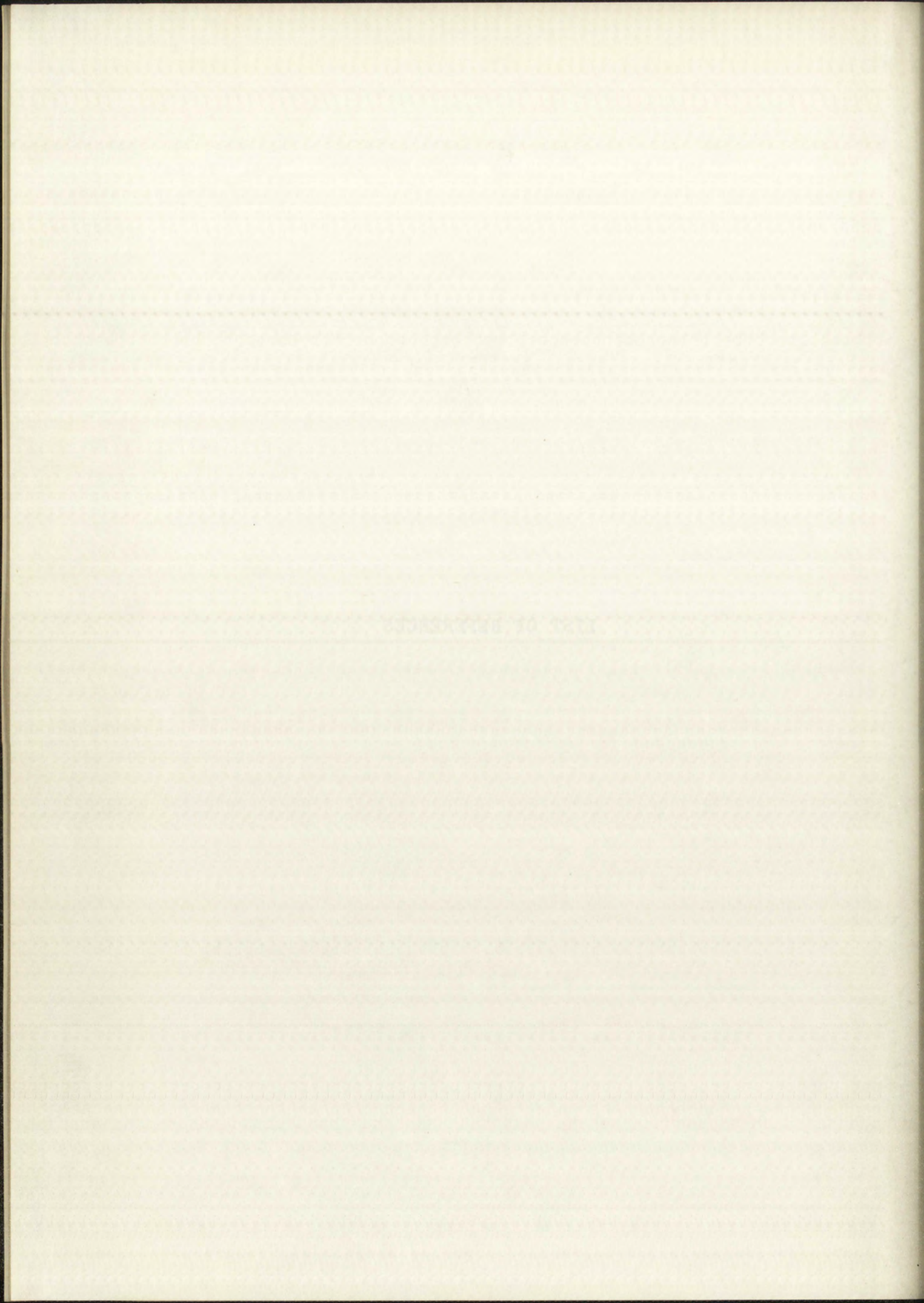
$$\frac{1}{R_T} = \frac{1}{R_n} + \frac{1}{R_{n-1}} + \dots + \frac{1}{R_1} \quad (24)$$

$$R_T = \frac{1}{\frac{1}{R_n} + \frac{1}{R_{n-1}} + \dots + \frac{1}{R_1}}$$

the resistor connected to  $C_n$  hence  $R_T = \frac{1}{\frac{1}{R_n} + \frac{1}{R_{n-1}} + \dots + \frac{1}{R_1}}$



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