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A Binary-To-Decimal Converter

Samuel D. Stearns

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A BINARY-TO-DECIMAL CONVERTER

by

Samuel D. Stearns

A Thesis

In partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering.

The University of New Mexico

1957

This thesis, directed and approved by the candidate's committee, has been accepted by the Graduate Committee of the University of New Mexico in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

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A BINARY-TO-DECIMAL CONVERTER

CHAPTER 1. INTRODUCTION AND SUMMARY DESCRIPTION

Introduction

This paper describes a device which electronically converts a binary number into its decimal equivalent. Such a device might be of use in digital computers, many of which use the binary number system, and also in similar machines, such as pulse code modulated data collectors.

The binary-to-decimal converter described here was designed specifically for use in Sandia Corporation's High-Speed Digital Recording and Data-Handling System, which actually uses the Gray code rather than the binary number system. However, conversion from Gray to binary (see Appendix B) is simple, and a binary-to-decimal converter seems much simpler than a Gray-to-decimal converter.

The converter is designed to have a parallel input of 7 binary bits, representing any number from 0 to 127. Extension of the converter to more bits is easy. Its output is presented on neon lights, representing the decimal equivalent of the input as shown in Fig. 1.1. The output is in lights because this converter is used as an indicating device; however, the output voltages could also be used to drive other memory or recording systems.

The converter is designed to make conversions at any rate from 0 to about 100 conversions/sec. When used in the Sandia Corporation data system mentioned previously, it will run at about 25 conversions/sec.

It seems reasonable that a design at least similar to the one used here might already have been built. However, a search of all available literature has not revealed any similar device either proposed or in use.

CHAPTER 1. INTRODUCTION AND BACKGROUND

This paper describes a device which automatically converts a binary number into its decimal equivalent. This is done by using a series of digital adders, which are connected in a chain. The first adder takes the binary number and adds it to a constant value of 1. The result is then passed to the next adder, which adds it to another constant value of 1. This process continues until the final adder, which produces the decimal equivalent of the binary number. The device is designed to be simple and reliable, and it can be used in a variety of applications where binary numbers need to be converted to decimal.

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It is important to note that the device is designed to be simple and reliable, and it can be used in a variety of applications where binary numbers need to be converted to decimal. It consists of a series of digital adders, which are connected in a chain. The first adder takes the binary number and adds it to a constant value of 1. The result is then passed to the next adder, which adds it to another constant value of 1. This process continues until the final adder, which produces the decimal equivalent of the binary number. The device is designed to be simple and reliable, and it can be used in a variety of applications where binary numbers need to be converted to decimal.

<u>Hundreds</u>	<u>Tens</u>	<u>Units</u>
1-☼	☼9	☼9
	☼8	☼8
	☼7	☼7
	☼6	☼6
	☼5	☼5
	☼4	☼4
	☼3	☼3
	☼2	☼2
	☼1	☼1
	☼0	☼0

Fig. 1.1 -- Output of Converter is in Lights Which Represent
Decimal Equivalent of Input

Following this introduction is a summary and general description of the converter, designed to give the reader an idea of how it works in a minimum of reading time.

Following the summary is an account of some of the methods for binary-to-decimal conversion, to show why the particular design used was chosen. Finally, there is a detailed description of the circuit operation of the converter.

Summary Description

In order to change a 7-bit binary number to its decimal equivalent, this converter first changes the binary number (N) to its two's complement ($2^n - N$, where $n = 7$ in this case). The converter then stores the two's complement in seven flip-flop stages.

After the two's complement of N, or $128-N$, has been stored, an oscillator begins to increase this quantity in storage, one unit at a time. The oscillator continues to increase the number in storage until the number reaches 128; then the oscillator stops. In order to increase the number in storage to 128, the oscillator has put out a number of pulses equal to the difference between 128 and the two's complement of N, or

$$128 - (128-N), \text{ or } N$$

Thus the oscillator puts out a number of pulses exactly equal to the number represented by the binary input to the converter. These pulses from the oscillator are also fed into a decade scaler which is capable of counting up to 127. The decade scaler then displays the number N in decimal form on direct-reading neon lights.

The entire converter (less power supply) uses 21 vacuum tubes, including twenty 5963 twin triodes and one 6CL6 pentode. Power requirements are as follows:

B+ — 250-300 v dc	at 80 ma
Fil. — 6.3 v ac	at 6.65 a

While, as mentioned, this converter was built specifically for use with the Sandia Corporation High Speed Digital Recording and Data Handling System, it may also be used for output and display purposes in digital computers which use the binary system. A photograph of the converter is shown in Fig. 1.2.

 

Fig. 1.2 -- A Binary-to-Decimal Converter

CHAPTER 2. METHODS FOR BINARY-TO-DECIMAL CONVERSION

The problem of finding the simplest and best circuit to perform even a moderately complicated logical function, such as binary-to-decimal conversion, is usually not simple or straightforward. The logical function can be described precisely in Boolean algebra,¹ but the Boolean expressions can be manipulated in various ways, and many different circuits can be built which will satisfy a single Boolean expression. Nevertheless, it is helpful to express the function in Boolean algebra first, and then to investigate various ways of mechanizing the function.

1. For an explanation of Boolean algebra, see Richards, R. K., Arithmetic Operations in Digital Computers, D. Van Nostrand Company, 1955.

CHAPTER 2. THE LOGIC OF THE ALGEBRA OF SETS

The problem of finding the algebra and logic of sets is a problem of great importance. The algebra of sets is a branch of algebra which deals with the properties of sets and the operations on them. The logic of sets is a branch of logic which deals with the properties of sets and the operations on them. The algebra of sets is a branch of algebra which deals with the properties of sets and the operations on them. The logic of sets is a branch of logic which deals with the properties of sets and the operations on them.

Method 1

This binary-to-decimal converter must accept an input (parallel in time) of a 7-bit binary number N , which will be denoted by

$$N = B_1 B_2 B_3 B_4 B_5 B_6 B_7 ,$$

where B_1 is the most significant bit, having weight 64, and B_7 is the least significant bit, having weight 1. Thus, if

$$N = 1010100 ,$$

where $B_1=1$, $B_2=0$, $B_3=1$, $B_4=0$, $B_5=1$, $B_6=0$, and $B_7=0$, then N represents the decimal number 84.

Likewise, the output will be denoted by

$$N = D_1 D_2 D_3 ,$$

where D_1 is the most significant decimal digit and D_3 the least significant decimal digit.

To express the function of the converter, the output must be written as a Boolean function of the input. But Boolean expressions can contain only variables with two possible values, so first the output must be re-expressed. To do this, the double-subscript notation is used for the D 's, the first subscript denoting the decade and the second subscript the unit within the decade. Thus the expression

$$N = D_{10} D_{28} D_{34}$$

means that N has the value 084. Note also that, for instance, if $D_{34} = 1$, then $D_{30}=D_{31}=D_{32}=D_{33}=D_{35}=D_{36}=D_{37}=D_{38}=D_{39}=0$ necessarily. Furthermore, D_{12} , D_{13} , D_{14} , D_{15} , D_{16} , D_{17} , D_{18} , and D_{19} are always 0, because it is impossible to have an input N greater than 127.

The Boolean equations for the D 's as functions of the B 's will now be given and simplified as much as possible. D_1 will be expressed first, then D_2 , and finally D_3 . These equations may be derived by inspection of Table 2.1.

The above-mentioned expression may be written in the form of a first class
 and $\mathbf{A}$, which will be denoted by

$$\mathbf{A} = \mathbf{A}_1 + \mathbf{A}_2 + \mathbf{A}_3$$

where $\mathbf{A}_1$ is the most significant bit, having weight 2^0 , and $\mathbf{A}_2$ is the least significant bit,
 having weight 2^{n-1} .

$$\mathbf{A} = \mathbf{A}_1 + \mathbf{A}_2 + \mathbf{A}_3$$

where $\mathbf{A}_1$ is the most significant bit, having weight 2^0 , and $\mathbf{A}_2$ is the least significant bit,
 having weight 2^{n-1} .

Similarly, the output will be denoted by

$$\mathbf{B} = \mathbf{B}_1 + \mathbf{B}_2 + \mathbf{B}_3$$

where $\mathbf{B}_1$ is the most significant bit, having weight 2^0 , and $\mathbf{B}_2$ is the least significant bit,
 having weight 2^{n-1} .

To express the function of the structure, the output must be written as a Boolean function
 of the input. But Boolean expressions may contain only variables with two possible values, so
 first the output must be re-expressed. To do this, the double-valued notation is used for
 the $\mathbf{B}_i$, the first subscript denoting the i th bit, and the second subscript denoting the i th bit within the
 double. Then the expression

$$\mathbf{B} = \mathbf{B}_1 + \mathbf{B}_2 + \mathbf{B}_3$$

may be written as the value $\mathbf{B}_i$. Note also that, for instance, if $\mathbf{B}_1 = 1$, then $\mathbf{B}_1 = 1$,
 $\mathbf{B}_2 = 0$, $\mathbf{B}_3 = 0$, etc. For example, if $\mathbf{B}_1 = 1$, $\mathbf{B}_2 = 1$, $\mathbf{B}_3 = 0$, then $\mathbf{B}_1 = 1$, $\mathbf{B}_2 = 1$, $\mathbf{B}_3 = 0$,
 and so on. It is impossible to have an input $\mathbf{B}$ greater than 2^n .

The Boolean expression for the $\mathbf{B}_i$ as a function of the $\mathbf{A}_i$ will now be given and simplified
 as much as possible. $\mathbf{B}_1$ will be expressed first, then $\mathbf{B}_2$, and finally $\mathbf{B}_3$. These expressions may
 be derived by inspection of Table III.

Table 2.1 -- BINARY AND DECIMAL NUMBERS

Bin
0001000

Dec

Decimal	Binary	Decimal
0	B 1234567	0
1	0000000	1
2	0000001	2
3	0000010	3
4	0000011	4
5	0000100	5
6	0000101	6
7	0000110	7
8	0000111	8
9	0001000	9
10	0001001	10
11	0001010	11
12	0001011	12
13	0001100	13
14	0001101	14
15	0001110	15
16	0001111	16
17	0010000	17
18	0010001	18
19	0010010	19
20	0010011	20
21	0010100	21
22	0010101	22
23	0010110	23
24	0010111	24
25	0011000	25
26	0011001	26
27	0011010	27
28	0011011	28
29	0011100	29
30	0011101	30
31	0011110	31
32	0011111	32
33	0100000	33
34	0100001	34
35	0100010	35
36	0100011	36
37	0100100	37
38	0100101	38
39	0100110	39
40	0100111	40
41	0101000	41
42	0101001	42
43	0101010	43
44	0101011	44
45	0101100	45
46	0101101	46
47	0101110	47
48	0101111	48
49	0110000	49
50	0110001	50
51	0110010	51
52	0110011	52
53	0110100	53
54	0110101	54
55	0110110	55
56	0110111	56
57	0111000	57
58	0111001	58
59	0111010	59
60	0111011	60
61	0111100	61
62	0111101	62
63	0111110	63
64	0111111	64
65	1000000	65
66	1000001	66
67	1000010	67
68	1000011	68
69	1000100	69
70	1000101	70
71	1000110	71
72	1000111	72
73	1001000	73
74	1001001	74
75	1001010	75
76	1001011	76
77	1001100	77
78	1001101	78
79	1001110	79
80	1001111	80
81	1010000	81
82	1010001	82
83	1010010	83
84	1010011	84
85	1010100	85
86	1010101	86
87	1010110	87
88	1010111	88
89	1011000	89
90	1011001	90
91	1011010	91
92	1011011	92
93	1011100	93
94	1011101	94
95	1011110	95
96	1011111	96
97	1100000	97
98	1100001	98
99	1100010	99
100	1100011	100
101	1100100	101
102	1100101	102
103	1100110	103
104	1100111	104
105	1101000	105
106	1101001	106
107	1101010	107
108	1101011	108
109	1101100	109
110	1101101	110
111	1101110	111
112	1101111	112
113	1110000	113
114	1110001	114
115	1110010	115
116	1110011	116
117	1110100	117
118	1110101	118
119	1110110	119
120	1110111	120
121	1111000	121
122	1111001	122
123	1111010	123
124	1111011	124
125	1111100	125
126	1111101	126
127	1111110	127
	1111111	127

1900

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REVENUE DEPARTMENT AND STAMPS - A. I. 1900:

REVENUE DEPARTMENT AND STAMPS - A. I. 1900:

REVENUE DEPARTMENT AND STAMPS - A. I. 1900:

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1. D_1 , the "hundreds" digit.

$$\begin{aligned} D_{10} &= \bar{B}_1 + B_1 \bar{B}_2 + B_1 B_2 \bar{B}_3 \bar{B}_4 \bar{B}_5 \\ &= \bar{B}_1 + \bar{B}_2 + \bar{B}_3 \bar{B}_4 \bar{B}_5 \end{aligned} \quad (2.1)$$

$$\begin{aligned} D_{11} &= B_1 B_2 B_3 + B_1 B_2 \bar{B}_3 B_4 + B_1 B_2 \bar{B}_3 \bar{B}_4 B_5 \\ &= B_1 B_2 (B_3 + \bar{B}_3 B_4 + \bar{B}_3 B_5) \\ &= B_1 B_2 (B_3 + B_4 + B_5) = \bar{D}_{10} \end{aligned} \quad (2.2)$$

2. D_2 , the "tens" digit.

$$\begin{aligned} D_{20} &= \bar{B}_1 \bar{B}_2 \bar{B}_3 (\bar{B}_4 + \bar{B}_5 \bar{B}_6) + B_1 B_2 \bar{B}_3 (\bar{B}_4 B_5 + B_4 \bar{B}_5 + B_4 B_5 \bar{B}_6) \\ &= \bar{B}_1 \bar{B}_2 \bar{B}_3 (\bar{B}_4 + \bar{B}_5 \bar{B}_6) + B_1 B_2 \bar{B}_3 (\bar{B}_4 B_5 + B_4 \bar{B}_5 + B_4 \bar{B}_6) \end{aligned} \quad (2.3)$$

$$\begin{aligned} D_{21} &= \bar{B}_1 \bar{B}_2 (\bar{B}_3 B_4 B_5 + \bar{B}_3 B_4 B_6 + B_3 \bar{B}_4 \bar{B}_5) + B_1 B_2 (\bar{B}_3 B_4 B_5 B_6 + B_3 \bar{B}_4) \\ &= \bar{B}_1 \bar{B}_2 [\bar{B}_3 B_4 (B_5 + B_6) + B_3 \bar{B}_4 \bar{B}_5] + B_1 B_2 (\bar{B}_3 B_4 B_5 B_6 + B_3 \bar{B}_4) \end{aligned} \quad (2.4)$$

$$\begin{aligned} D_{22} &= \bar{B}_1 \bar{B}_2 B_3 \bar{B}_4 B_5 + B_1 B_2 (\bar{B}_5 + B_5 \bar{B}_6) + B_1 B_2 B_3 B_4 \\ &= \bar{B}_1 \bar{B}_2 B_3 (\bar{B}_4 B_5 + B_4 \bar{B}_5 + B_4 \bar{B}_6) + B_1 B_2 B_3 B_4 \end{aligned} \quad (2.5)$$

$$D_{23} = \bar{B}_1 (\bar{B}_2 B_3 B_4 B_5 B_6 + B_2 \bar{B}_3 \bar{B}_4) \quad (2.6)$$

$$D_{24} = \bar{B}_1 B_2 (\bar{B}_3 B_4 + B_3 \bar{B}_4 \bar{B}_5 \bar{B}_6) \quad (2.7)$$

$$\begin{aligned} D_{25} &= \bar{B}_1 B_2 B_3 \bar{B}_4 (\bar{B}_5 B_6 + B_5) + B_4 \bar{B}_5 \\ &= \bar{B}_1 B_2 B_3 [\bar{B}_4 (B_5 + B_6) + B_4 \bar{B}_5] \end{aligned} \quad (2.8)$$

$$\begin{aligned} D_{26} &= \bar{B}_1 B_2 B_3 B_4 B_5 + B_1 \bar{B}_2 \bar{B}_3 \bar{B}_4 (\bar{B}_5 + B_5 \bar{B}_6) \\ &= \bar{B}_1 B_2 B_3 B_4 B_5 + B_1 \bar{B}_2 \bar{B}_3 \bar{B}_4 (\bar{B}_5 + \bar{B}_6) \end{aligned} \quad (2.9)$$

$$D_{27} = B_1 \bar{B}_2 \bar{B}_3 (B_4 + B_5 B_6) \quad (2.10)$$

$$D_{28} = B_1 \bar{B}_2 B_3 (\bar{B}_4 + \bar{B}_5 \bar{B}_6) \quad (2.11)$$

$$\begin{aligned}
 D_{29} &= B_1 [\bar{B}_2 B_3 B_4 (\bar{B}_5 B_6 + B_5) + B_2 \bar{B}_3 \bar{B}_4 \bar{B}_5] \\
 &= B_1 [\bar{B}_2 B_3 B_4 (B_5 + B_6) + B_2 \bar{B}_3 \bar{B}_4 \bar{B}_5]
 \end{aligned}
 \tag{2.12}$$

Before writing the D_3 equations, it should be noted here that so far the conversion is not too cumbersome, since the twelve equations above can be mechanized with about 141 diodes and 7 triodes. The situation for D_3 is different.

3. D_3 , the "units" digit.

$$\begin{aligned}
 D_{30} &= \bar{B}_7 [\bar{B}_1 \bar{B}_2 \bar{B}_3 \bar{B}_4 \bar{B}_5 \bar{B}_6 + \bar{B}_1 \bar{B}_2 \bar{B}_3 B_4 \bar{B}_5 \bar{B}_6 + \bar{B}_1 \bar{B}_2 B_3 \bar{B}_4 \bar{B}_5 \bar{B}_6 \\
 &\quad + \bar{B}_1 \bar{B}_2 B_3 B_4 B_5 \bar{B}_6 + \bar{B}_1 B_2 \bar{B}_3 \bar{B}_4 \bar{B}_5 \bar{B}_6 + \bar{B}_1 B_2 B_3 \bar{B}_4 \bar{B}_5 \bar{B}_6 \\
 &\quad + \bar{B}_1 B_2 B_3 B_4 B_5 \bar{B}_6 + B_1 \bar{B}_2 \bar{B}_3 \bar{B}_4 B_5 \bar{B}_6 + B_1 \bar{B}_2 \bar{B}_3 B_4 \bar{B}_5 \bar{B}_6 \\
 &\quad + B_1 \bar{B}_2 \bar{B}_3 B_4 B_5 \bar{B}_6 + B_1 B_2 \bar{B}_3 \bar{B}_4 \bar{B}_5 \bar{B}_6 + B_1 B_2 \bar{B}_3 B_4 B_5 \bar{B}_6 \\
 &\quad + B_1 B_2 B_3 \bar{B}_4 \bar{B}_5 \bar{B}_6]
 \end{aligned}
 \tag{2.13}$$

$$D_{31} = B_7 [\text{Same as inside brackets above}]
 \tag{2.14}$$

$$\begin{aligned}
 D_{32} &= \bar{B}_7 [\bar{B}_1 \bar{B}_2 \bar{B}_3 \bar{B}_4 \bar{B}_5 \bar{B}_6 + \bar{B}_1 \bar{B}_2 \bar{B}_3 B_4 B_5 \bar{B}_6 + \bar{B}_1 \bar{B}_2 B_3 \bar{B}_4 B_5 \bar{B}_6 \\
 &\quad + \bar{B}_1 \bar{B}_2 B_3 B_4 B_5 \bar{B}_6 + \bar{B}_1 B_2 \bar{B}_3 \bar{B}_4 \bar{B}_5 \bar{B}_6 + \bar{B}_1 B_2 B_3 \bar{B}_4 B_5 \bar{B}_6 \\
 &\quad + \bar{B}_1 B_2 B_3 B_4 B_5 \bar{B}_6 + B_1 \bar{B}_2 \bar{B}_3 \bar{B}_4 B_5 \bar{B}_6 + B_1 \bar{B}_2 \bar{B}_3 B_4 \bar{B}_5 \bar{B}_6 \\
 &\quad + B_1 \bar{B}_2 \bar{B}_3 B_4 B_5 \bar{B}_6 + B_1 B_2 \bar{B}_3 \bar{B}_4 \bar{B}_5 \bar{B}_6 + B_1 B_2 \bar{B}_3 B_4 B_5 \bar{B}_6 \\
 &\quad + B_1 B_2 B_3 \bar{B}_4 \bar{B}_5 \bar{B}_6]
 \end{aligned}
 \tag{2.15}$$

$$D_{33} = B_7 [\text{Same as inside brackets above}]
 \tag{2.16}$$

- - - - -

Without writing the rest of the D_3 equations, the results can be evaluated. If all of the D_3 equations are written, there will be a total of 128 terms in all 10 equations (13 terms in each of the equations for $D_{30} - D_{37}$ and 12 in the equations for D_{38} and D_{39}). None of the equations can be reduced, as may be suspected by observing the first four. Therefore, to mechanize the D_3 equations, all 128 terms could be generated in one of the standard "and-tree" matrices, such as the one shown in Fig. 2.1.

Fig. 2.1 — Tree Matrix Which Will Generate the 128 Terms for the D_3 Equations

A matrix such as the one in Fig. 2.1 would take about 328 diodes, plus the 7 triodes necessary to give the inverted inputs. Since the outputs of this matrix must be combined further, the matrix is denoted as follows:

The outputs of M_1 can now be combined in "or" circuits to form the ten D_3 outputs. Also, since all of the 128 elemental forms have been generated in M_1 , the ten D_2 outputs could be generated using the outputs of M_1 . To generate the D_2 outputs would take 128 additional diodes, compared with about 141 diodes to generate separately the D_2 outputs (see Eqs 2.3 through 2.12). It is evidently better to use the M_1 outputs to generate both the D_3 and the D_2 outputs.

The D_1 outputs could of course also be formed using the outputs of M_1 , but obviously Eqs 2.1 and 2.2 are much easier to mechanize.

The complete form of this type of binary-decimal converter is now shown in Fig. 2.2. The ten D_2 and the ten D_3 outputs are generated using the M_1 outputs, and D_1 is generated separately.

Altogether, the converter shown in Fig. 2.2 would take 590 diodes and 8 triodes, not counting extra devices needed for clamping, amplification, etc. Although expensive and complex, it could operate rapidly and all 22 decimal outputs would be completely isolated.

 

Fig. 2.2 — One Type of Binary-to-Decimal Converter

Fig. 2. Schematic diagram of the 128-bit shift register.

Method 2

Two special criteria for the binary-decimal converter needed by Sandia Corporation suggest other approaches to the problem. First, the converter will be used as an indicating device with the output displayed on lights. Secondly, the necessary conversion rate here is quite low, being 25 conversions/sec. The first criterion suggests that the output of the converter might be in some decimal code, rather than on 22 separate lines. This is essentially the difference between Method 2 and Method 1. The second criterion will be disregarded for the time being.

A large number of decimal codes is available.² All of the simplest codes use four binary bits to represent a single decimal digit, four bits being the minimum number for representing a digit having ten possible values. In different codes, each of the four bits has a different weight assigned to it, or no weight at all. Examples of some different four-bit codes are given in Table 2.2. The 8421 code is a straight binary representation of the decimal digit. All other four-bit codes simply use ten unique combinations of ones and zeros to represent the ten decimal digits.

Table 2.2 — FOUR-BIT DECIMAL CODES

<u>Decimal Number</u>	8421 Code	6311 Code	Nonweighted (Excess-3) Code
	$\begin{smallmatrix} b_1 & b_2 & b_3 & b_4 \\ \hline 1 & 2 & 3 & 4 \end{smallmatrix}$	$\begin{smallmatrix} b_1 & b_2 & b_3 & b_4 \\ \hline 1 & 2 & 3 & 4 \end{smallmatrix}$	$\begin{smallmatrix} b_1 & b_2 & b_3 & b_4 \\ \hline 1 & 2 & 3 & 4 \end{smallmatrix}$
0	0 0 0 0	0 0 0 0	0 0 1 1
1	0 0 0 1	0 0 0 1	0 1 0 0
2	0 0 1 0	0 0 1 1	0 1 0 1
3	0 0 1 1	0 1 0 0	0 1 1 0
4	0 1 0 0	0 1 0 1	0 1 1 1
5	0 1 0 1	0 1 1 1	1 0 0 0
6	0 1 1 0	1 0 0 0	1 0 0 1
7	0 1 1 1	1 0 0 1	1 0 1 0
8	1 0 0 0	1 0 1 1	1 0 1 1
9	1 0 0 1	1 1 0 0	1 1 0 0

2. Ibid.

If the converter output consisted of decimal digits in some four-bit code, straight decimal indication could be achieved with the use of neon lights and resistors in a permutating network. A permutating network for the 8421 code is shown in Fig. 2.3. In this example, the numbered neon lights in the center will fire at 70 volts, and any "b" input is either 60 or 140 volts depending on whether it is 0 or 1. The inverse bits, or " $\bar{b}$ "'s, are available here also, since each bit is assumed to be stored in a flip-flop stage, where either plate voltage may be used. Note that a given lamp will not light unless the proper b_4 bus is at +140 volts and all inputs to the other side of the lamp are at 60 volts. Referring to Table 2.2, it can be seen how the decimal indication of the 8421 code is achieved in Fig. 2.3. The permutation of any other decimal code is just as simple and would require about the same number of components.

Fig. 2.3 — Permutating Network for 8421 Code

Thus, if it were easier to convert from binary to some decimal code than to straight decimal as in Method 1, a saving in components could probably be achieved, since the permutating network is quite simple.

Of the many four-bit codes, the excess-3 code was chosen for use as an example here, not because it has any unique properties, but because a binary-to-excess-3 converter has already

been built with relays.³ In looking at other four-bit codes, it appears that conversion from binary to other codes is no simpler than conversion to excess-3. However, no proof of this fact is known to the author, and the existence of an easier-to-convert-to code is possible.

The excess-3 code is shown in Table 2.2. Since three decimal digits must be represented by this code at the converter output, nine bits must be generated. The output will be of the form

$$e_1 \quad e_2 e_3 e_4 e_5 \quad e_6 e_7 e_8 e_9 \quad ,$$

where e_1 represents the hundreds digit (can only be 0 or 1), $e_2 e_3 e_4 e_5$ represents the tens digit, and $e_6 e_7 e_8 e_9$ represents the units digit. A permutating network for the tens digit is shown in Fig. 2.4. Operation is similar to the 8421 code permutating network already described.

Fig. 2.4 — Permutating Network for Excess-3 Code (Tens Digit)

For conversion from binary to excess-3, the Boolean equations may be examined for possible means of mechanization. This has been done, and it has been found⁴ that the simplest way to convert is to generate all 12 decades on separate lines, and then generate most of the e 's

3. Robnett, A. V. and Vulgan, E. J., Small-Scale Automatic Field-Data Reduction System, Sandia Corporation TM-236-55-51, October 3, 1955.

4. Ibid.

and with a view to the fact that the system is not a simple one, the following is a brief description of the system. The system is a simple one, and the following is a brief description of the system. The system is a simple one, and the following is a brief description of the system.

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The system is a simple one, and the following is a brief description of the system. The system is a simple one, and the following is a brief description of the system. The system is a simple one, and the following is a brief description of the system.

using these decade lines. Letting $\Delta_1, \Delta_2, \dots, \Delta_{12}$ be the twelve decades, and letting $B_1 B_2 B_3 B_4 B_5 B_6 B_7$ be the seven-bit binary input, the Boolean expressions for the e's are as follows:

$$e_1 = B_1 B_2 (B_3 + B_4 + B_5) \quad (2.17)$$

$$e_2 = \Delta_5 + \Delta_6 + \Delta_7 + \Delta_8 + \Delta_9 \quad (2.18)$$

$$e_3 = \Delta_1 + \Delta_2 + \Delta_3 + \Delta_4 + \Delta_9 + \Delta_{11} + \Delta_{12} \quad (2.19)$$

$$e_4 = \Delta_0 + \Delta_3 + \Delta_4 + \Delta_7 + \Delta_8 + \Delta_{10} \quad (2.20)$$

$$e_5 = \Delta_0 + \Delta_2 + \Delta_4 + \Delta_6 + \Delta_8 + \Delta_{10} + \Delta_{12} \quad (2.21)$$

$$e_6 = e_7 \bar{e}_8 \bar{e}_9 \left[B_4 (\Delta_0 + \Delta_2 + \Delta_5 + \Delta_7 + \Delta_8 + \Delta_{10}) + \bar{B}_4 (\Delta_1 + \Delta_3 + \Delta_4 + \Delta_6 + \Delta_9 + \Delta_{11} + \Delta_{12}) \right] + \bar{e}_7 \left[\bar{e}_8 + \bar{e}_9 + B_4 (\Delta_0 + \Delta_2 + \Delta_5 + \Delta_7 + \Delta_8 + \Delta_{10}) + \bar{B}_4 (\Delta_1 + \Delta_3 + \Delta_4 + \Delta_6 + \Delta_9 + \Delta_{11} + \Delta_{12}) \right] \quad (2.22)$$

$$e_7 = (\Delta_0 + \Delta_4 + \Delta_8 + \Delta_{12}) \left[B_5 \bar{B}_6 \bar{B}_7 + \bar{B}_5 (B_6 + B_7) \right] + (\Delta_2 + \Delta_6 + \Delta_{10}) \left[\bar{B}_5 \bar{B}_6 \bar{B}_7 + B_5 (B_6 + B_7) \right] + (\Delta_1 + \Delta_5 + \Delta_9) \left[B_5 (\bar{B}_6 + \bar{B}_7) + \bar{B}_5 B_6 B_7 \right] + (\Delta_3 + \Delta_7 + \Delta_{11}) \left[\bar{B}_5 (\bar{B}_6 + \bar{B}_7) + B_5 B_6 B_7 \right] \quad (2.23)$$

$$e_8 = (\Delta_1 + \Delta_3 + \Delta_5 + \Delta_7 + \Delta_9 + \Delta_{11}) (B_6 \bar{B}_7 + \bar{B}_6 B_7) + (\Delta_0 + \Delta_2 + \Delta_4 + \Delta_6 + \Delta_8 + \Delta_{10} + \Delta_{12}) (B_6 B_7 + \bar{B}_6 \bar{B}_7) \quad (2.24)$$

$$e_9 = \bar{B}_7 \quad (2.25)$$

The separate generation of Δ_1 through Δ_{12} is of course also necessary, and so the following equations must also be mechanized:

$$\Delta_0 = \bar{B}_1 \bar{B}_2 \bar{B}_3 (\bar{B}_4 + \bar{B}_5 \bar{B}_6) \quad (2.26)$$

using these same lines. Let $\alpha = \frac{1}{2} \pi$ be the angle between the lines

and $\beta = \frac{1}{2} \pi$ be the angle between the lines and the line

then

$$(2.10) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.11) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.12) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.13) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.14) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$\alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$\alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$\alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.15) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$\alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$\alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$\alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.16) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$\alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$\alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.17) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.18) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.19) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

The separate connection of α through β is of course also necessary, and so the

following equation must also be considered:

$$\alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$(2.20) \quad \alpha = \frac{1}{2} \pi, \quad \beta = \frac{1}{2} \pi$$

$$\Delta_1 = \bar{B}_1 \bar{B}_2 [\bar{B}_3 B_4 (B_5 + B_6) + B_3 \bar{B}_4 \bar{B}_5] \quad (2.27)$$

$$\Delta_2 = \bar{B}_1 \bar{B}_2 B_3 [\bar{B}_4 B_5 + B_4 (\bar{B}_5 + \bar{B}_6)] \quad (2.28)$$

$$\Delta_3 = \bar{B}_1 (\bar{B}_2 B_3 B_4 B_5 B_6 + B_2 \bar{B}_3 \bar{B}_4) \quad (2.29)$$

$$\Delta_4 = \bar{B}_1 B_2 (\bar{B}_3 B_4 + B_3 \bar{B}_4 \bar{B}_5 \bar{B}_6) \quad (2.30)$$

$$\Delta_5 = \bar{B}_1 B_2 B_3 [\bar{B}_4 (B_5 + B_6) + B_4 \bar{B}_5] \quad (2.31)$$

$$\Delta_6 = \bar{B}_1 B_2 B_3 B_4 B_5 + B_1 \bar{B}_2 \bar{B}_3 \bar{B}_4 (\bar{B}_5 + \bar{B}_6) \quad (2.32)$$

$$\Delta_7 = B_1 \bar{B}_2 \bar{B}_3 (B_5 B_6 + B_4) \quad (2.33)$$

$$\Delta_8 = B_1 \bar{B}_2 B_3 (\bar{B}_4 + \bar{B}_5 \bar{B}_6) \quad (2.34)$$

$$\Delta_9 = B_1 [\bar{B}_2 B_3 B_4 (B_5 + B_6) + B_2 \bar{B}_3 \bar{B}_4 \bar{B}_5] \quad (2.35)$$

$$\Delta_{10} = B_1 B_2 \bar{B}_3 [\bar{B}_4 B_5 + B_4 (\bar{B}_5 + \bar{B}_6)] \quad (2.36)$$

$$\Delta_{11} = B_1 B_2 (\bar{B}_3 B_4 B_5 B_6 + B_3 \bar{B}_4) \quad (2.37)$$

$$\Delta_{12} = B_1 B_2 B_3 B_4 \quad (2.38)$$

A converter using the mechanization of these e - and Δ - equations has been built⁵ with relays and diodes, and it uses 15 multicontact relays and 36 diodes. Because of the relays, its maximum conversion rate is 25 conversions/sec. Using only diodes, the same converter would require about 250 diodes, plus 7 triodes for inverting the input; again not counting extra devices for clamping, amplification, etc.

Method 2, then, although still requiring a large number of components, is simpler than Method 1 and would operate as rapidly as desired.

5. Ibid.

(2.30)
(2.29)
(2.28)
(2.27)
(2.26)
(2.25)
(2.24)
(2.23)
(2.22)
(2.21)
(2.20)
(2.19)
(2.18)
(2.17)

$$\begin{aligned}
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots \\
 & \dots
 \end{aligned}$$

A computer using the mechanism of these a and b operations has been built with relays and diodes, and it does its minimum relay and is fitted. Because of the relay, the relay computer is a 20 computer, being only diodes, the same answer would require about the diodes, plus 7 relays for testing the relay, again not counting extra devices for clearing, registering, etc.

Method 2. This, although still requiring a large number of components, is faster than Method 1 and would give an output as desired.

Method 3

The third and final method for mechanizing the binary-decimal converter is suggested by the second special criterion mentioned at the beginning of the discussion of Method 2; that is, that the necessary conversion rate of this particular converter is quite slow, being only 25 or more conversions/sec. This slow conversion rate suggests that the binary input might actually be counted by some scaling device after it enters the converter.

Using a scale-of-128 binary scaler with 7 scaling stages, each of the 7 binary input bits could alter each of the scaling stages in some prescribed manner from some known reset condition. Then the scaler could be triggered by an external device and set to some known stable condition. The number of trigger pulses required to set the scaler to this known condition would depend upon the manner in which the scaler had been altered from its reset condition; i.e., the number of trigger pulses would be a function of the seven-bit binary input. If the number of trigger pulses were counted, a decimal indication of the input could be obtained.

A block diagram of this idea is shown in Fig. 2.5. The binary scaler, consisting of the 7 coupled binary stages at the top of Fig. 2.5, is reset to 1111111. Then the binary input ($B_1B_2B_3B_4B_5B_6B_7$) is allowed to enter the scaling stages. If a particular B input is 1, it will change its corresponding scaler stage to the zero condition; otherwise the stage will remain set at 1. Thus each of the B's is effectively inverted when it is stored. Inverting all of the bits of a binary number in this manner is the same as creating its one's complement, which is

$$2^n - N - 1 \quad ,$$

where N is the binary number and n is the number of bits in N, or 7 in this case. The number

$$127 - N \quad ,$$

then, is stored in the binary scaler.

When the binary scaler was reset to 1111111, the decade scaler at the bottom of Fig. 2.5 was reset to 199. The decade scaler altogether is a scale-of-200 scaler, so that one pulse from the oscillator will make it read 000.

The first and most important consideration in the design of the system is the selection of the material of construction. It is essential that the material be capable of withstanding the stresses and strains to which it will be subjected. The material should also be resistant to corrosion and have a long service life.

The second consideration is the selection of the type of joint to be used. The joint should be capable of transmitting the full load without any loss of strength. It should also be easy to install and maintain. The type of joint selected will depend on the nature of the service to which the system is to be put.

The third consideration is the selection of the type of support to be used. The support should be capable of supporting the full load without any deflection. It should also be easy to install and maintain. The type of support selected will depend on the nature of the service to which the system is to be put.

The fourth consideration is the selection of the type of fastener to be used. The fastener should be capable of withstanding the full load without any failure. It should also be easy to install and maintain. The type of fastener selected will depend on the nature of the service to which the system is to be put.

The fifth consideration is the selection of the type of paint to be used. The paint should be capable of protecting the system from corrosion. It should also be easy to apply and maintain. The type of paint selected will depend on the nature of the service to which the system is to be put.

Fig. 2.5 — A Binary-to-Decimal Converter Using Method 3

After the above-mentioned reset and storage operations have taken place, a clock pulse starts the oscillator running. The pulses out of the oscillator enter both scalers. The first pulse from the oscillator increases the number stored in the binary scaler by one, and also changes the decade scaler from a reading of 199 to a reading of 000. Thus, at the instant that the decade scaler reads 000, the number in the binary scaler is:

$$\begin{aligned} & (127 - N) + 1 \\ & = 128 - N \end{aligned}$$

The oscillator continues to trigger both scalers until an output from the last binary stage shuts it off. At this point, the binary scaler is actually storing the number 128, since all of its stages are in the "0" condition. The decade scaler now reads the difference between 128 and $(128 - N)$, or N , and the binary-to-decimal conversion has been completed.

This relatively simple method of conversion seems to represent a considerable saving in components over Methods 1 and 2. For this reason, it was chosen as the best method for the mechanization of the converter.

Fig. 2.1. A 10-stage digital counter.

After the counter has been reset, a clock pulse is applied to the oscillator. The pulse out of the oscillator enters both counters. The first pulse from the oscillator increases the number stored in the binary counter by one, and the second pulse from the oscillator increases the number stored in the decimal counter by one. When the decimal counter changes the decade value from a reading of 9 to a reading of 0, the binary counter also changes the decade value from 9 to 0.

$$(10^N - 1) + 1$$

$$= 10^N - 1$$

The oscillator continues to deliver clock pulses until an output from the first binary stage shows it is 0. At this point, the binary counter is reset to 0, and the decimal counter is reset to 0. The counter now reads the difference between 10 and 0, which is 10. The counter is now reset to 0, and the binary counter is reset to 0.

This relatively simple method of generating a constant value is used in many digital systems. The value of the constant is determined by the number of stages in the counter. The value of the constant is also determined by the value of the reset input.

Although Method 3 seems to be somewhat unique, it is not presented as an absolute or "best" method of binary-decimal conversion. It is, however, the best method that could be found for this particular application. The next chapter describes in detail the circuitry and operation of a binary-decimal converter using Method 3.

CHAPTER 3. CIRCUITRY AND OPERATION OF THE BINARY-TO-DECIMAL CONVERTER

A basic block diagram of the converter was given in the third part of the preceding chapter, and the theory of operation was discussed. It was found that an oscillator could be made to put out a number of pulses equal to the input binary number plus one, and that these pulses could be counted by a decade scaler which had effectively been reset to minus one. The decade scaler would then give a decimal indication of the input.

A complete operational block diagram is shown in Fig. 3.1. The dotted lines around the individual blocks give reference to the figures that show the individual circuit schematics. In the scalers, where individual stages are identical, the circuit of only one stage will be shown. A complete schematic appears at the end of this chapter.

Referring to Fig. 3.1, the binary scaler consisting of seven binary blocks may be seen at the top of the figure, and the decade scaler at the bottom. Assuming that the binary scaler has been reset to lllllll and the decade scaler to 199, the sequence of operation goes as follows:

1. Binary number $B_1B_2B_3B_4B_5B_6B_7$ enters scaler stages. If any $B_i = 1$, then i^{th} stage is flipped to "0." "And Drive" is not on, so no interstage coupling is possible at this time.
2. With inverted binary bits now stored, clock pulse enters "Timing One-Shot."
3. Timing One-Shot immediately pulses "MV Switch," turning on "MV" (free-running multivibrator). And Drive is energized simultaneously, and interstage coupling in binary scaler is now possible.
4. MV free-runs and sends pulses to inputs of both scalers.
5. MV continues to run until binary scaler reaches 128, or 0000000, and gives an output pulse, causing MV Switch to turn MV off. "Decade Scaler" now reads decimal equivalent of input.

Fig. 3.1 -- Operational Block Diagram of the Binary-Decimal Converter

FIG. 3.1 - General Block Diagram of the Binary-Decimal Counter

6. Converter remains inoperative, with decade scaler reading correct output, until Timing One-Shot relaxes and returns to stable state.
7. When Timing One-Shot relaxes, "Reset Drive" is operated and scalars are reset. And Drive is simultaneously de-energized, cutting off interstage coupling.
8. Next binary number enters scaling stages, and cycle starts again.

Since the converter output is presented on the neon lights of the decade scaler, it is essential to have the scaler reading the correct output most of the time, in order that the observer may see the correct lights lit brightly. The decade scaler is either reset to 199, or it is being pulsed by the multivibrator, or it is reading the correct output. From this consideration, two things are essential for proper operation:

1. Reset must occur at the last possible moment before the binary number enters the converter.
2. The free-running multivibrator must run at a high enough frequency so that up to 128 pulses can be put out in a small fraction of the time between binary inputs.

If these two conditions are met, then the proper lights on the decade scaler will appear to burn brightly and continuously. They are easily met in this particular application, since the binary input frequency can be made to be as low as 25 numbers/sec. The multivibrator runs at 27.8 kc, and will put out 128 pulses in about 4.6 milliseconds. Thus, if the conversion rate is 25 conversions/sec, or one conversion every 40 milliseconds, multivibrator time is negligibly short. The time that the converter spends in the reset condition is determined somewhat by the shape of the binary input pulses, but it too is negligibly short. Due to the persistence of the eye, the proper neon lights appear to glow continuously.

The circuitry of each block in Fig. 3.1 is generally quite simple and straightforward. The binary scaler stages will be described first, and then the Timing One-Shot, the And Drive, the MV Switch, the MV, the Decade Scaler and the Reset Drive will be described in order.

 

Binary Scaler Stage with Coupling

The Binary Stage is shown in Fig. 3.2. It is almost exactly like a single Berkeley scaler stage,⁶ and is a typical example of the standard flip-flop circuit, or Eccles-Jordan circuit, with some modifications. Each of the seven stages is the same, except that the first stage does not have the IN48 diode or the input from And Drive.

Fig. 3.2 — Binary Scaler Stage (Except First Stage)

When a positive pulse arrives from Reset Drive, the left grid is driven positive and the left side conducts. A positive "Binary Bit" pulse on the right grid would cause the right side to conduct and the left side to cut off, or if there were no Binary Bit input, the left side would continue to conduct.

Both positive and negative pulses are coupled in from the previous stage; however, the circuit can be triggered only with negative pulses. The negative pulses will only trigger the

6. Berkeley Scientific Division of Beckman Instruments, Inc., "Instruction Manual - Berkeley Decimal Counting Units - Models 700A and 705A."

circuit if the And Drive input is less than 180 volts. If the And Drive input is more than 180 volts, the input pulse will see a lower impedance through the diode, and will be too small to trigger the stage.

The stage uses a 5963 twin-triode, which is specially designed for this type of on-off operation. It has a resolution time of about 10 microseconds, so that input frequencies up to about 100 kc may be used.

Matching the input binary lines to the 7 binary stages is important for proper operation of the converter. In the circuit used here, almost complete isolation of the scaler stage from any input source impedance is necessary. If some loading is anticipated at the binary bit inputs, component changes may be necessary in the binary stages in order to obtain stable operation and proper interstage triggering.

The Timing One-Shot

The Timing One-Shot, shown in Fig. 3.3, is a typical one-shot, or unistable multivibrator. The left side, with its grid tied to B+, is normally conducting. When a negative clock pulse enters, the left side cuts off and the right side conducts for a length of time determined primarily by the 1-meg resistor, the 0.03-mfd capacitor, and the setting of the 5-meg pot. The one-shot then returns to its stable condition.

Fig. 3.3 -- The Timing One-Shot

 

A clock pulse in causes the left plate to rise from 30 volts to 300 volts, and this positive-going voltage is coupled out to the And Drive circuit. At the same time, a negative pulse is coupled from the right plate to turn on the MV Switch. Later, when the one-shot returns to its stable state, the negative-going left plate turns off the And Drive, and simultaneously sends a negative pulse out to the Reset Drive. It is obvious that the clock pulse must be a negative pulse which arrives just after the binary inputs (see description of Fig. 3.1).

The length of time between the clock pulse and the negative pulse out to Reset Drive is determined by the setting of the 5-meg pot. The 5-meg pot, then, may be used to adjust the timing of reset, so that it occurs just before the binary input pulses arrive at the scaler stages. The duration between clock pulse and reset is variable from 8 ms to 53 ms. The 1-meg resistor is added in series with the 5-meg pot to insure a minimum duration, long enough for the MV to put out 128 pulses. The input capacitor, C, has a value which depends on the size and shape of the clock pulse.

A typical waveform appearing at the left plate is shown below.

And Drive

The And Drive circuit is simply a triode amplifier, inverter and impedance matcher which is connected to the six interstage binary coupling lines through six diodes. With no signal in on the grid, the triode is held cut off by the cathode biasing arrangement shown in Fig. 3.4.

After the storage operation has taken place in the binary stages, the positive-going plate of the Timing One-Shot is coupled to the grid of And Drive through the 0.05-mfd capacitor. The plate of And Drive then goes negative, and binary interstage coupling is then possible. The long-time constant in the And Drive grid circuit causes the plate to remain low until a negative voltage is coupled in from the Timing One-Shot, cutting off the And Drive tube and thus again making binary interstage coupling impossible.

A series of experiments were conducted to determine the effect of the concentration of the solution on the rate of reaction.

The results of the experiments are shown in the following table:

TABLE I

Rate of reaction as a function of the concentration of the solution

The rate of reaction was measured by the volume of gas evolved per unit time.

The results of the experiments are shown in the following table:

TABLE II

Rate of reaction as a function of the concentration of the solution

The rate of reaction was measured by the volume of gas evolved per unit time.

The results of the experiments are shown in the following table:

TABLE III

Rate of reaction as a function of the concentration of the solution

The rate of reaction was measured by the volume of gas evolved per unit time.

The results of the experiments are shown in the following table:

TABLE IV

Rate of reaction as a function of the concentration of the solution

The rate of reaction was measured by the volume of gas evolved per unit time.

The results of the experiments are shown in the following table:

TABLE V

Rate of reaction as a function of the concentration of the solution

The rate of reaction was measured by the volume of gas evolved per unit time.

The results of the experiments are shown in the following table:

TABLE VI

Rate of reaction as a function of the concentration of the solution

The rate of reaction was measured by the volume of gas evolved per unit time.

The results of the experiments are shown in the following table:

TABLE VII

Rate of reaction as a function of the concentration of the solution

The rate of reaction was measured by the volume of gas evolved per unit time.

The results of the experiments are shown in the following table:

TABLE VIII

Rate of reaction as a function of the concentration of the solution

The rate of reaction was measured by the volume of gas evolved per unit time.

The results of the experiments are shown in the following table:

TABLE IX

Rate of reaction as a function of the concentration of the solution

The rate of reaction was measured by the volume of gas evolved per unit time.

Fig. 3.4 — And Drive Circuit

The And Drive 50-k plate resistance is low enough so that a low shunting impedance is seen by the binary outputs whenever the And Drive tube is not conducting.

MV Switch

The MV Switch is a single flip-flop stage which acts as an on-off switch for the MV (Fig. 3.5). When a negative pulse is coupled in from the Timing One-Shot the right side cuts off, the right plate goes positive, and the MV is turned on. When a negative pulse is coupled in from the last Binary Stage, the circuit is flipped back and the MV is turned off. The manner in which the MV is switched on and off is described in the next section.

The MV

The MV stage is a standard plate-coupled free-running multivibrator circuit, designed to run at about 27.8 kc (Fig. 3.6). The circuit is symmetric and free-running only if the right side of the MV Switch circuit is cut off. If the right side of the MV Switch is conducting, then the left side of the MV is driven into cutoff by virtue of the direct coupling between the stages. Fast and positive switching of the MV is accomplished with this arrangement.

Fig. 1.4 - 555 timer circuit

The 555 timer is a monostable multivibrator. It is used to generate a single pulse of a specific width and amplitude.

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Fig. 1.4

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Fig. 3.5 — MV Switch Circuit

Fig. 3.6 — MV Circuit

One point is important in the operation of the MV: when it is switched on, the left side conducts first, and so a positive pulse is first coupled out to the scalars, and then a negative pulse, a positive pulse, a negative pulse, and so on. Since only negative pulses will trigger the scalars, a delay of

$$\frac{1}{2} \left(\frac{1}{f} \right) = \frac{1}{2} \left(\frac{1}{27.8 \times 10^3} \right) = 18.0 \mu\text{sec}$$

is created between the time that the MV Switch operates and the time that the first trigger pulse goes to the scalars. This delay allows the And Drive circuit time to completely turn on interstage coupling in the binary scaler. The free-running MV waveform is shown below.

The Decade Scaler

The units and tens decades are alike, and Fig. 3.7 shows the circuit of either decade. The hundreds decade is shown in Fig. 3.8. When the three decades are cascaded, a scale-of-200 decade scaler is the result. Since the maximum number of input pulses to the scaler is 128, the scale of 200 is adequate.

The units and tens decades are almost exact copies of the Berkeley decade unit,⁷ except for the reset connections, the capacitors in the permutating networks, and other minor changes. The Berkeley unit is designed for mechanical reset, while electronic reset was necessary here. Also, the Berkeley units are reset to zero, while the units and tens decades here are each reset to nine. These decades are standard split-feedback scale-of-ten circuits, with capacitive coupling and 4221 code permutating networks.⁸ The 0.25-mfd capacitors in Figs. 3.7 and 3.8 hold the neon lights off during reset, so that they will not flicker while the converter is running.

The Hundreds circuit, shown in Fig. 3.8, is a single binary stage. It is exactly like binary stages 2, 3 or 4 in either the units or the tens circuit. The Ne-51 neon lamp will light when the stage remains in the "one" state, with the right side conducting. This stage is reset to one.

7. Ibid.

8. For description of operation, see Ibid.

is shown in the figure. The figure shows the results of the experiment.

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Fig. 3.7 — Units and Tens Decades

Fig. 3.8 — Hundreds Decade

Reset Drive

The Reset Drive circuit, which sends a positive pulse to the proper grids of all scaler stages, is shown in Fig. 3.9. Due to the short time constant in the input grid circuit, the pulse from the left plate of the Timing One-Shot appears at the input grid in differentiated form, which is a positive pulse followed by a negative pulse. Since the input triode is normally conducting, only the negative input pulse has an appreciable effect on the plate voltage.

Fig. 3.9 — Reset Drive Circuit

Fig. 1-1 - Vacuum Tube

Notes

The first stage, which is a pentode, is the first of all stages. It is shown in Fig. 1-1. The second stage is a triode, which is shown in Fig. 1-2. The third stage is a pentode, which is shown in Fig. 1-3. The fourth stage is a triode, which is shown in Fig. 1-4. The fifth stage is a pentode, which is shown in Fig. 1-5. The sixth stage is a triode, which is shown in Fig. 1-6. The seventh stage is a pentode, which is shown in Fig. 1-7. The eighth stage is a triode, which is shown in Fig. 1-8. The ninth stage is a pentode, which is shown in Fig. 1-9. The tenth stage is a triode, which is shown in Fig. 1-10. The eleventh stage is a pentode, which is shown in Fig. 1-11. The twelfth stage is a triode, which is shown in Fig. 1-12. The thirteenth stage is a pentode, which is shown in Fig. 1-13. The fourteenth stage is a triode, which is shown in Fig. 1-14. The fifteenth stage is a pentode, which is shown in Fig. 1-15. The sixteenth stage is a triode, which is shown in Fig. 1-16. The seventeenth stage is a pentode, which is shown in Fig. 1-17. The eighteenth stage is a triode, which is shown in Fig. 1-18. The nineteenth stage is a pentode, which is shown in Fig. 1-19. The twentieth stage is a triode, which is shown in Fig. 1-20. The twenty-first stage is a pentode, which is shown in Fig. 1-21. The twenty-second stage is a triode, which is shown in Fig. 1-22. The twenty-third stage is a pentode, which is shown in Fig. 1-23. The twenty-fourth stage is a triode, which is shown in Fig. 1-24. The twenty-fifth stage is a pentode, which is shown in Fig. 1-25. The twenty-sixth stage is a triode, which is shown in Fig. 1-26. The twenty-seventh stage is a pentode, which is shown in Fig. 1-27. The twenty-eighth stage is a triode, which is shown in Fig. 1-28. The twenty-ninth stage is a pentode, which is shown in Fig. 1-29. The thirtieth stage is a triode, which is shown in Fig. 1-30. The thirty-first stage is a pentode, which is shown in Fig. 1-31. The thirty-second stage is a triode, which is shown in Fig. 1-32. The thirty-third stage is a pentode, which is shown in Fig. 1-33. The thirty-fourth stage is a triode, which is shown in Fig. 1-34. The thirty-fifth stage is a pentode, which is shown in Fig. 1-35. The thirty-sixth stage is a triode, which is shown in Fig. 1-36. The thirty-seventh stage is a pentode, which is shown in Fig. 1-37. The thirty-eighth stage is a triode, which is shown in Fig. 1-38. The thirty-ninth stage is a pentode, which is shown in Fig. 1-39. The fortieth stage is a triode, which is shown in Fig. 1-40. The forty-first stage is a pentode, which is shown in Fig. 1-41. The forty-second stage is a triode, which is shown in Fig. 1-42. The forty-third stage is a pentode, which is shown in Fig. 1-43. The forty-fourth stage is a triode, which is shown in Fig. 1-44. The forty-fifth stage is a pentode, which is shown in Fig. 1-45. The forty-sixth stage is a triode, which is shown in Fig. 1-46. The forty-seventh stage is a pentode, which is shown in Fig. 1-47. The forty-eighth stage is a triode, which is shown in Fig. 1-48. The forty-ninth stage is a pentode, which is shown in Fig. 1-49. The fiftieth stage is a triode, which is shown in Fig. 1-50. The fifty-first stage is a pentode, which is shown in Fig. 1-51. The fifty-second stage is a triode, which is shown in Fig. 1-52. The fifty-third stage is a pentode, which is shown in Fig. 1-53. The fifty-fourth stage is a triode, which is shown in Fig. 1-54. The fifty-fifth stage is a pentode, which is shown in Fig. 1-55. The fifty-sixth stage is a triode, which is shown in Fig. 1-56. The fifty-seventh stage is a pentode, which is shown in Fig. 1-57. The fifty-eighth stage is a triode, which is shown in Fig. 1-58. The fifty-ninth stage is a pentode, which is shown in Fig. 1-59. The sixtieth stage is a triode, which is shown in Fig. 1-60. The sixty-first stage is a pentode, which is shown in Fig. 1-61. The sixty-second stage is a triode, which is shown in Fig. 1-62. The sixty-third stage is a pentode, which is shown in Fig. 1-63. The sixty-fourth stage is a triode, which is shown in Fig. 1-64. The sixty-fifth stage is a pentode, which is shown in Fig. 1-65. The sixty-sixth stage is a triode, which is shown in Fig. 1-66. The sixty-seventh stage is a pentode, which is shown in Fig. 1-67. The sixty-eighth stage is a triode, which is shown in Fig. 1-68. The sixty-ninth stage is a pentode, which is shown in Fig. 1-69. The seventieth stage is a triode, which is shown in Fig. 1-70. The seventy-first stage is a pentode, which is shown in Fig. 1-71. The seventy-second stage is a triode, which is shown in Fig. 1-72. The seventy-third stage is a pentode, which is shown in Fig. 1-73. The seventy-fourth stage is a triode, which is shown in Fig. 1-74. The seventy-fifth stage is a pentode, which is shown in Fig. 1-75. The seventy-sixth stage is a triode, which is shown in Fig. 1-76. The seventy-seventh stage is a pentode, which is shown in Fig. 1-77. The seventy-eighth stage is a triode, which is shown in Fig. 1-78. The seventy-ninth stage is a pentode, which is shown in Fig. 1-79. The eightieth stage is a triode, which is shown in Fig. 1-80. The eighty-first stage is a pentode, which is shown in Fig. 1-81. The eighty-second stage is a triode, which is shown in Fig. 1-82. The eighty-third stage is a pentode, which is shown in Fig. 1-83. The eighty-fourth stage is a triode, which is shown in Fig. 1-84. The eighty-fifth stage is a pentode, which is shown in Fig. 1-85. The eighty-sixth stage is a triode, which is shown in Fig. 1-86. The eighty-seventh stage is a pentode, which is shown in Fig. 1-87. The eighty-eighth stage is a triode, which is shown in Fig. 1-88. The eighty-ninth stage is a pentode, which is shown in Fig. 1-89. The ninetieth stage is a triode, which is shown in Fig. 1-90. The ninety-first stage is a pentode, which is shown in Fig. 1-91. The ninety-second stage is a triode, which is shown in Fig. 1-92. The ninety-third stage is a pentode, which is shown in Fig. 1-93. The ninety-fourth stage is a triode, which is shown in Fig. 1-94. The ninety-fifth stage is a pentode, which is shown in Fig. 1-95. The ninety-sixth stage is a triode, which is shown in Fig. 1-96. The ninety-seventh stage is a pentode, which is shown in Fig. 1-97. The ninety-eighth stage is a triode, which is shown in Fig. 1-98. The ninety-ninth stage is a pentode, which is shown in Fig. 1-99. The one hundredth stage is a triode, which is shown in Fig. 1-100.

The negative input pulse causes the triode plate to rise momentarily, and this positive pulse is coupled to the control grid of the pentode, which is held close to cutoff with cathode biasing. The pentode acts as a cathode follower and sends a 110-volt positive pulse out through the 2-mfd capacitor to all scaler stages. This pulse is shown below.

This completes the discussion of the individual circuits in the converter. A complete schematic is given in Fig. 3.10. Power requirements for the converter are as follows:

Plate Supply: 300 v dc at 80 ma unregulated

Filaments: 6.3 v ac at 6.65 a.

The binary input pulses (positive pulse = 1, no pulse = 0) and the input clock pulse (negative pulse) are matched to the converter by varying the input coupling capacitors. In the case of the binary stages, it is essential that the inputs do not present too low an impedance as seen by the input grids; otherwise the binary scaler will not count properly. The clock pulse must arrive just after the binary input pulses.

Fig. 1-1 - Vacuum Tube

The first stage circuit, which serves as a pre-amplifier for the power stage of all series amplifiers, is shown in Fig. 1-1. The input signal is applied to the grid of the 6X4 tube through a 100K resistor. The grid is also connected to ground through a 0.001MFD capacitor. The plate of the 6X4 tube is connected to the B+ supply through a 50K resistor. The output of the first stage is taken from the plate through a 50K resistor and a 0.001MFD capacitor to ground. The cathode of the 6X4 tube is connected to ground through a 10K resistor and a 0.001MFD capacitor to ground.

CHAPTER 4. CONCLUSION

There are several different basic designs for a binary-to-decimal converter. The design used here seems to have the advantage of being a very simple design, but it cannot be proven to be the simplest possible.

The maximum conversion rate of this converter is limited because the converter actually "counts" the binary number. Other designs do not have this limitation.

The converter described here meets the requirements of the Sandia Corporation data handling system for which it was designed, and it should be useful in other data handling and computing systems as an indicating device.

APPENDIX A

THE GRAY CODE AND GRAY-TO-BINARY CONVERSION

The data-handling system that the binary-to-decimal converter has been designed for actually employs the inverted binary, or Gray code, and a Gray-to-decimal converter is what is actually required. The seven-bit Gray code for decimal numbers 1 through 127 is shown in Table A.1.

The Gray code is a nonweighted code. Inspection of this code indicates that Gray-to-decimal conversion would be more difficult than binary-to-decimal conversion. The Boolean equations for Gray-decimal are as complex or more complex than the binary-decimal equations. Furthermore, since the Gray code is nonweighted, no Gray-decimal converter employing Method 3 is possible.

Gray-to-binary conversion, however, is quite simple. Letting $G_1 G_2 G_3 \dots G_7$ be the Gray-coded number and $B_1 B_2 B_3 \dots B_7$ be the binary number, where B_1 and G_1 are the most significant bits, the Boolean relationships are

$$B_1 = G_1$$

and

$$B_n = B_{n-1} \overline{G_n} + \overline{B_{n-1}} G_n \quad \left| \quad n = 2, 3, 4, 5, 6, 7 \right.$$

These equations may be easily verified by inspecting Table A.1. They are comparatively easy to mechanize. A block diagram equivalent of the above equations is shown in Fig. A.1. In order to minimize the number of inverters (triodes), the B_n equations are manipulated as follows:

Table A.1 -- THE SEVEN-BIT GRAY CODE

Decimal	Gray	Decimal
	G 1 2 3 4 5 6 7	
0	0000000	0
1	0000001	1
2	0000011	2
3	0000010	3
4	0000110	4
5	0000111	5
6	0000101	6
7	0000100	7
8	0001100	8
9	0001101	9
10	0001111	10
11	0001110	11
12	0001010	12
13	0001011	13
14	0001001	14
15	0001000	15
16	0011000	16
17	0011001	17
18	0011011	18
19	0011010	19
20	0011110	20
21	0011111	21
22	0011101	22
23	0011100	23
24	0010100	24
25	0010101	25
26	0010111	26
27	0010110	27
28	0010010	28
29	0010011	29
30	0010001	30
31	0010000	31
32	0110000	32
33	0110001	33
34	0110011	34
35	0110010	35
36	0110110	36
37	0110111	37
38	0110101	38
39	0110100	39
40	0111100	40
41	0111101	41
42	0111111	42
43	0111110	43
44	0111010	44
45	0111011	45
46	0111001	46
47	0111000	47
48	0101000	48
49	0101001	49
50	0101011	50
51	0101010	51
52	0101110	52
53	0101111	53
54	0101101	54
55	0101100	55
56	0100100	56
57	0100101	57
58	0100111	58
59	0100110	59
60	0100010	60
61	0100011	61
62	0100001	62
63	0100000	63
64	1100000	64
65	1100001	65
66	1100011	66
67	1100010	67
68	1100110	68
69	1100111	69
70	1100101	70
71	1100100	71
72	1101100	72
73	1101101	73
74	1101111	74
75	1101110	75
76	1101010	76
77	1101011	77
78	1101001	78
79	1101000	79
80	1111000	80
81	1111001	81
82	1111011	82
83	1111010	83
84	1111110	84
85	1111111	85
86	1111101	86
87	1111100	87
88	1110100	88
89	1110101	89
90	1110111	90
91	1110110	91
92	1110010	92
93	1110011	93
94	1110001	94
95	1110000	95
96	1010000	96
97	1010001	97
98	1010011	98
99	1010010	99
100	1010110	100
101	1010111	101
102	1010101	102
103	1010100	103
104	1011100	104
105	1011101	105
106	1011111	106
107	1011110	107
108	1011010	108
109	1011011	109
110	1011001	110
111	1011000	111
112	1001000	112
113	1001001	113
114	1001011	114
115	1001010	115
116	1001110	116
117	1001111	117
118	1001101	118
119	1001100	119
120	1000100	120
121	1000101	121
122	1000111	122
123	1000110	123
124	1000010	124
125	1000011	125
126	1000001	126
127	1000000	127

$$\begin{aligned}
 B_n &= B_{n-1} \overline{G_n} + \overline{B_{n-1}} G_n \\
 &= \overline{B_{n-1} G_n + \overline{B_{n-1}} \overline{G_n}} \\
 &= \overline{(B_{n-1} G_n) (\overline{B_{n-1}} \overline{G_n})} \\
 &= \overline{B_{n-1} G_n} (B_{n-1} + G_n)
 \end{aligned}$$

The final expression above is mechanized in Fig. A.1 below.

Fig. A.1 -- Gray-to-Binary Converter

Diagram illustrating the logic circuit for the function $f(A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z)$.

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