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Andrew Hollowell

COPPER ELECTRODEPOSITION IN FULL WAFER THICKNESS THROUGH-SILICON VIAS

BY

REBECCA PAULINE SCHMITT

B.S., Natural Sciences, Colorado State University, 2014
B.S., Chemistry, University of New Mexico, 2018

THESIS

Submitted in Partial Fulfillment of the
Requirements for the Degree of

Master of Science
Chemical Engineering

The University of New Mexico
Albuquerque, New Mexico

December 2020

DEDICATION

This work is dedicated to my husband, Jason, and to my family. Jason, I am grateful for your unwavering support and encouragement as I complete my master's program. Stella and Tux, thanks for the endless fun, love, hugs, and stress relief after every long day at school and work. Thank you to my parents, Joe and Peggy, for showing me the value of hard work and supporting my academic pursuits throughout my life. To my brother, Matt, I am continually grateful for your friendship through each stage of life and thank you for always offering a listening ear and being a caring friend. To my Grandma Rose, thank you for your constant love, for taking pride in our family, and for supporting me in all that I do.

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ABSTRACT

Through-silicon vias (TSVs) are a key interconnect technology for advanced packaging of microelectronic devices, and full wafer thickness TSVs are required for certain microelectromechanical systems (MEMS) applications. In this work, electrolytes containing copper sulfate, an acid, chloride, and Tetronic 701 suppressor were implemented for Cu filling of high aspect ratio (10:1), full wafer thickness TSVs. For each electrolyte system, rotating disk electrode voltammetry was used to identify a voltage range for bottom-up Cu filling in the TSVs. Die level feature filling was performed using voltage ramping, which moved active deposition through the vias to yield void-free Cu features. During voltage-controlled deposition experiments, current was measured, and a characteristic current minimum was identified, which is presented as a process endpoint detection method for TSV Cu filling.[1]

To transition these Cu plating processes from the die to wafer level, experiments were performed to identify parameters required for wafer level plating. Since wafer level electroplating tools often do not have reference electrodes, a current-controlled deposition method was developed at the die level. To scale the deposition process from small 1 cm^2 samples to a full wafer, multi-die scaling experiments were performed to evaluate how current scales with active plating area. Since vias along a rotating wafer's radius have different linear velocities, rotation rate studies were conducted to observe the relationship between fluid flow and Cu fill profile. Future work will transition these results to a wafer level plating capability to produce full wafer thickness Cu-filled TSVs for MEMS and other microelectronics applications.[2]

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Chapter 1: Overview, Introduction, and Background

1.1 Chapter Overview

Chapter 1 discusses the motivation for this work, which is ultimately the development of high aspect ratio (AR), full wafer thickness Cu TSVs for advanced packaging of MEMS. Electrochemical deposition (ECD) processes have been developed for full wafer thickness TSVs that have a 5:1 AR,[3-5] but this work focuses on the development of robust plating procedures for 10:1 AR features.[1] The semiconductor fabrication process for forming these TSVs is discussed, and this work specifically focuses on the Cu electrodeposition step. This chapter outlines Cu electrodeposition fundamentals, additive-based plating electrolytes, the Curvature Enhanced Adsorbate Coverage (CEAC) and S-shaped Negative Differential Resistance (S-NDR) mechanisms,[6,7] deposition phenomenon in single suppressor additive electrolytes, and plating results for 5:1 AR TSVs.

Chapter 2 expands upon the problems involved with scaling Cu ECD processes from 5:1 AR TSVs to 10:1 AR features. Due to the change in geometry, process parameters that successfully filled the 5:1 AR features did not directly translate to fill the 10:1 AR TSVs, and these initial experimental results are shown. Chapter 2 outlines the experimental process used for plating development in the 10:1 AR features, which includes electrolyte preparation, rotating disk electrode (RDE) voltammetry, the electrodeposition laboratory setup, and sample characterization.[1]

In Chapter 3, the results for ECD experiments in full wafer thickness, 10:1 AR TSVs are discussed in detail. Experiments were performed in electrolytes containing copper sulfate ($CuSO_4$), either methanesulfonic acid (MSA) or sulfuric acid (H_2SO_4), chloride, and Tetronic 701, and RDE voltammetry was used to characterize each electrolyte. The high Tetronic 701 concentration (≥ 25 μM), high chloride (~ 1 mM), MSA-based electrolytes provided too narrow and operational window for robust bottom-up ECD processes in these 10:1 AR features, even though these electrolytes have been previously successful in filling 5:1 AR TSV features.[3,4] The results presented in this chapter show that a low chloride (~80 μM), H_2SO_4 electrolyte can be used to produce a robust, voltage-controlled plating process at the die level.[1]

Chapter 4 presents an electrical Cu endpoint detection method, analogous to endpoint detection in a deep reactive ion etching (DRIE) tool. During voltage-controlled deposition, the measured current data showed a characteristic current transient. This chapter discusses using this current feature, which is observed as a current dip, for Cu fill endpoint detection during electrodeposition and discusses how this detection method could impact both die level experiments and production scale full wafer plating.[1]

In Chapter 5, experiments are presented that will help transition the die level, voltage-controlled plating experiments to current-controlled, wafer level plating. A die level current-controlled process is presented, which was developed from the measured current data during voltage-controlled deposition. Results from die size scaling experiments and rotation rate studies are also presented to evaluate how current scales

with active plating area and how rotation rate impacts TSV Cu fill profile, respectively. These data will be used to establish operational windows for applied current and wafer rotation rate during wafer level plating development.[2] Finally, Chapter 6 outlines future work for wafer level plating, which will ultimately result in a Cu plating process for full wafer thickness TSVs for MEMS and other microelectronics applications.

1.2 Introduction: Cu-filled TSV Interconnects for MEMS Applications

TSVs are a critical interconnect technology enabling 2.5D, 3D, and heterogeneous integration of microelectronics devices.[8,9] TSVs aid in overall system miniaturization and can increase device input/output, since TSV interconnects are embedded in the substrate volume as opposed to wire bonds on the device periphery.[4] Cu-filled TSVs, which have high thermal conductivity and low electrical resistivity, can minimize electrical parasitics, improve thermal management, and lead to a clean, streamlined die stacking assembly process.[4] In the microelectronics industry, TSVs can be utilized for applications such as high bandwidth memory, photonic integrated circuits, application specific integrated circuits (ASICs), and MEMS.[1,8] Wafer thinning is commonly employed to achieve high density, fine-pitch TSVs; however, certain MEMS accelerometers require full thickness silicon substrates (≥ 600 μm) for operation, which creates a need for full wafer thickness TSVs. Some MEMS applications also need full thickness silicon substrates to maintain structural rigidity, alleviate stress caused by film deposition during fabrication, and preserve wafer flatness.[4] In this work, the TSVs discussed span a full wafer thickness of 625 μm and are intended for advanced packaging of MEMS.[1]

To fill these TSVs, Cu electrodeposition was performed using an acidic $CuSO_4$ electrolyte with additives, which enable bottom-up filling of deep inlaid features. Traditional additive-based plating chemistries consist of levelers, accelerators, and suppressors, but a single suppressor additive chemistry was utilized in this work and consists of $CuSO_4$, an acid (either H_2SO_4 or MSA), chloride, and Tetronic 701 suppressor additive. In previous work, a void-free electrodeposition process was developed for 5:1 AR TSVs (600 μm deep, 125 μm wide). Bottom-up, void-free filling has been achieved in these 5:1 AR features using both MSA- and H_2SO_4-based $CuSO_4$ electrolytes through both potentiostatic and galvanostatic deposition methods.[3-5] However, more narrow (higher AR) TSVs are desirable for increasing interconnect density and input/output, while still spanning a full wafer thickness. When scaling the AR of these features, the ideal plating parameters for Cu ECD in 5:1 AR TSVs did not produce bottom-up filling in 10:1 AR TSVs, as can be seen from Figure 1. Both samples were plated at -640 mV (MSE) in a 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 μM Tetronic 701 electrolyte. These results show that ideal parameters for plating in one geometry do not directly translate to another geometry.[1]

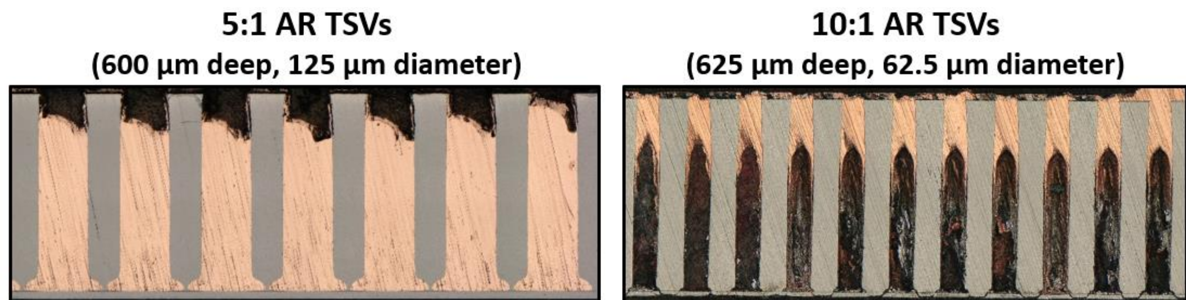


Figure 1. Impact of via geometry on Cu ECD under constant plating conditions. The ideal plating parameters for 125 μm diameter, full wafer thickness TSVs did not produce bottom-up filling in 62.5 μm diameter TSVs. Both samples were plated at -640 mV (MSE) at 400 rpm in a 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 μM Tetronic 701 electrolyte.[1,3] Adapted with permission.

The results presented in this work regarding 10:1 AR full wafer thickness TSVs build upon the previous plating work in 5:1 AR TSVs.[3-5] Further process development was needed to produce a robust die level Cu ECD procedure in the 10:1 AR features, due to the change in geometry, which impacts fluid replenishment. Process tuning included changing electrolyte composition, altering solution constituent concentrations, and modifying the applied voltage,[1] and a summary of this development work is presented here. The intent of this work is to produce a production scale wafer level plating process for full wafer thickness TSVs for MEMS applications. Since wafer level plating tools require current-control, a current-controlled process was derived from the die level voltage-controlled process. Other problems can arise when scaling a process in a small 200 mL plating path to a large 10 L production level plating tool. For example, TSVs along a rotating wafer's radius move at different linear velocities, so studies were performed to analyze the impact of fluid flow on Cu fill profile. When transitioning from small die samples to a full wafer, the relationship between applied current magnitude and active plating area must also be determined through die size scaling studies.[2] Ultimately, future work will build upon these results to produce a production scale wafer level plating capability.

1.3 TSV Fabrication Process Overview

1.3.1 General Processes for Fabrication of TSVs

TSV fabrication processes vary depending on the application and requirements but are classified into three main categories, depending on the point at which they are

formed in the overall fabrication process. These categories include via-first, -middle, and -last.[10] Via-first means that TSV fabrication occurs before CMOS front-end-of-line processing (FEOL). Via-middle is when TSV integration occurs after FEOL but before CMOS back-end-of-line (BEOL) processes. Via-last schemes place TSV fabrication after BEOL processing.[10]

The fabrication process steps for via-mid or via-last integration are depicted in Figure 2.[10,11] Prior to the first step, a hard mask and photoresist are deposited, followed by photoresist patterning and etching of the hard mask.[12] Then, the via opening is etched in the substrate through deep reactive ion etching (DRIE).[10,12] After the etch is complete, an insulating layer, such as silicon dioxide (SiO_2) or alumina (Al_2O_3), is deposited to electrically isolate the vias.[10] A barrier layer is then deposited to prevent Cu electromigration and diffusion, and tantalum nitride (TaN) or titanium nitride (TiN) are common materials for barrier layers.[10] Following the barrier layer, a seed metal is deposited, which provides a conformally conductive surface. During Cu electrodeposition, electrical contact is made with the seed metal, which allows Cu^{2+} ion reduction to occur onto the surface. Depending on the application and requirements, subsequent processing steps can include attachment of a carrier wafer, wafer thinning, back side processing, and carrier wafer removal.[10]

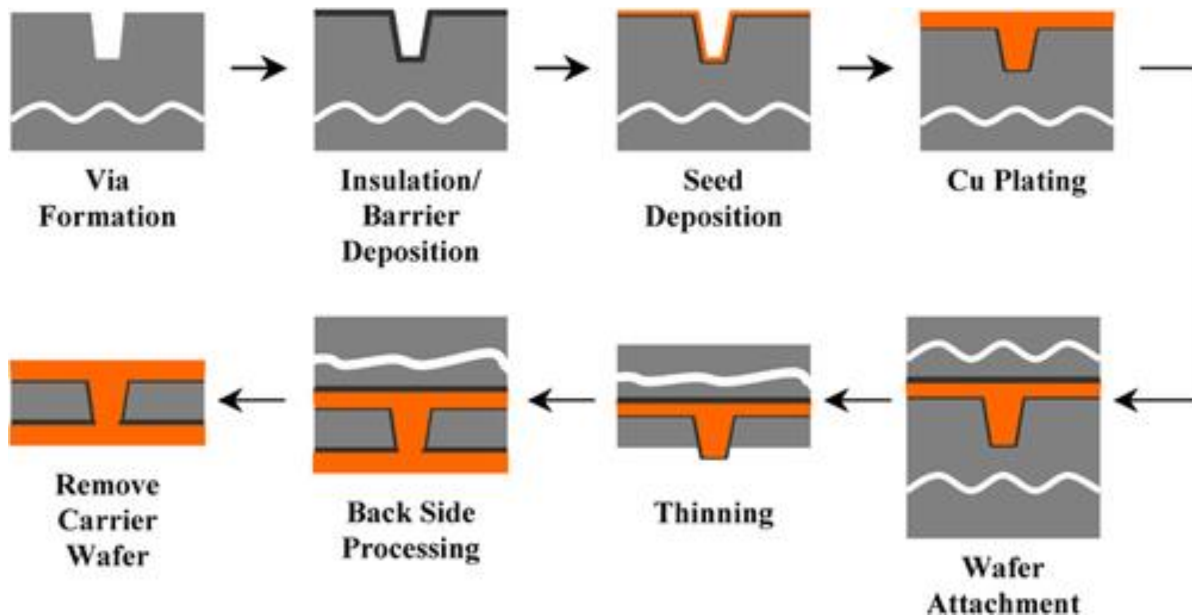


Figure 2. A multistep process flow schematic of TSV fabrication.[10,11] Reproduced from S. Burkett *et al* 2020 *J. Vac. Sci. Technol. A* 38, with the permission of AIP Publishing.

1.3.2 Fabrication Processes for High Aspect Ratio, Full Wafer Thickness TSVs

Although industry commonly uses wafer thinning after Cu ECD to achieve high density TSV interconnects, the TSVs discussed here span a full wafer thickness for MEMS device requirements. These TSVs are 625 μm deep and 62.5 μm diameter and are fabricated in a silicon-on-insulator (SOI) wafer. A single die, shown in Figure 3, consist of 102 vias in total, which are contained in five sections. Four of the sections contain two rows of vias each, and every row contains 12-13 vias that have a pitch of 150 μm between each via. The fifth section consists of a cluster of three vias in the die center. The entire sample that is shown in Figure 3 is coated with Pt.

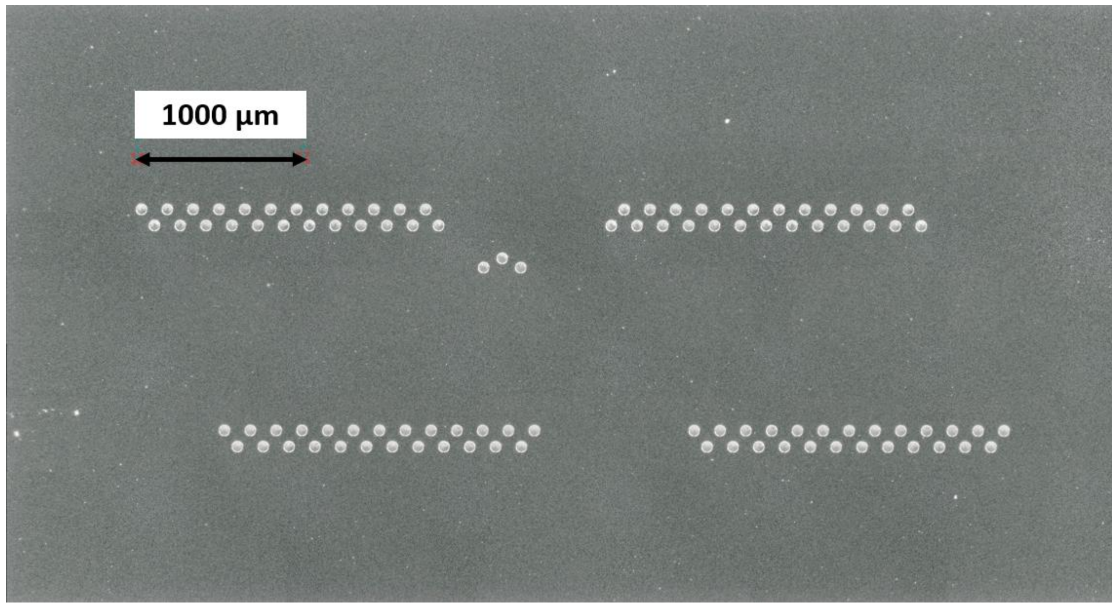


Figure 3. A single die consisting of 102 vias in five sections. The TSVs are 62.5 µm in diameter. Image stitched at 200X magnification.

The fabrication process for these TSVs starts with deposition of 1 µm of low stress nitride (LSN), 0.85 µm of amorphous Si, 6 µm of SiO_2, and 3 µm of photoresist on the backside of the wafer. After resist is patterned, the oxide, amorphous Si, and LSN layers are etched. A Bosch etch recipe is used for the deep trench etch, which forms the via structure and lands on the buried oxide (BOx) layer. Because of etch nonuniformity across the wafer, the vias are over-etched, which produces an exaggerated notched feature (Figure 4).[4,13] During the etch, this notch results from charge accumulation on the insulating oxide layer and lateral ion reflection, due to the accumulated charge repelling the incoming ionized gas molecules.[13] Si spires at the bottom of the trenches are smoothed off using a fluorine chemical downstream etch, which is followed by an oxide etch to remove the BOx at the bottom of the TSV and contact the device layer.[4] After oxide removal at the TSV bottom, Al_2O_3 is deposited as an insulating layer using

ALD, which allows for uniform coating of the TSVs, including the notched features. This insulating layer electrically isolates the vias. A spacer etch is used to clear the Al_2O_3 insulating layer at the bottom of the vias. Then, the vias are coated with ALD Pt, which functions as a barrier layer to prevent electromigration and diffusion as well as the seed metal on which Cu deposition can occur.[10] For the TSVs discussed here, Cu is deposited through ECD in a solution of $CuSO_4$, acid (either MSA or H_2SO_4), Tetronic 701 suppressor, and KCl using either a potential- or current-controlled deposition method. The Cu ECD process development and results are the focus of this work.

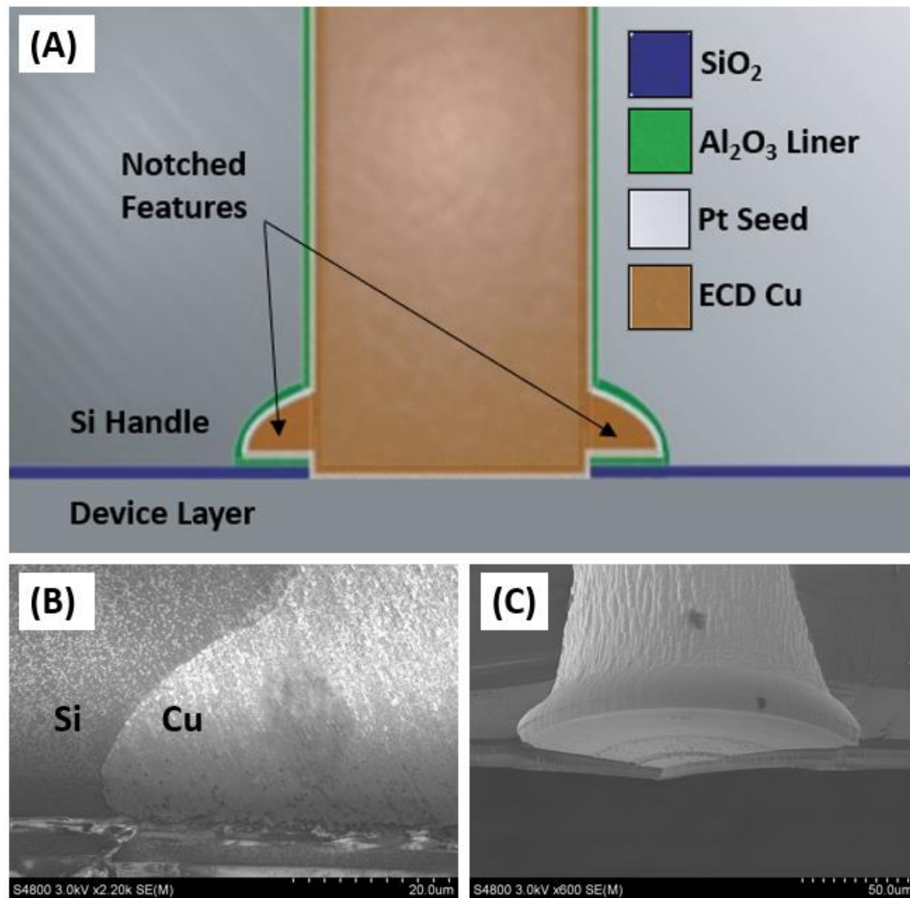
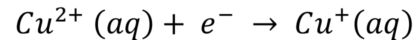


Figure 4. (A) Schematic of a TSV etched into an SOI substrate, which has an Al_2O_3 liner, Pt seed layer, and ECD Cu.[4] SEM images (B) show the Cu-Si interface at the notched feature in a Cu-plated sample, and (C) depict the notched feature in an unplated TSV from a wafer that has been scribed and broken. Adapted with permission.

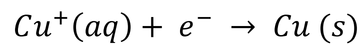
1.4 Fundamentals of Cu Electrochemical Deposition and Rotating Disk Electrode Voltammetry

1.4.1 Cu Electrodeposition Fundamentals

This work focuses on a specific step of Cu TSV fabrication, namely Cu electrodeposition. Cu deposition can be performed in a simple electrochemical cell using a copper salt solution, counter electrode (anode), working electrode (cathode), and power supply. As a potential is applied, electrons move away from the counter electrode and travel toward the working electrode, and anions migrate to the counter electrode and cations to the working electrode.[10] Electron transfer occurs at the cathode and anode electrode-solution interfaces, where species in solution are reduced and oxidized, respectively. At the working electrode, Cu^{2+} ions are deposited onto the electrode surface in a two-electron reduction. The simple two-step reduction reaction that occurs at the cathode is shown below.



$$Cu^{2+}\,(aq) + e^{-} \rightarrow Cu^{+}(aq)$$



$$Cu^{+}(aq) + e^{-} \rightarrow Cu\,(s)$$

In a TSV experimental setup, the TSV sample substrate operates as the working electrode, and electrical contact is made through the conductive seed metal coating the sample. Three electrode cells, which include a reference electrode, can be used along with a potentiostat to control the voltage between a reference electrode and the working electrode. A three-electrode schematic is depicted in Figure 5.[14] Current moves only between the working electrode and counter electrode, with ideally no current moving through the reference electrode.[14] Similarly, during current-controlled

deposition, a reference electrode can be used to measure voltage as a constant current is applied.

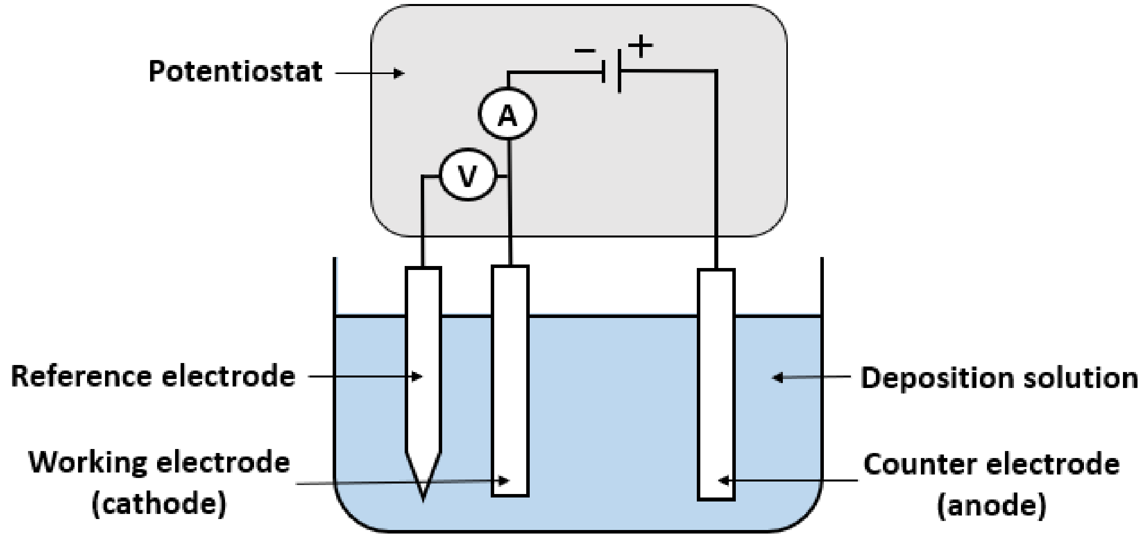


Figure 5. Three-electrode setup schematic used for Cu electrodeposition in TSVs. Current, from a power supply, moves between the counter and working electrodes. A potentiostat monitors the voltage difference between the reference and working electrodes.[14] Figure adapted from M. Kemell *et al* 2005 *Crit. Rev. Solid State Mater. Sci*. 30, 1. Obtained permission for reuse.

1.4.2 The Rotating Disk Electrode System

The rotating disk electrode (RDE) system has a very well-defined fluid flow pattern, in which fluid steadily flows toward the RDE from bulk solution and is expelled outward as the RDE rotates (Figure 6).[15] The solution near the RDE-solution interface is stationary relative to the RDE (no slip boundary). The thickness of the hydrodynamic boundary layer at the RDE is given by δ_H, where v is the kinematic viscosity of the electrolyte and ω is the angular velocity of the RDE apparatus (Equation 1.1).[16] The even thinner stationary layer closest to the RDE suface is called the diffusion layer. In Equation 1.2, δ_F is the diffusion layer thickness, and D_F is the diffusion coefficient of the

metal ion species in the electrolyte.[15] Although not directly apparent, the boundary layer thickness across a TSV sample surface correlates to that of a rotating disk electrode, as $\delta \propto \omega^{-1/2}$, meaning that faster rotation rates thin the boundary layer for better solution component transport. This will be discussed further in Section 5.2.

$$\delta_H = 3.6\, v^{1/2}\omega^{-1/2} \tag{1.1}$$

$$\delta_F = 1.61 D_F^{1/3} v^{1/6}\omega^{-1/2} \tag{1.2}$$

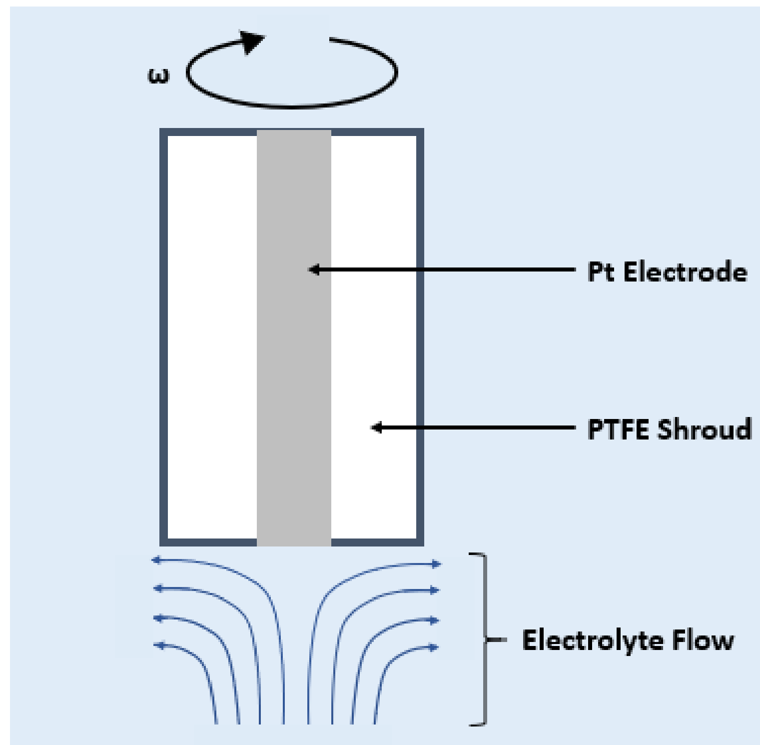


Figure 6. RDE system depicting the Pt electrode and laminar fluid flow.[15] Figure adapted from J. Nikolic *et al* 2000 *J. Chem. Educ*. 77, 1191 with permission.

1.5 Impacting Cu Deposition Profile through Pulsed Plating and Organic Additives

Cu deposition in the vias discussed here occurs from Cu^{2+} ion reduction as electrical contact is made with the conformally coated seed metal surface, which lines

the via bottoms, sidewalls, and sample surface area. Figure 7 shows three samples obtained from Cu ECD that exhibit (A) subconformal plating, (B) conformal plating, and (C) superconformal deposition.[10,17] In the absence of plating chemistry additives and under an applied bias, Cu deposition occurs preferentially on the field surface area and high up in the vias, since this area has substantial fluid flow and Cu^{2+} replenishment compared to further down in the vias. Conformal plating can occur by using a pulsed plating method, which allows for Cu^{2+} replenishment in the vias during periods when the applied bias is off or reversed.[10] It can also occur from slow deposition at a constant applied bias if the Cu deposition rate matches the ion replenishment rate throughout the TSV feature.[10] Superconformal Cu filling can occur in an electrolyte that contains plating additives under voltage-controlled or current-controlled conditions. Under certain applied current or voltage conditions, the plating additives cause preferential deposition to occur at the bottom of the via, which moves from the bottom up to fill the feature.[10,17]

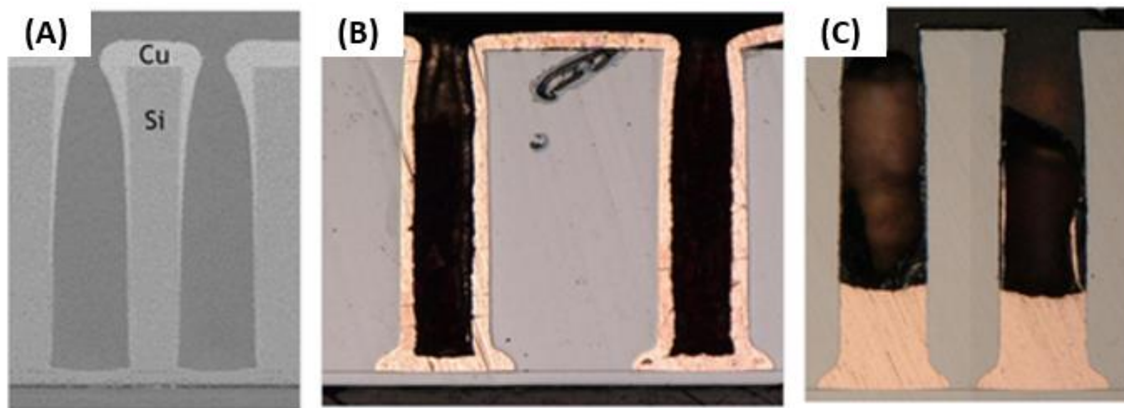


Figure 7. Samples exhibiting (A) subconformal, (B) conformal, and (C) superconformal filling. The Cu deposition in these samples occurs on a Pt seed metal that conformally coats the vias, and each deposition profile can be achieved by a unique applied electrical bias and the presence or absence of additives.[10,17] Reproduced with permission.

1.6 Plating Additives, the CEAC Mechanism, and Cu fill Profiles

1.6.1 Plating Additives

When IBM replaced aluminum-based interconnects with electroplated Cu interconnects in the late 1990s, they implemented the damascene process for Cu deposition in vias and trenches on Si chips.[18] The damascene process is derived from Cu printed circuit board plating and can fill small (micron and submicron) recessed features.[18] During the damascene process, a $CuSO_4$ solution with organic additives, specifically levelers, accelerators, and suppressors, is used to achieve superfilling in via and trench features. Although the entire substrate is coated with a seed metal layer, Cu deposition occurs preferentially in the inlaid features, because of the impact from the organic additives.[18]

Accelerators, such as bis(sodiumsulfopropyl) disulfide (SPS), increase Cu plating rate by catalyzing Cu^{+} formation, which is considered the slow step in the two-step electron reduction of Cu^{2+}.[18] Polyethylene glycol (PEG) is a commonly used suppressor additive, and Janus Green B (JGB) is an example of a leveling agent.[18] Suppressor and leveler additives inhibit Cu^{+} formation; suppressors specifically prevent Cu deposition high up in the vias, and levelers reduce Cu overburden and behave as a grain refiner.[17,18] Chloride is required for both suppressor and accelerator surface adsorption, and both additives compete for adsorption sites on the sample's metal surface.[18] The work discussed here utilizes Tetronic 701, a poloxamine suppressor additive, and its chemical structure is shown below in Figure 8.[19]

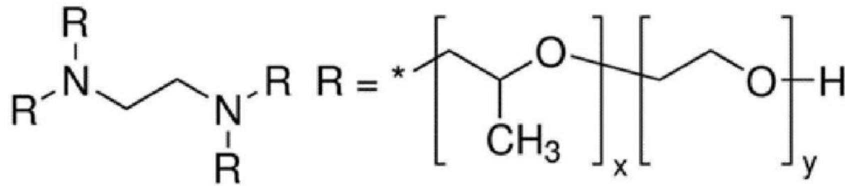


Figure 8. Chemical structure of Tetronic 701, a poloxamine suppressor additive.[19]

Diffusion coefficients for common plating additives, PEG and SPS, and Cu^{2+} are shown in Table 1. It is thought that SPS undergoes an electrochemical reaction to form sodium 3-mercapto-1-propanesulfonate (MPS), which is shown in Table 1, since it is the effective accelerant.[18,20] A simple calculation gives the approximate time scales for these plating additives to diffuse to the bottom of a 600 μm via, which are approximately 700 s, 3700 s, and 45 s for MPS, PEG, and Cu^{2+}, respectively. These diffusion timescales explain preferential Cu deposition behavior in additive-based plating electrolytes, as accelerator molecules and Cu^{2+} more quickly diffuse to the bottom of the vias, causing Cu deposition to initiate at the via bottom. Suppressor molecules have high molecular weights and slower diffusion times, leading to greater suppressor concentration at the via openings and the field surface area.

Table 1. Diffusion coefficients for common electroplating additives.

Additive	Diffusion Coefficient ($\mu m^2\ s^{-1}$)
MPS	506 [20]
PEG (MW 3k)	97 [21]
Cu^{2+}	8000 [22]

1.6.2 The CEAC Mechanism

The Curvature Enhanced Adsorbate Coverage (CEAC) filling mechanism describes how superconformal via filling can occur using accelerator additives.[10] The main principles of the CEAC mechanism are that 1) Cu growth velocity is proportional to local accelerator surface coverage and that 2) the accelerator remains at the metal-solution interface during deposition and is not consumed or expelled into bulk solution.[6,10] The impact of the CEAC mechanism is observed for metal deposition at curved surfaces on small length scales. For concave surfaces, accelerator-catalyzed metal growth causes accelerator enrichment as the metal deposit moves inward, but on convex surfaces, the outward metal growth causes catalyst dilution.[6]

The CEAC mechanism applies to Cu filling in a TSV, which is a "concave" feature. Figure 9 (A) shows the TSV, accelerator and suppressor additives, and conformal seed metal layer.[10] As Cu deposition occurs in the TSV feature and grows inward, accelerator coverage is enhanced due to the change in surface area (B), which eventually leads to a void-free fill (C).[10] Due to increased local concentration of accelerator, momentum plating occurs at the top of the feature and leads to Cu overburden.[10] At this point, the Cu growth front becomes convex (not shown in Figure 9), leading to accelerator dilution according to the CEAC mechanism.[6]

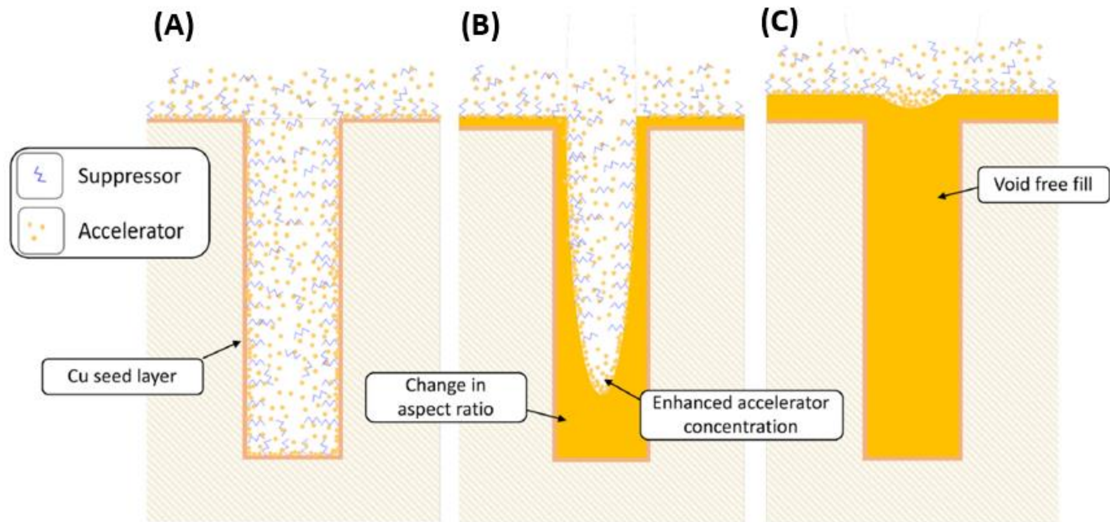


Figure 9. Schematic of the CEAC mechanism. (A) TSV, accelerator, suppressor, and conformal seed metal layer. (B) Enhanced accelerator coverage due to Cu growth on a concave surface. (C) Void-free fill and enhanced concentration of accelerator at the top of the via, which leads to momentum plating.[10,17] Figure modified from Lee & Chen 2018 *Metals* 8, 338, Copyright 2018 Author(s), licensed under a Creative Commons Attribution 4.0 License.

1.6.3 Cu Fill Profile Features Caused by Magnitude of Applied Current or Voltage

Deposition fill profile in a given electrolyte can be impacted by applied current or voltage, and ideal deposition parameters requires a balance between additive concentrations, applied current or voltage, and Cu^{2+} ion transport during deposition. Figure 10 shows cross-sections of five samples, which were plated at different current densities in a $CuSO_4$-MSA electrolyte containing three additives.[23] Figure 10 (a) shows that deposition at too low a current density (4 mA/cm^2) creates a seam void, likely resulting from a conformal Cu fill profile that closes off.[23] Due to deposition at ideal current densities of 5 mA/cm^2 and 7 mA/cm^2, which are usually experimentally determined, samples (b) and (c) show uniform, void-free deposition.[23] Using too high a current density for deposition, such as (d) at 10 mA/cm^2 and (e) at 15 mA/cm^2, leads to keyhole voids in which deposition occurs too high in the via while a voided region

remains below.[23] These results show the impact of current density of Cu fill profile. Similarly, during voltage-controlled deposition, plating at too high or low a voltage can result in deposition defects. For potentiostatic deposition, a voltage operational window can be determined through RDE voltammetry, and subsequent deposition experiments can determine ideal plating parameters. This will be discussed further in Section 1.7.

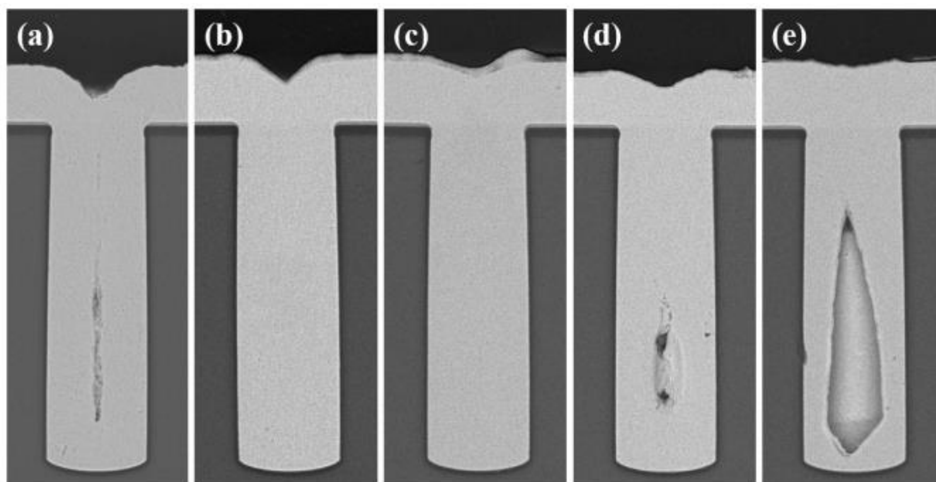


Figure 10. Cu electrodeposition results for current-controlled deposition indicating that the applied current impacts fill profile. Sample (a) shows a seam void due to too low a current density, and samples (d) and (e) show keyhole void formation that resulted from deposition at too high a current density.[23] Figure modified from F. Wang *et al* 2017 *Nature Sci. Rep*. 7, 1, licensed under a Creative Commons Attribution 4.0 License.

1.7 Suppressor-only Additive Electrolytes for Cu ECD

1.7.1 The S-NDR Mechanism

Although three to four additive systems have historically been utilized for via superfilling, this work is significant, since it implements a single suppressor additive electrolyte with no accelerator or leveler additives to achieve bottom-up Cu filling. This electrolyte contains $CuSO_4$, an acid (commonly either MSA or H_2SO_4), a single

suppressor additive, and chloride. RDE voltammetry on this electrolyte produces a scan that exhibits hysteresis in the voltage-current relationship, shown in Figure 11. This disparity in current between forward and reverse scans is caused by suppressor disruption at the cathode surface.[7] On the forward scan, suppression is eventually overcome, which is shown here around -0.65 V (MSE). At this point, breakdown of the suppressor layer is initiated and amplified by positive feedback caused by the Cu deposition reaction occurring on the electrode surface, and significant current flow is observed.[7] On the reverse scan, due to limited suppressor molecule readsorption, current is higher than on the forward scan as Cu deposition continues to occur.

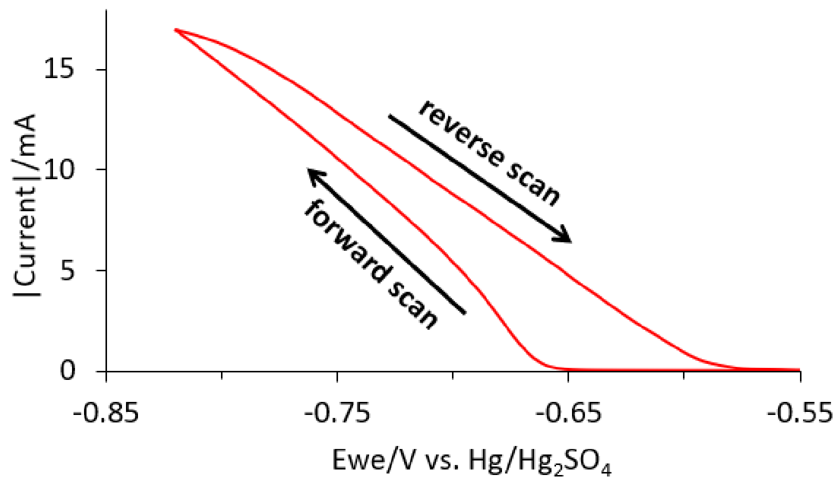


Figure 11. Cyclic voltammogram produced by RDE voltammetry in a single suppressor additive solution illustrating hysteresis in the voltage-current relationship.

Electrolytes that possess this hysteretic behavior are termed as having s-shaped negative differential resistance (S-NDR) due to the s-shaped curve resulting from IR correction using the ~3 Ω electrolyte resistance, shown in Figure 12.[7] Hysteretic voltammetry indicates bifurcating behavior in the electrolyte system, where bottom-up filling is achievable in the vias, while the field surface remains passivated by

suppressor.[7] RDE experiments performed on such electrolytes provide a rough operational window of voltages that that can achieve bottom-up filling. The filling voltages usually lie in the passive region of the forward scan, which is the window from ~-0.50 V to -0.65 V (SSE) in Figure 12 (A).[7] The cross-sections plated for 4 minutes each in this electrolyte show overplating at -0.66 V, bottom-up filling at -0.60 V, and minimal deposition at the more positive voltage of -0.54 V.[7] Overactivation at -0.66 V results from implementing a deposition voltage too negative relative to the breakdown voltage (at ~-0.65V), since that large overpotential is able to overcome suppressor adsorption high up in the vias. Conversely, plating at a voltage far right on the curve (-0.54 V) shows minimal Cu deposition due to insufficient overpotential, which cannot effectively overcome suppressor behavior. Within the hysteretic region, an ideal voltage of ~-0.60 V was identified that could initiate bottom-up filling.[7]

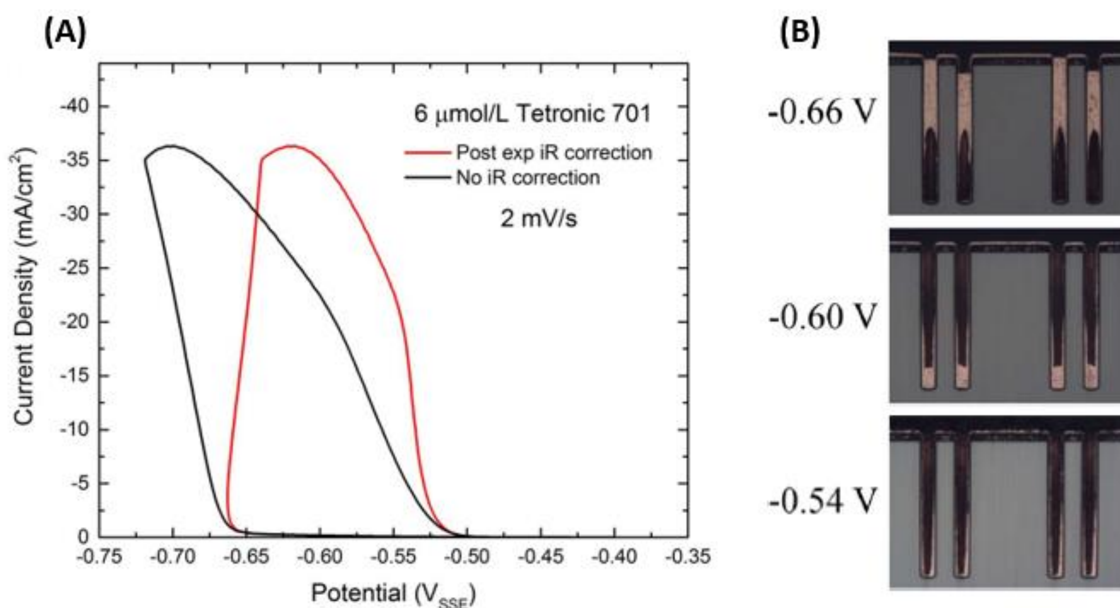


Figure 12. (A) Cyclic voltammetry scan showing raw data and IR correction. (B) Samples from Cu deposition in an electrolyte of 1 M $CuSO_4$, 0.5 M H_2SO_4, 1 mM chloride, and 6 μM Tetronic 701 rotating at 100 rpm.[7] Figure modified with permission from D. Josell & T. P. Moffat 2018 *J. Electrochem. Soc.* 165, D23.

1.7.2 Mechanism for Suppression through Additive and Chloride Coadsorption

Suppressive behavior in the S-NDR electrolyte system discussed here occurs from the coadsorption of suppressor molecules with chloride ions on the substrate's metal surface. Therefore, the level of suppression in an S-NDR electrolyte system can be controlled through both suppressor molecule concentration and chloride concentration. Figure 13 displays cyclic voltammetry (CV) scans that illustrate the tunability of suppressor behavior in the electrolyte system using both Tetronic 701 suppressor concentration and chloride ion concentration (from KCl). In the figures, linear current-voltage relationships are observed for 0 μM Tetronic 701 (A) and 0 μM KCl (B), indicating that both additives are required for hysteretic behavior in the CV scan and are involved in coadsorption for suppression. Figure 13 (A) shows that increasing suppressor concentration while chloride is held constant shifts the CV curve to the left, and the breakdown voltage occurs at a more negative potential, thereby demonstrating increased suppression. Similarly, (B) shows that increasing chloride concentration while all other concentrations are held constant also shifts the scans and breakdown voltage to more negative potentials.

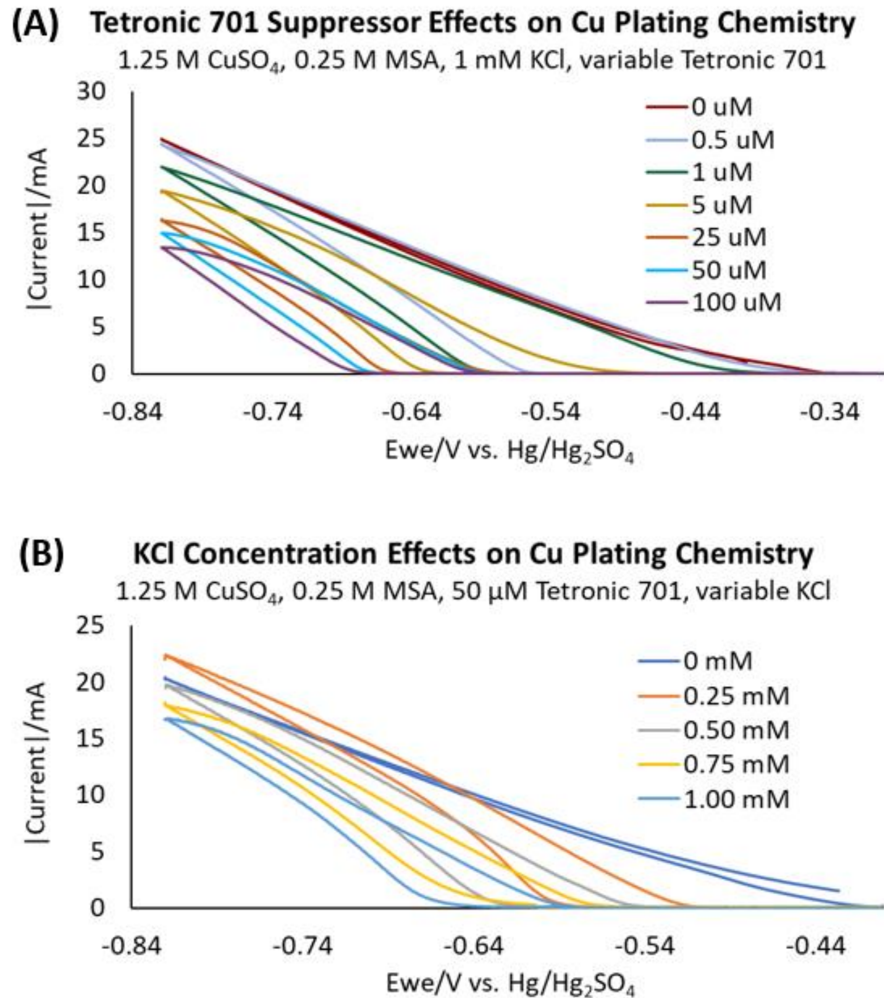


Figure 13. (A) CV scans from an electrolyte containing 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and variable Tetronic 701 concentration. (B) CV scans from an electrolyte containing 1.25 M $CuSO_4$, 0.25 M MSA, 50 μM Tetronic 701, and variable KCl concentration.

1.7.3 Filling Phenomena in Suppressor-only Systems

For a given TSV geometry, bottom-up, void-free filling in a suppressor-only electrolyte relies on fine tuning of electrolyte composition and applied electrical bias.[1] For some combinations of TSV geometry and electrolyte (particularly those containing high suppressor and chloride concentrations) a constant applied bias can result in sustained bottom-up Cu growth that leads to a completely filled feature.[3,5] When

performing ECD in systems with low suppressor behavior (such as an electrolyte with low chloride concentration), active Cu deposition can initiate at a specific height on the feature side wall.[5] The location of this passive-active transition on the TSV sidewall is based on the height in the via at which the suppressor-chloride passivation layer breaks down. This blocking layer's formation is limited by chloride flux, and its breakdown correlates to the magnitude of the applied overpotential.[24] The localized deposition grows inward toward the via center and requires an increasingly negative applied potential to move active deposition vertically through the feature.[5] As Cu filling occurs and the TSV AR changes, the growth mode can shift, and a constant voltage can be used to fill the rest of the feature.[1]

1.8 Previous Work on Cu ECD in 5:1 AR, Full Wafer Thickness TSVs

Cu deposition has been demonstrated using single-suppressor additive electrolytes in full wafer thickness vias that were ~600 μm thick and 125 μm in diameter, which is a 5:1 AR.[3-5] Voltage-controlled deposition was used to achieved void-free, bottom-up filling in these features using three different electrolyte systems: 1) a $CuSO_4$-MSA electrolyte with 50 μM Tetronic and 1 mM chloride, 2) $CuSO_4$-H_2SO_4, 35-50 μM Tetronic, and high chloride concentration (1 mM chloride), and 3) $CuSO_4$-H_2SO_4, 40 μM Tetronic, and low chloride concentration (80 μM chloride).[3,5] Galvanostatic plating conditions have also been derived to fill these geometries using the $CuSO_4$-MSA electrolyte,[4] but voltage-controlled deposition is the focus of this section.

The results in Figure 14 were obtained through potentiostatic Cu ECD in an electrolyte containing 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 μM Tetronic 701.[3] Voltammetry on this electrolyte (not shown) gave a potential window of suppressor-chloride passivation layer disruption at -0.67 V and repassivation at -0.59 V (MSE).[3] Deposition outside of this window at -0.70 V caused keyhole void formation due to electrodeposition at too negative a voltage. Samples plated at -0.64 V and -0.66 V show bottom-up, void-free filling, and the small voided regions near the TSV bottoms in the -0.66 V sample are possibly caused by merging of the over etched TSV notches.[3] The sample plated at -0.62 V shows minor seam void formation likely due to conformal deposition that grew toward the TSV center. The asymmetry in the -0.62 V sample image, which shows the seam void on the rightmost TSVs and apparent uniform filling on the left, is due to the cross-section not capturing the center of all TSVs.[3] Figure 14 (B) depicts -0.64 V potentiostatic deposition growth evolution in time, as cross-sections were obtained at 1, 2, 4, and 6 hours during deposition.[3] This extreme bottom-up filling that grows through the via at a sustained potential is a characteristic of a high suppressor concentration (>25 μM Tetronic) and high chloride concentration (~ 1 mM KCl) electrolyte system, due to high suppression confining deposition to the via bottoms at a specified potential range.[5,7]

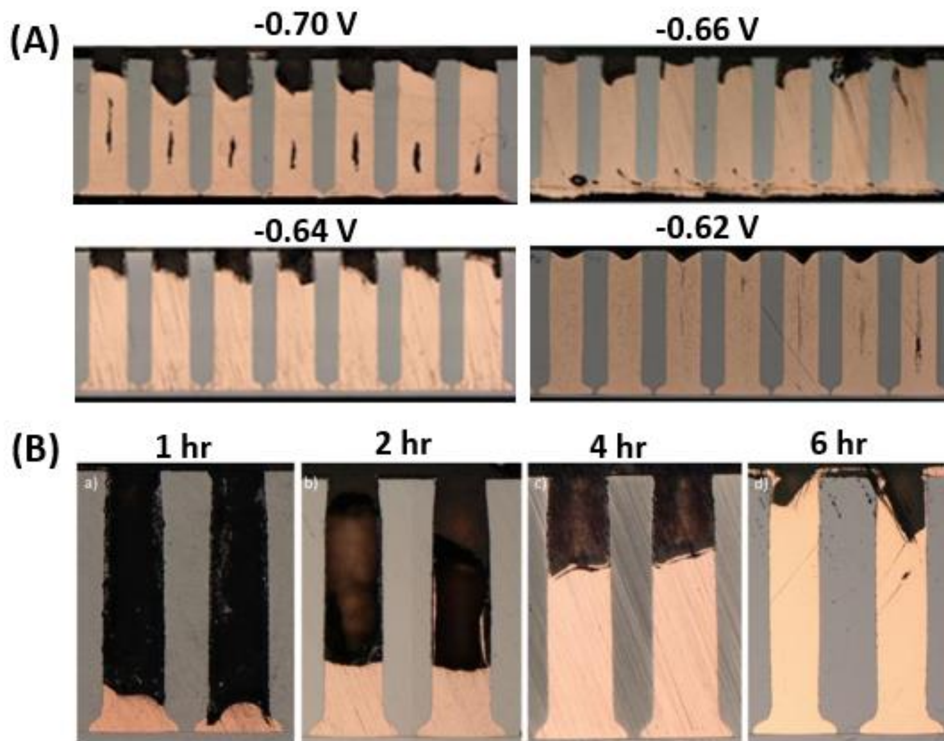


Figure 14. (A) Cross-sectioned 125 μm diameter TSVs from potentiostatic deposition in an electrolyte of 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 μM Tetronic 701. The samples rotated at 400 rpm. (B) Cu deposit evolution over time at a sustained potential of -0.64 V.[3] Figure modified with permission from L. A. Menk *et al* 2019 *J. Electrochem. Soc.* 166, D3066.

Void-free filling results were also achieved potentiostatically in a high chloride, high suppressor concentration electrolyte consisting of 1 M $CuSO_4$, 0.5 M H_2SO_4, 35-50 μM Tetronic, and 1 mM chloride, and Cu ECD was performed based on the window provided by previous hysteretic voltammetry.[5] Applying a fixed voltage of -0.61 V or -0.62 V (SSE) led to sustained bottom-up filling, which can be observed by the cross-sections produced at different times during deposition in Figure 15 (A) and (B).[5] These samples show a distinct outwardly rounded growth front feature, due to the highly passivated sample side walls in the high chloride, high suppressor concentration electrolyte.[5]

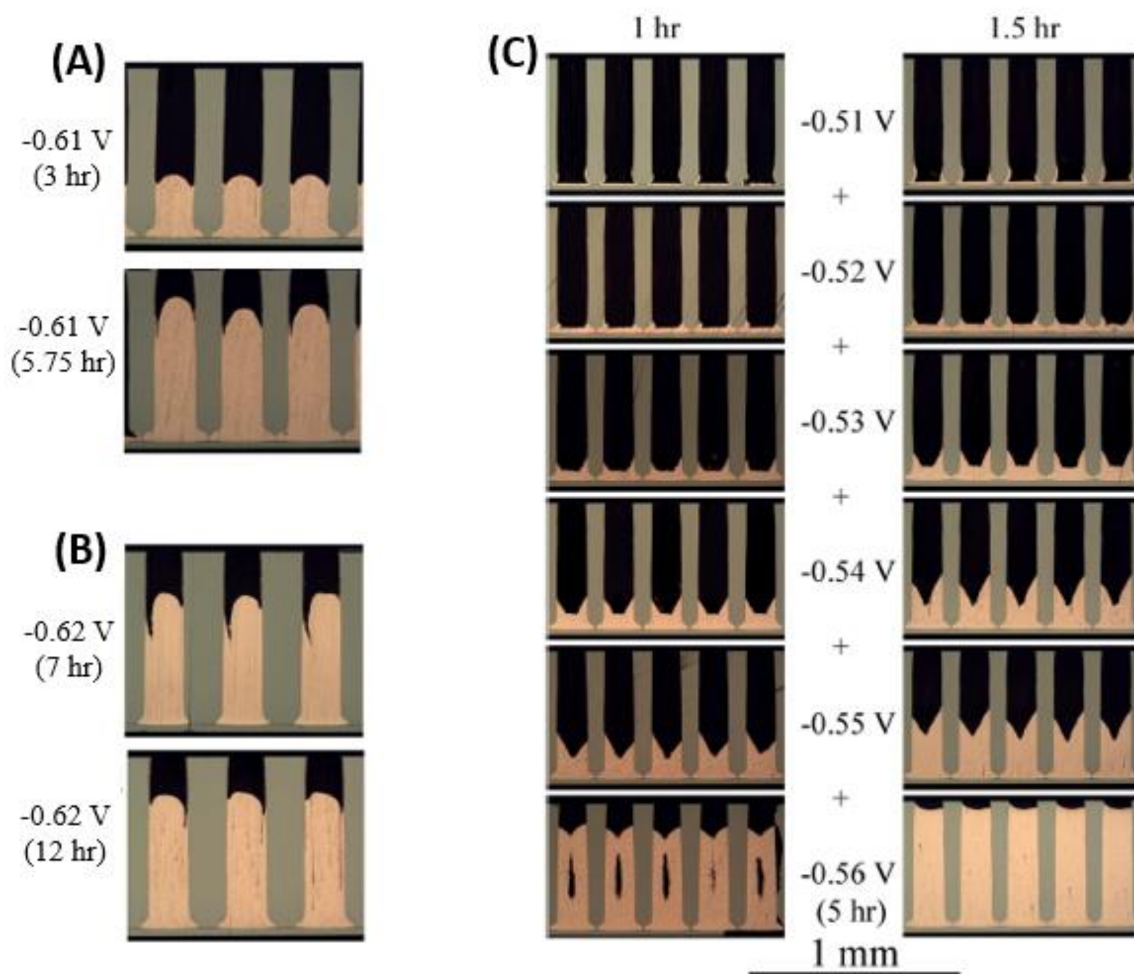


Figure 15. (A) Cross-sectioned 125 μm diameter TSVs after 3 hours and 5.75 hours of Cu deposition at -0.61 V (SSE) in a high chloride electrolyte containing 1 mM chloride and 35 μM Tetronic 701. (B) Cross-sectional TSV images exhibiting Cu deposition after 7 hours and 12 hours of plating at -0.62 V in a high chloride electrolyte of 1 mM chloride and 50 μM Tetronic 701. (C) Evolution of Cu deposition in cross-sectioned TSVs. Voltage ramping from -0.51 V to -0.55 V in steps of 0.01 V was implemented for 1-hour or 1.5-hour time intervals. The last step at -0.56 V was held for 5 hours. All samples were rotated at 400 rpm during deposition.[5] Figure modified with permission from D. Josell *et al* 2019 *J. Electrochem. Soc.* 166, D3254.

Figure 15 (C) also shows samples plated in a low chloride electrolyte with 80 μM chloride and 40 μM Tetronic 701.[5] Deposition in this low chloride electrolyte occurs with a characteristic passive-active transition that is localized at a specific height on the vias side walls based on the magnitude of the applied voltage.[5] Ramping the voltage

over time causes the localized deposition in the low chloride electrolyte to move through the TSV feature. Figure 15 (C) shows the Cu deposition over time as the voltage is stepped from -0.51 V to -0.55 V (SSE) in 10 mV increments, with the final step being held at -0.56 V for 5 hours.[5] The samples electroplated for timestep durations of 1 hour show void formation, since the active-passive transition is moved through the feature prior to sufficient Cu deposition. The samples deposited for longer time intervals of 1.5 hours show void-free filling.[5] A distinctive v-shaped Cu growth front is observed in the samples plated at low chloride concentration, since deposition occurs on the side walls, which are less suppressed than the sidewalls in the high chloride, high suppressor concentration electrolytes.[5]

Chapter 2: Scaling from 5:1 to 10:1 AR TSVs and Experimental Processes for Cu ECD Development in 10:1 AR TSVs

2.1 Impact of Geometry Change on Cu Fill Profile when Scaling From 5:1 AR to 10:1 AR TSVs

In previous work, void-free, bottom-up filling of 5:1 AR TSVs (600 µm deep, 125 µm diameter) was achieved under constant voltage conditions in an electrolyte of 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 µM Tetronic 701.[3] These same plating parameters were applied to the 10:1 AR vias (625 µm deep, 62.5 µm diameter), and extremely different deposition results were obtained.[1] Figure 16 displays a scan from RDE voltammetry performed in this chemistry as well as cross-sectional filling results from potentiostatic experiments in the 5:1 and 10:1 AR TSVs.[1] For the 5:1 AR TSVs, samples corresponding to plating voltages of -600 mV, -620 mV, -640 mV, and -700 mV (MSE) are shown. The 5:1 AR TSV sample plated at -600 mV (MSE) exhibits substantial deposition (with minor voids) in the vias on the right side of the sample, while those on the left show evidence of suppression. The inconsistent filling results obtained at -600 mV (MSE) indicate that a higher overpotential is required to activate deposition in all the features. Uniform deposition was accomplished in the features for the sample plated at -620 mV (MSE), but the presence of seam voids indicates that the applied voltage was still too low. Electrodeposition at -640 mV (MSE) led to void-free filling in the 5:1 AR features. When using a more negative voltage of -700 mV (MSE), keyhole voids were observed due to suppressor desorption high up in the features.[1,3]

For the 10:1 AR TSVs, Cu ECD was performed in the same $CuSO_4$-MSA solution (with 1 mM chloride and 50 µM Tetronic 701 suppressor) at voltages of -600 mV, -620

mV, and -640 mV (MSE), and the results are also shown in Figure 16.[1] Samples obtained from potentiostatic experiments conducted at -600 mV and -620 mV (MSE) exhibit limited Cu deposition, indicating that those voltages were insufficient to break down the adsorbed chloride-suppressor layer and deposit Cu. Deposition at -640 mV (MSE), at only 20 mV more negative, resulted in Cu deposition high up in the features, leaving large voids underneath. These results indicate a small process window in which bottom-up filling might be achievable, which is indicated by suppression at -620 mV (MSE) and overactivation at -640 (MSE).[1]

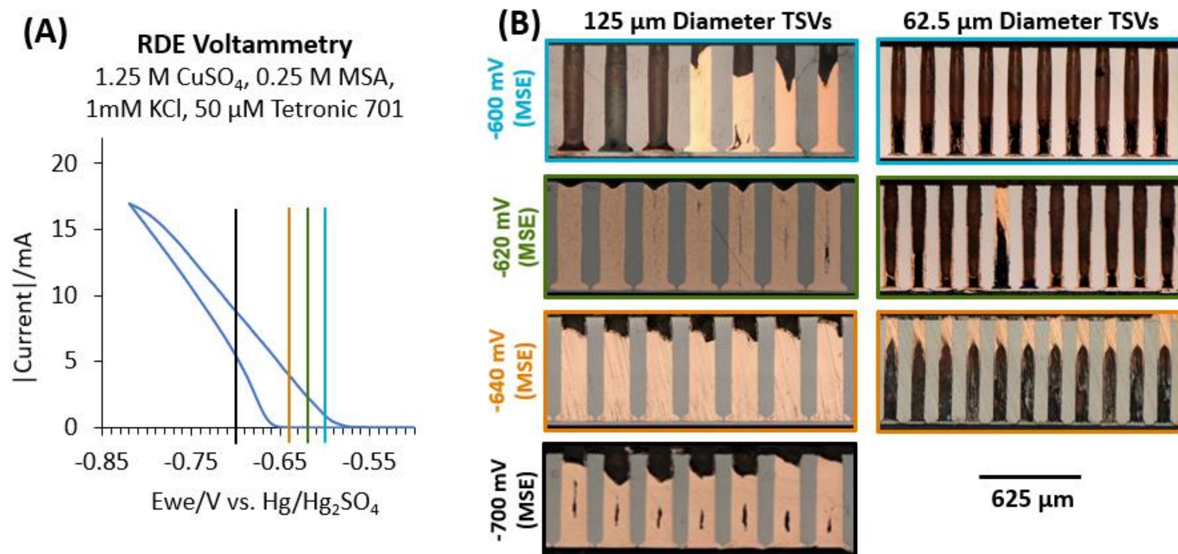


Figure 16. (A) RDE voltammetry performed in a 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 μM Tetronic 701 electrolyte. The voltages for potentiostatic ECD are indicated. (B) Mechanical cross-sections are shown for samples plated at selected voltages for 125 μm diameter (5:1 AR)[3] and 62.5 μm diameter (10:1 AR) TSVs.[1] Figure modified with permission.

The results in Figure 16 illustrate the dependence of Cu fill profile on applied bias and TSV geometry, the latter of which impacts Cu^{2+} replenishment and suppressor transport into the features.[1] Because of the small 20 mV process window observed for

the 10:1 AR TSV samples, further process development was needed to produce a robust die level plating method, and changes to the plating electrolyte composition, solution concentrations, electrical biasing methods, and sample rotation rate were investigated. The results of this development are discussed in Chapter 3. These results are built upon to produce an endpoint detection method (Chapter 4) and to transition the Cu ECD process for the 10:1 AR TSVs to a wafer level plating process (Chapter 5). Section 2.2 provides an overview of the experimental processes utilized in this study to prepare and characterize plating electrolytes, execute experiments, and analyze plated TSV samples.

2.2 Experimental Processes for Cu ECD Development in 10:1 AR TSVs

2.2.1 Section Overview

This section discusses the experimental methods used for Cu ECD process development in the 62.5 μm diameter, 625 μm deep TSVs. Plating electrolytes were prepared from stock solutions that were made in the laboratory, and these electrolytes were analyzed through RDE voltammetry. Approximately four to five TSV experiments were run in each 200 mL plating bath before replacing the electrolyte. After Cu ECD, the samples were characterized through mechanical cross-sectioning, optical microscopy, and X-ray CT scan technology.[1]

2.2.2 Electrolyte Preparation

Stock solutions of 10 mM Tetronic 701, 1 mM KCl, $CuSO_4$-MSA (1.25 M $CuSO_4$ and 0.25 M MSA), and $CuSO_4$-H_2SO_4 (1 M $CuSO_4$ and 0.5 M H_2SO_4) were prepared and used

to produce electrolytes for Cu ECD. The stock solution of concentrated Tetronic 701 required refrigeration at 4 °C, since 10 mM Tetronic 701 precipitates at room temperature. Electrolytes were prepared by adding aliquots from the Tetronic 701 and KCl stock solutions to 200 mL of either the $CuSO_4$-MSA or $CuSO_4$-H_2SO_4 solutions. In this work, the primary electrolytes utilized consisted of 1) 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 μM Tetronic 701, 2) 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 25 μM Tetronic 701, and 3) 1 M $CuSO_4$, 0.5 M H_2SO_4, 80 μM KCl, and 40 μM Tetronic 701.[1]

2.2.3 Rotating Disk Electrode Voltammetry

For this work, RDE voltammetry was used to monitor plating solution health over time, characterize plating electrolytes, and identify rough process parameters for voltage-controlled deposition. RDE voltammetry was performed at 400 rpm using a Pt RDE (Pine Research), modulated speed rotator (Pine Research), Pt anode (Pine Research), Hg/Hg_2SO_4 reference electrode (MSE, Pine Research), and BioLogic SP-200 potentiostat (BioLogic USA), and EC-lab software to scan from -0.4 V to -0.82 V (MSE) in 2 mV/s steps. To monitor the plating chemistries, RDE voltammetry was performed on electrolytes prior to running any TSV deposition experiments, and the electrolyte was replenished regularly to ensure consistent solution concentrations. RDE voltammetry was implemented to characterize the $CuSO_4$-MSA and $CuSO_4$-H_2SO_4 electrolytes, which had varying concentrations of KCl and Tetronic 701, and to identify process windows for voltage-controlled deposition in these electrolytes.[1]

2.2.4 Sample Preparation, TSV Wetting Process, and Electrodeposition Setup

Die level ECD experiments were executed using 1 cm^2 die (illustrated previously in Figure 3), which were scribed and broken from a 150 mm wafer. For sample preparation, a cleaved die was inserted into the sample slot of a machined Al rod fixture and fastened with a set screw at the bottom of the rod. The sample underside and Al rod were coated with XP-2000 stop-off (Tolber) to mask conductive surfaces not intended for Cu deposition.[1] Figure 17 (B) shows a mounted TSV sample, and Figure 17 (A) shows the experimental Cu deposition setup.

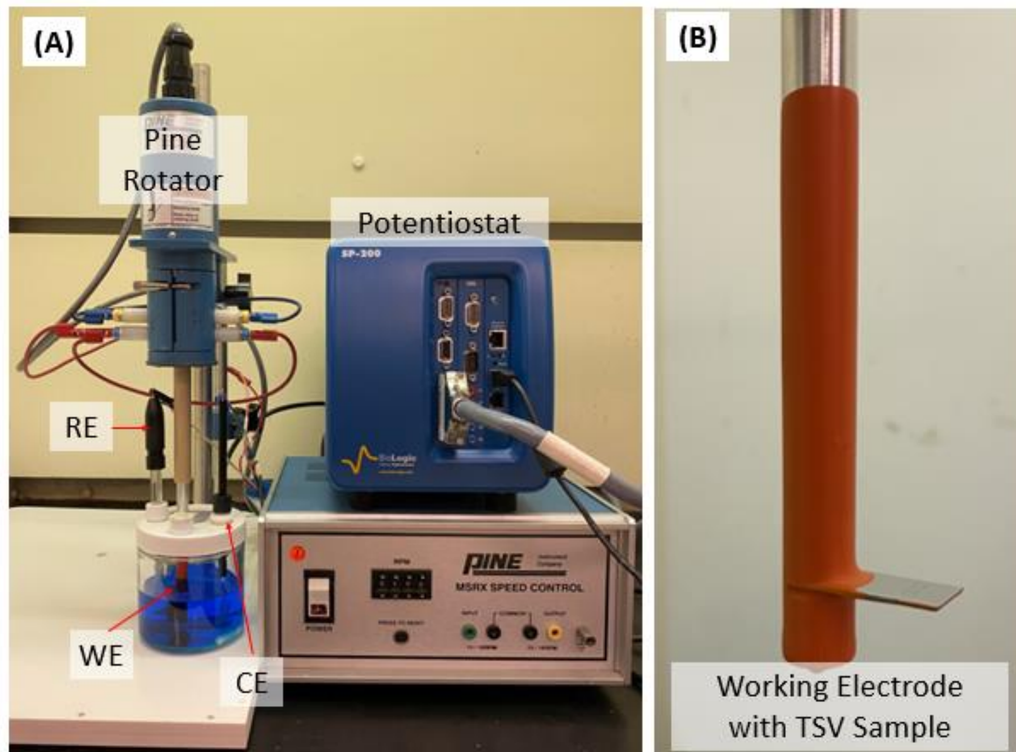


Figure 17. (A) Photograph of the ECD experimental setup, which includes a Cu plating solution, reference electrode (RE), working electrode (WE), Pt counter electrode (CE), Pine modulated speed rotator and control box, and BioLogic SP-200 potentiostat. (B) A zoom view of the working electrode, which contains a single die TSV sample with the TSVs facing upward and field surface area exposed. The remaining conductive area is masked with XP-2000.

After sample mounting and XP-2000 stop-off drying, the TSV sample underwent a prewet process in -18 °C isopropyl alcohol (IPA, Sigma Aldrich) under vacuum to remove air bubbles in the TSV features. The vacuum-based wetting process was performed in a sealed container using a roughing pump until no additional air bubbles were visible. The wetted sample was then immediately placed into the plating electrolyte solution, and the Al rod was threaded into the modulated speed rotator apparatus to facilitate fluid replenishment during deposition. Prior to applying a plating voltage, the TSV sample experienced a "dwell" or "incubation" period, in which the voltage was maintained near the open circuit potential (~0.4 V) for 1-2 minutes. During deposition experiments, plating voltages were controlled with the BioLogic SP-200 potentiostat and EC-lab software.[1]

2.2.5 TSV Fill Characterization through Mechanical Polishing and X-ray CT Scans

Evaluation of Cu fill profile in the TSVs was performed using mechanical polishing and X-ray computed tomography (CT). Mechanical cross-sectioning provides high quality sample images of Cu fill profile, but it can mask certain sample features, such as voids, since it only provides a 2D snapshot of the vias. Full 3D analysis using mechanical polishing involves extensive amounts of time cross-sectioning and imaging each row of vias. Conversely, X-ray CT scans provide a comprehensive 3D sample view; however, CT image resolution is constrained to ~5 μm. X-ray CT scans also provide a method for nondestructive imaging of plated TSV samples. The combination of these two sample characterization methods leads to robust, thorough sample analysis.[1]

Cu-plated TSV samples were potted prior to cross-sectioning to protect sample structural integrity during mechanical grinding. Epoxybond 110 fast curing epoxy was distributed over the via openings, and the sample was placed under vacuum for 10 minutes to ensure epoxy infiltration into the vias. After the vacuum process was complete (when no more air bubbles emerged from the vias), the TSV sample was coated with excess epoxy and embedded between two glass slides. Subsequently, the sample was pressurized at 32 PSI in a small chamber (Allied High Tech Products) for 10 minutes. The Epoxybond 110 was then cured at 175 °C for ~5 minutes or until a reddish-brown color change was observed. Sample cross-sectioning was performed using an Allied MultiPrep polishing tool, silicon carbide (SiC) pads, and diamond polishing films (Allied Type B). A rough SiC pad was used to remove bulk material from the outer edge of the TSV sample; then, diamond lapping pads of 30 μm to 0.5 μm grit were implemented in order of decreasing grit size for finer material removal. Allied Red Final C polishing pads and a 0.05 μm colloidal silica suspension were used to polish the sample cross-section, which was photographed at 300X magnification using a stitching method on a Keyence optical microscope.[1]

X-ray CT scans were obtained for Cu-plated samples using a North Star X50 imaging tool with a Feinfocus FXE X-ray source, which was operated at 220 KV and 5.5 W, and Varex 2520 DX detector, 630 mm away from the source. The sample was mounted with a 45° offset at distance of 30 mm from the source. The system recorded 8000 projections (3 frames per projection) at 21X magnification, and North Star efX-CT software was implemented for data reconstruction. Using the rendered model, video files were generated that showed a comprehensive view of the sample. Snapshots were

taken from the videos and are presented in Chapter 3 alongside the mechanical cross-sections to provide thorough sample characterization results.[1]

Chapter 3: Cu ECD Process Development for Filling 10:1 AR TSVs

3.1 ECD in High AR TSVs Using a Single-additive Electrolyte

As discussed in Chapter 1, high quality Cu electrodeposition for microelectronics applications can be achieved using a single-additive electrolyte containing a Cu salt, an acid, chloride, and a suppressor additive, rather than a traditional three to four additive system.[3-5] Bottom-up, void-free deposition can be achieved in TSVs in single-suppressor additive electrolytes according to the S-NDR mechanism. Here, the principles of the S-NDR mechanism were used to develop a Cu filling recipe for 10:1 AR TSV features. The plating electrolytes were analyzed through RDE voltammetry, and through the resulting scans, voltages were determined for experimentation. Sample characterization and analysis informed tuning of electrolyte composition and biasing regime. This section outlines changes made to electrolyte composition, biasing method, and sample rotation rate and describes the impact of each on Cu fill profile in the 10:1 AR features. Ultimately, this tuning process leads to bottom-up, void-free filling at the die level in these high aspect ratio geometries.[1]

RDE voltammetry was used to characterize the three plating electrolytes implemented in this work, and the resulting scans are displayed in Figure 18 alongside a scan obtained in an additive-free electrolyte. The electrolyte containing no Tetronic 701 suppressor shows a linear, Ohmic voltage-current relationship, due to relatively constant surface chemistry at the electrolyte-electrode interface during the forward (more negative) and reverse (more positive) scans. The plotted data for the $CuSO_4$-acid

electrolytes that contain Tetronic 701 suppressor show a disparity in the measured current between forward and reverse scans, and this hysteresis is due to changes in suppressor-surface interactions. On the forward scan, the poloxamine suppressor-chloride blocking layer on the RDE surface is desorbed as Cu nucleates on the surface, and on the reverse scan, much of the suppressor is already desorbed and only limitedly readsorbs. Due to the breakdown of the suppressor layer, higher current is observed and more Cu deposition occurs on the reverse scan.[1]

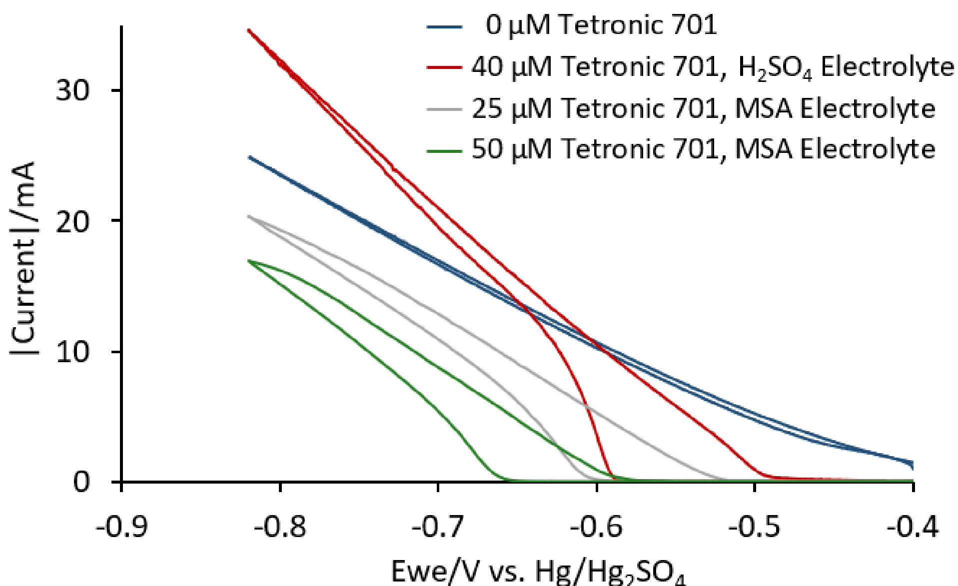


Figure 18. RDE voltammetry results from four $CuSO_4$ solutions. The suppressor-free electrolyte (0 µM Tetronic 701) shows a linear voltage-current relationship. Scans from solutions containing Tetronic 701 suppressor exhibit hysteresis. The suppressor-based electrolytes have the following compositions: 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 25 µM or 50 µM Tetronic 701 and 1 M $CuSO_4$, 0.5 M H_2SO_4, 80 µM KCl, and 40 µM Tetronic 701.[1]

Figure 18 also illustrates characteristic differences between the electrolyte systems utilized in this work. Comparing the two curves produced from voltammetry on the MSA-based electrolytes, the chemistry with a higher suppressor concentration of

50 μM Tetronic 701 exhibits a breakdown voltage that is shifted more negative relative to that of the 25 μM Tetronic 701 electrolyte, indicating a more suppressed system. The slope of the $CuSO_4$-MSA electrolyte is also lower than that of the $CuSO_4$-H_2SO_4 electrolyte, indicating a higher impedance for the MSA-based chemistry. For each of these systems, the hysteretic region yields a rough process range for bottom-up filling in each electrolyte. Applying too negative a potential relative to the hysteretic window leads to overactivation and void formation because of suppressor layer desorption high up in the vias. Due to suppressor behavior, applying too little overpotential can lead to minimal Cu deposition.[1]

3.2 Changing Applied Bias and Investigating Sample Rotation Rate

Since the plating parameters for bottom-up, void-free filling in the 5:1 AR TSVs did not produce void-free deposition in the 10:1 AR TSVs, further altering of experimental parameters was investigated, including applied bias and rotation rate. Using the same chemistry of 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 μM Tetronic 701, further potentiostatic experimentation was performed at -630 mV (MSE), since that voltage fell between the fully suppressed state (-620 mV) and overactivated state (-640 mV), which are shown in Figure 16 in Chapter 2. Pictured in Figure 19, the -630 mV (MSE) sample shows preferential deposition high up in the vias, similar to the results of the -640 mV (MSE) sample in Figure 16. A sample run at -620 mV (MSE) is shown for comparison. The 10-mV difference between a fully suppressed state (-620 mV) and overplating (-630 mV) indicates an even smaller operational window than previously observed in initial experimentation, making sustained-voltage deposition in

this chemistry challenging for the 10:1 AR TSV geometry. It is possible that plating at -625 mV would lead to bottom-up filling, but this was not investigated, since such a sensitive plating process would not meet future needs for wafer level plating.

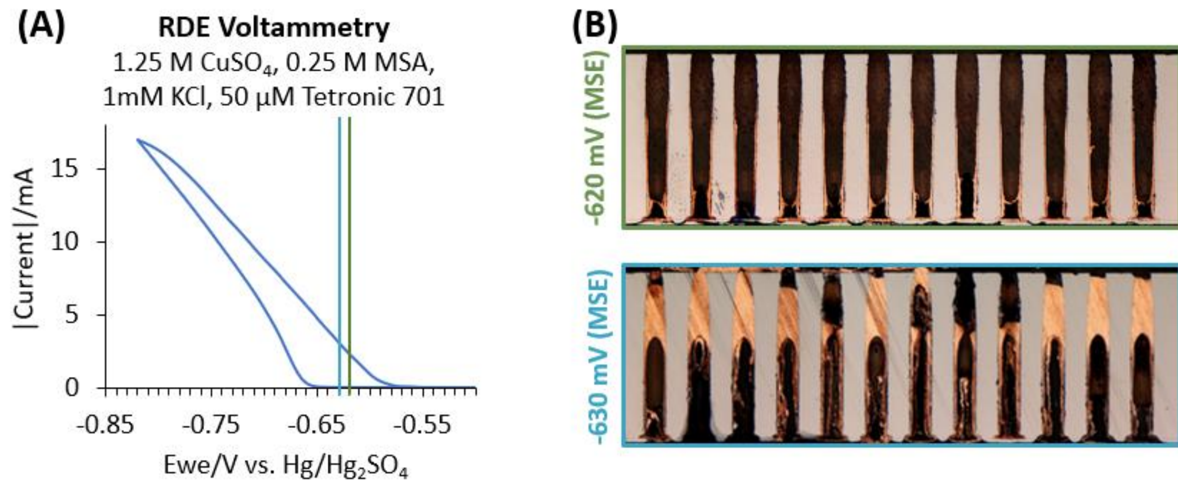


Figure 19. (A) RDE voltammetry is shown for the 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 µM Tetronic 701 solution along with voltages for potentiostatic ECD. (B) Cross-sectioned samples that were plated at -620 mV and -630 mV (MSE) and 400 rpm.

Due to the challenges of potentiostatic plating in this chemistry, different rotation rates were investigated to alter the process window, since fluid flow and mass transport are directly impacted by sample rotation rate. Rotation rate experiments were performed at -620 mV since that voltage showed underplating rather than system overactivation. Figure 20 shows the cross-sectioned samples plated at -620 mV for 4 hours and rotated at 25, 100, 400, or 800 rpm. Although the samples show little to no Cu deposition in the vias, they have characteristic differences due to the different rotation rates, which correlate to the measured current data. The slowly rotating samples (25 rpm and 100 rpm) show significant deposition on the field surface area, likely due to the slower fluid flow and limited suppressor transport to the sample

surface, which allows Cu deposition to occur there. The high current (> 1 mA) observed for the 25 rpm and 100 rpm samples correlates to the substantial Cu plating at the top of the vias and on the field surface area. The 400 rpm and 800 rpm samples show almost no Cu deposition in the vias or on the sample surface, and the measured current is lower for both samples (~ 0.5 mA). Although these results did not produce bottom-up Cu deposition, the data are still beneficial, as they show the impact of die level rotation rate on suppressor transport and adsorption.

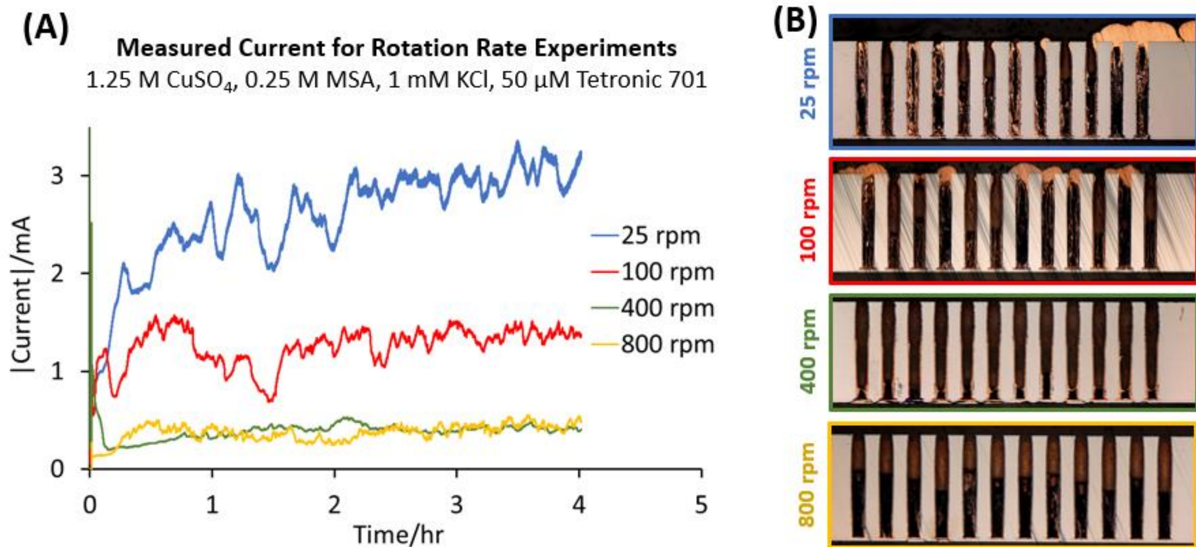


Figure 20. Rotation rate experiments for samples electroplated at -620 mV (MSE) in the 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 µM Tetronic 701 electrolyte. (A) The measured current magnitude is inversely proportional to rotation rate, due to amount of suppressor readsorption. (B) Sample cross-sections for each rotation experiment.

Additional experiments were conducted in the 1 mM KCl, 50 µM Tetronic, $CuSO_4$-MSA chemistry that did not produce void-free filling. Further potentiostatic experimentation was conducted at -620 mV (MSE) and 400 rpm in the same chemistry in which dwell time was altered. Dwell time is the incubation period before plating during which the voltage is held near the open circuit potential value (~-400 mV).

Increased dwell time allows solution constituent influx into the vias before a voltage is applied. Galvanostatic experiments were also performed in this chemistry, but some of the cross-sections showed inconsistent deposition results, likely due to the narrow process window for plating in high AR vias using this chemistry. Cross-sections and CT scans for the dwell time experiments and galvanostatic depositions are shown in APPENDIX A.

3.3 Decreasing Suppression to Alter the Plating Operational Window

Due to the narrow Cu deposition window observed experimentally in the 50 μM Tetronic, 1 mM KCl $CuSO_4$-MSA chemistry, the Tetronic 701 concentration was decreased to 25 μM to lower suppressor behavior in the electrolyte. Figure 21 shows RDE voltammetry performed on both electrolytes. (These are the same curves from Figure 18 and are depicted separately in Figure 21 for clarity.) The voltammogram for the 25 μM Tetronic electrolyte is shifted right relative to the curve for the 50 μM Tetronic electrolyte due to the lower poloxamine suppressor concentration. The breakdown voltage occurs around -600 mV (MSE) rather than -650 mV (MSE), and this shift indicates a less suppressed system for the 25 μM Tetronic chemistry. Both curves are relatively narrow in width, and the disparity between current on the forward versus reverse scan is not as exaggerated as in other chemistries. In retrospect, it is evident that the small hysteretic region indicates a narrow operational window for bottom-up TSV filling.

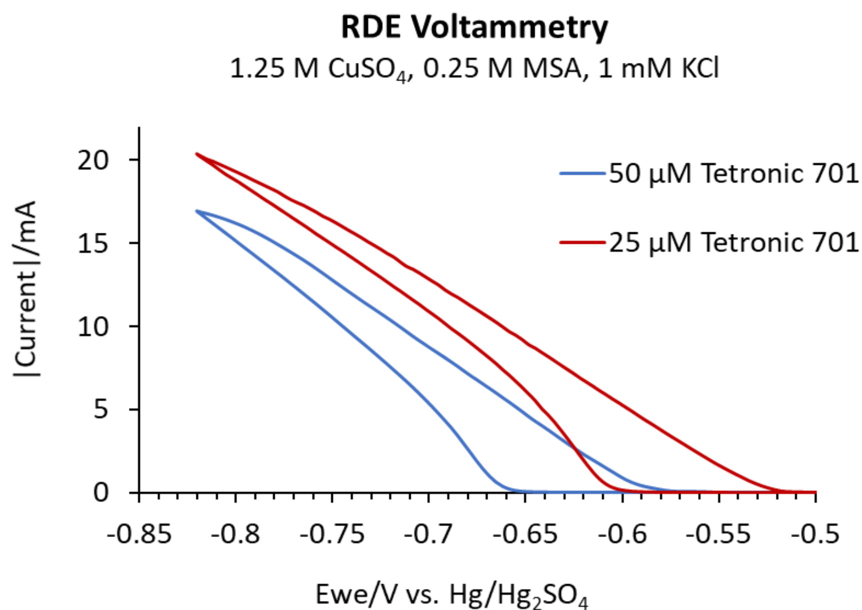


Figure 21. RDE voltammetry curves from 50 μM and 25 μM Tetronic 701 in the 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl electrolyte.

Plating voltages of -620 mV, -630 mV, and -640 mV (MSE) were used for potentiostatic experiments in the 25 μM Tetronic chemistry, and cross-sectioned samples are shown in Figure 22 (B). Deposition results at -620 mV, -630 mV, and -640 mV show signs of bottom up filling, alongside vias with Cu overplating. Due to the sporadic overplating in these TSV samples, an experiment was run at -600 mV (also displayed in Figure 22), but this sample shows minimal Cu deposition even though it was run for 15 hours. Based on the suppression observed at -600 mV and mild overplating observed just 20 mV more negative, a voltage stepping method was implemented to move deposition through the TSV features. These results are shown in APPENDIX B, but they do not exhibit void-free filling, which could possibly be related to the uncontrolled deposition observed at the various plating potentials in this chemistry.

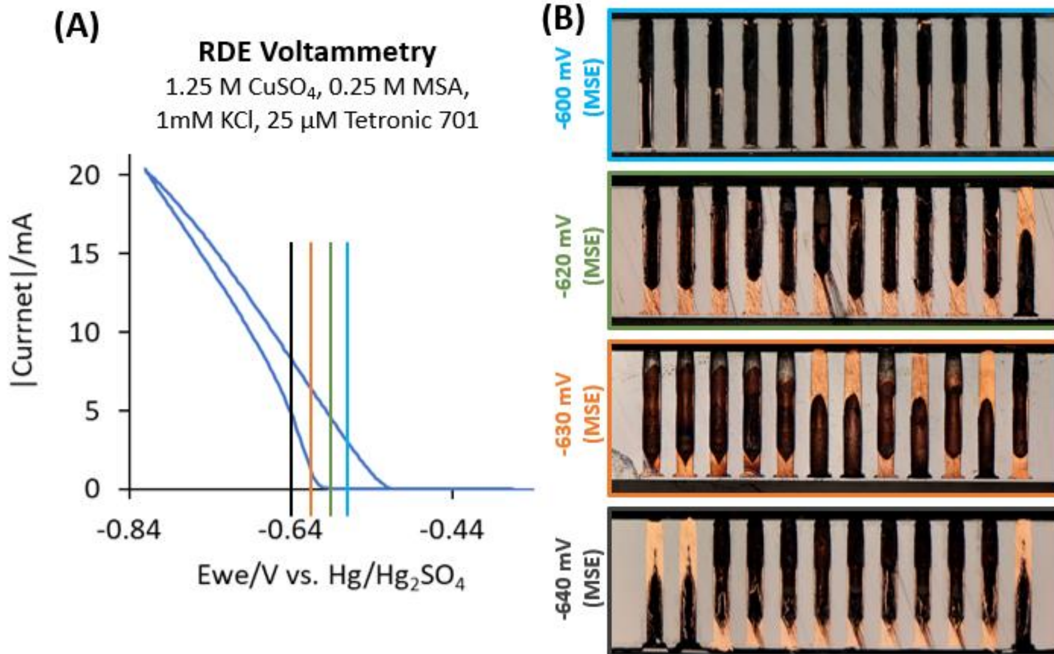


Figure 22. (A) RDE voltammetry on a 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 25 μM Tetronic 701 electrolyte. (B) Cross-sections for potentiostatic plating experiments in this electrolyte, rotated at 400 rpm. Samples were held at the voltages shown for 4 hours, except for the -600 mV (MSE) sample, which was plated for 15 hours.

It is entirely possible that decreasing the Tetronic 701 concentration further in this $CuSO_4$-MSA high chloride electrolyte would lead to a void-free filling recipe for these features, since widening of the passive range is observed from RDE voltammetry on electrolytes with lower Tetronic concentration.[7] Figure 13 (A) shows that lower Tetronic 701 concentrations in the MSA electrolyte lead to widening of the passive range, which extends the window over which bifurcating behavior can occur. Again, this bifurcating behavior includes passivation on the field surface and high up in the vias and active deposition at the bottom of the vias. However, no further work was performed in the MSA electrolyte for the 10:1 AR TSVs, and focus was shifted to an electrolyte that has been successfully implemented to fill mesoscale TSV features in literature.[5]

3.4 Void-free Filling Using Voltage Stepping in a Low Chloride Electrolyte

For the 10:1 AR TSVs, Cu ECD in the high Tetronic 701 concentration (≥ 25 μM), high chloride (~1 mM) electrolytes did not result in robust bottom-up filling processes, due to the narrow operational window observed in the 50 μM Tetronic 701 chemistry and inconsistent filling results in the 25 μM Tetronic 701 electrolyte. Therefore, the plating electrolyte composition and concentrations were altered more to widen the operational window. Since Tetronic 701 and chloride cooperatively form the suppressor blocking layer on the via walls and sample top surface, the level of suppression can be tuned by decreasing chloride concentration. (Suppression level can also be tuned through altering suppressor concentration. Slight changes in suppressor concentration drastically change the electrolyte system behavior, and a very small amount is needed for suppression to occur.) For this application, the KCl concentration was decreased from 1 mM to 80 μM, and the electrolyte implemented also consisted of 1 M $CuSO_4$, 0.5 M H_2SO_4, and 40 μM Tetronic 701.[1]

RDE voltammetry, shown in Figure 23 (A) was performed on the low chloride electrolyte to identify a voltage process window for plating in the modified chemistry.[1] Plating voltages that fell within the hysteretic window were selected for potentiostatic deposition, and the associated cross-sectional images are displayed in Figure 23 (B).[1] These results show features commonly observed in suppressor-based electrolytes, where the height of active deposition correlates to the applied overpotential. Electroplating at the largest overpotential (-570 mV, MSE) caused Cu deposition to occur at the via opening. The more positive voltages of -540 mV and -520 mV (MSE) led

to preferential deposition at the bottom and side walls of the TSVs and illustrate passive-active Cu deposition behavior at a specific height in the features.[1]

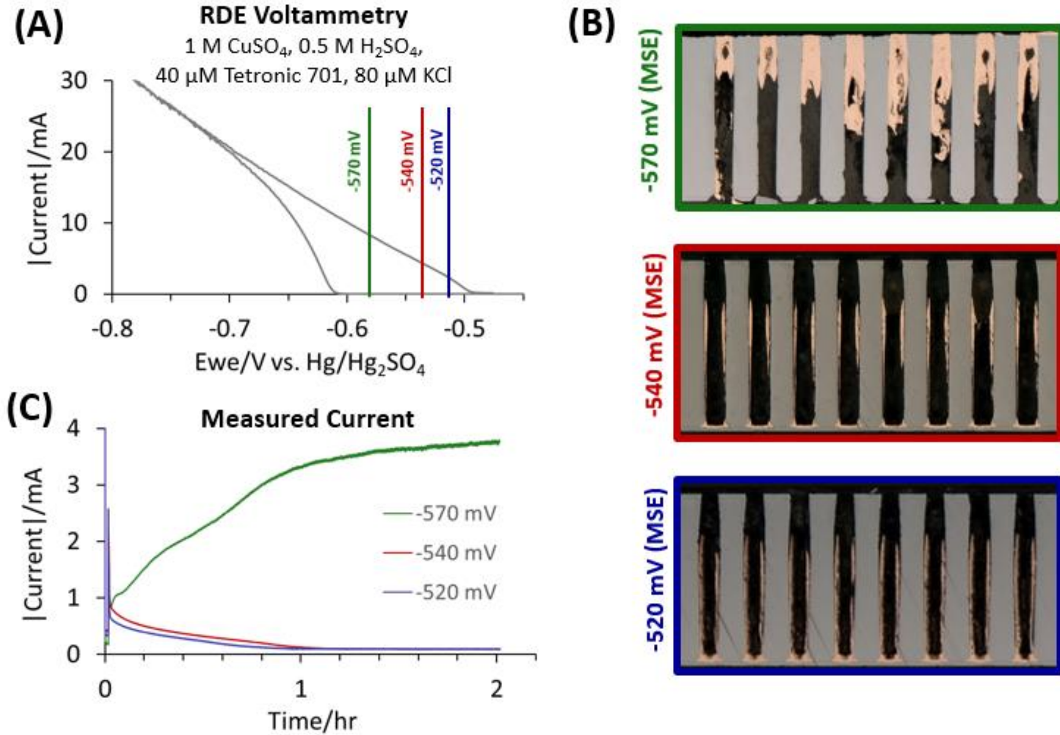


Figure 23. (A) RDE voltammetry in an electrolyte containing 1 M $CuSO_4$, 0.5 M H_2SO_4, 80 μM KCl, and 40 μM Tetronic 701. (B) Mechanically cross-sectioned samples produced by potentiostatic Cu ECD at -570 mV, -540 mV, and -520 mV (MSE), all rotated at 400 rpm. (C) Measured current during deposition for each sample.[1]

In Figure 23 (C), the current transient for the sample plated at -570 mV (MSE) shows substantial measured current, which correlates to that voltage providing enough overpotential to overcome suppressor behavior high up in the vias and deposit Cu. The two samples plated at -540 mV and -520 mV (MSE) show less current flow due to system passivation high up in the vias and more limited Cu deposition in the features, which is evidenced by the cross-sections in Figure 23 (B). After about 1 hour of plating at -520 mV and -540 mV, the decrease in current observed in Figure 23 is likely due to

passivation by suppressor, based on the diffusion coefficient for Tetronic 701 in literature.[24] In this low chloride system, localized active deposition grows from the via walls inward and eventually becomes suppressed, so voltage ramping was required to move active deposition through the features. Based on the results in Figure 23, the voltage stepping recipe needed to start more positive than -520 mV (MSE) to confine deposition to the bottom of the vias, and the time constant for passivation of ~1 hour, observed in Figure 23 (C), provided an approximate time interval for sustaining each voltage step.[1]

Figure 24 (A) shows the applied voltage for each of the voltage ramping recipes developed in this work.[1] Experiments started at -500 mV and ended at -560 mV (MSE) with voltage increments of 5 mV or 10 mV and time durations at each voltage step ranging from 45 minutes to 2 hours. Figure 24 (B) displays the polished cross-sectional images and X-ray CT scan snapshots for each sample. The CT scan images reveal information about the volume of the voids that is not directly apparent in the 2D mechanical cross-sections. For example, when comparing the cross-sectional images for the 1-hour interval, 10 mV sample and 1.5-hour interval, 10 mV sample cross-sections, the 1-hour sample appears to have smaller voids. However, the corresponding CT scan reveals larger voids that are hidden by the 2D cross-section. The CT image for the 2-hour, 10 mV sample also elucidates small seam voids in the electrodeposit which are not observed in the cross-sectional image. The results in Figure 24 also show that longer time intervals at each voltage minimize void formation. The 45-minute interval sample shows substantial voids, since the voltage advanced too rapidly prior to sufficient Cu deposition at each height in the vias. Much smaller voids are observed for

the 2-hour interval sample, and a similar result occurs when decreasing the voltage increment from 10 mV to 5 mV and simultaneously decreasing the interval from 2 hours to 1 hour. The CT scan images show that void volume and location is similar for the 1 hour interval, 5 mV step sample and the 2 hour interval, 10 mV step sample.[1]

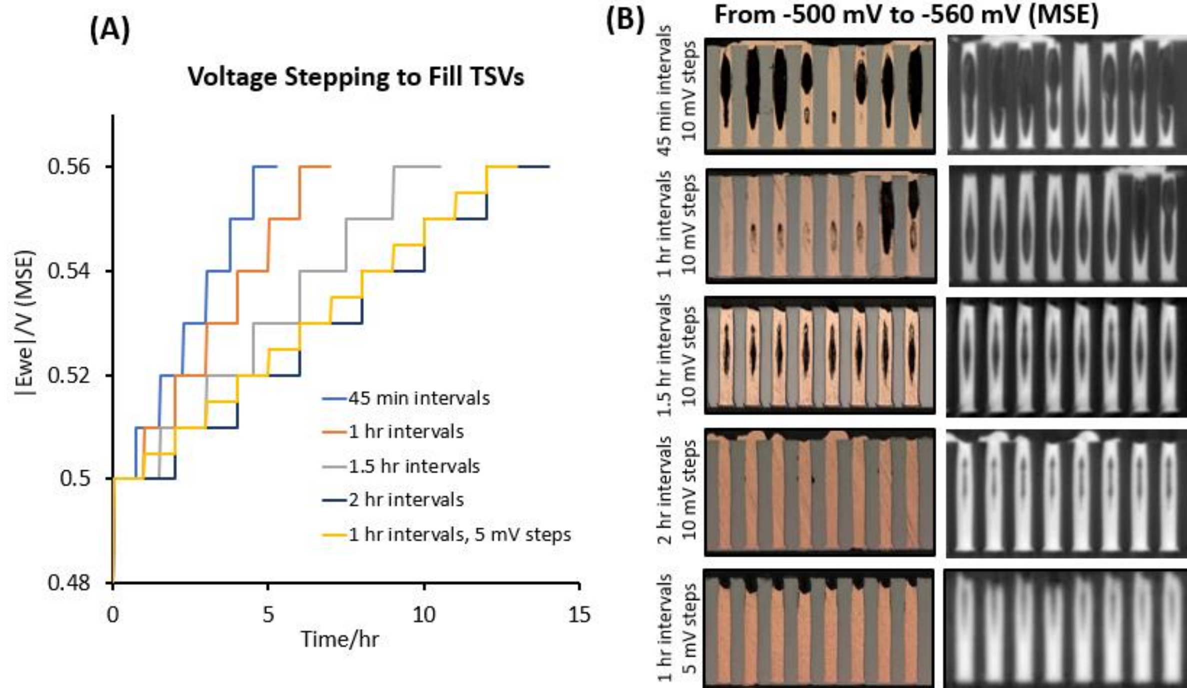


Figure 24. Voltage stepping experiments performed in the low chloride electrolyte. (A) Voltage stepping recipes from -500 mV to -560 mV (MSE) in increments of 5 mV or 10 mV are indicated. Time intervals ranged from 45 minutes to 2 hours for each sample. (B) Cross-sectioned samples and X-ray CT scans correspond to each recipe.[1]

Although the sample obtained from 2-hour intervals and 10 mV steps exhibits relatively small voids, void-free fill is required for long-term TSV interconnect reliability, since voids can contain trapped electrolyte that slowly degrades the electrodeposit. To evaluate void formation during the 2-hour interval, 10 mV step recipe, samples were obtained at different points during the filling process and

characterized. Figure 25 (A) shows the voltage stepping scheme from -500 mV to -560 mV (MSE) for the 2-hour interval, 10 mV step recipe and indicates points at which deposition was terminated for sample analysis.[1] Samples were obtained after steps 2, 5, 6, and 7, which correspond to -510 mV, -540 mV, -550 mV, and -560 mV (MSE), respectively, and the characterized samples are shown in Figure 25 (B). The first cross-section indicates that bottom-up filling has initiated by the end of step 2. After step 5, a distinctive v-shaped growth front is observed, which is characteristic of the low chloride plating chemistry.[5] At this point in the recipe, the remaining aspect ratio of the feature has changed dramatically, and significant sidewall plating occurs during step 6, which eventually leads to seam void formation. During step 7, Cu deposition reaches the top of the via, and the seam void closes off.[1]

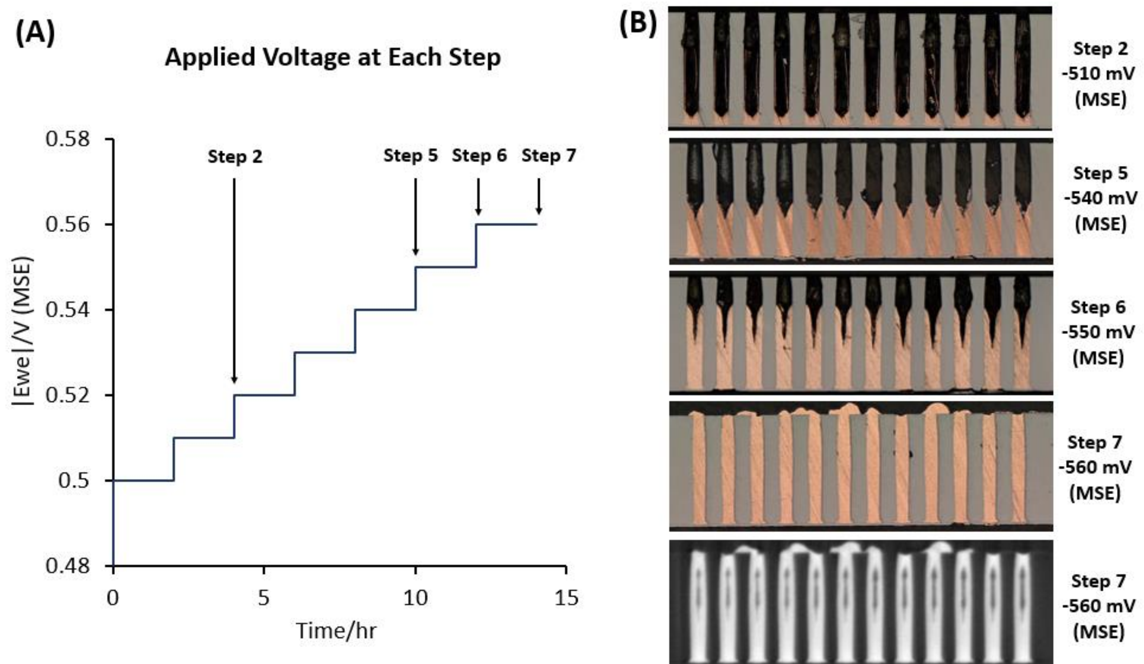


Figure 25. Void formation analysis was performed on the voltage stepping recipe that had 2-hour time intervals and 10 mV increments. (A) The recipe for this sample is shown, and four selected stopping points for sample analysis are indicated. (B) Cross-sectioned samples from selected stopping points show void formation as the Cu electrodeposit evolves over time.[1]

Due to the increased Cu deposition rate between steps 5 and 6, it was determined that step 5 should be prolonged. Increasing the duration of step 5 would allow for continued feature filling but would also mitigate the rapid sidewall plating that led to void formation during step 6. Figure 26 (A) shows a voltage stepping schematic depicting the experimental changes that were made in extending step 5, which is the -540 mV step, from 2 hours to 5 hours.[1] The mechanical cross-section for the sample with an extended step 5 appears to be void-free, and the CT scan solidified this conclusion and indicates that the modified recipe produces void-free filling at the die level for the 10:1 AR TSV samples.[1]

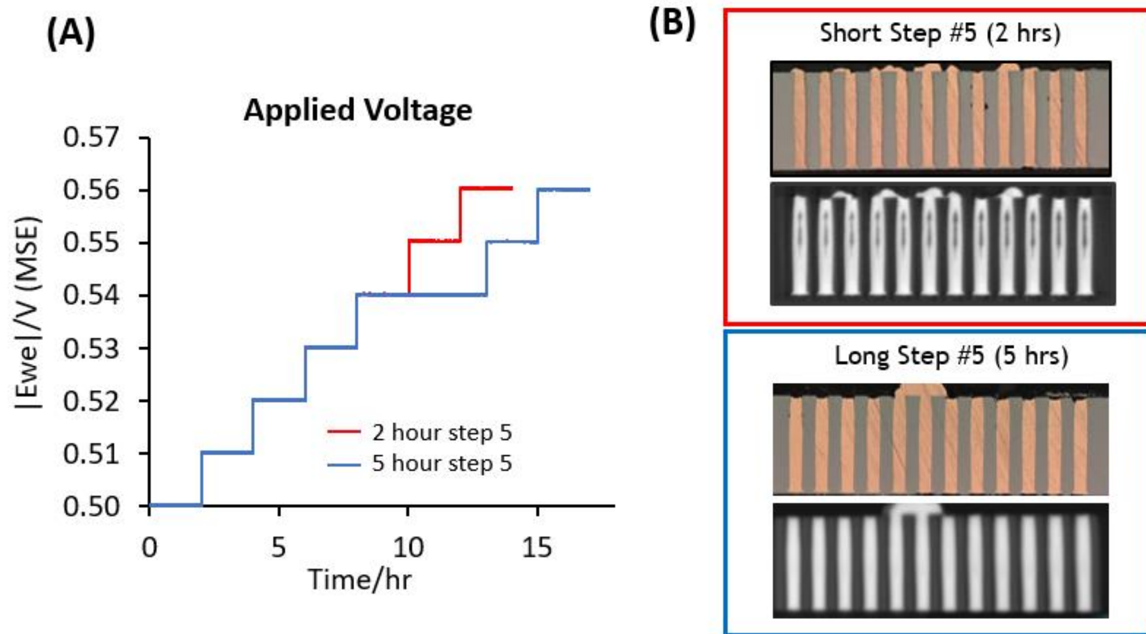


Figure 26. Extending step 5 (the -540 mV step) from 2 hours to 5 hours leads to void-free filling. (A) Voltage stepping schematic of both samples. (B) Mechanical cross-sections and CT scans for 2-hour and 5-hour long step 5 samples.[1]

The low chloride chemistry was instrumental in producing a Cu ECD method for these high aspect ratio, full wafer thickness TSVs, and stepping the voltage during

deposition moved the Cu growth front through the features. During the voltage-controlled deposition process, current was measured, and a characteristic current feature was observed.[1] In Chapter 4, this current feature will be presented as a deposition endpoint detection method for Cu filling in these TSV features.

Chapter 4: Endpoint Detection for Cu TSV Filling

4.1 A Cu ECD Endpoint Detection Method through Monitoring Measured Current or Voltage

The endpoint detection method presented here is based upon in situ monitoring of Cu deposition through characteristics in the measured current data and is analogous to etch endpoint detection by spectroscopic analysis of gaseous byproducts in a deep reactive ion etching (DRIE) tool.[2] Cu-filled TSVs are a critical interconnect technology enabling 3D and heterogeneous integration of microelectronics devices, and endpoint detection during Cu electrodeposition allows for process control and tunability of the Cu fill profile. Terminating deposition when Cu reaches the top of the vias, based on the electrical endpoint signal, reduces the amount of Cu overburden on the field surface and eliminates the need for subsequent fabrication steps such as chemical-mechanical polishing (CMP) to remove excess Cu.[2]

4.2 Experimental Data: Current Transients Identify Cu ECD Endpoint

Current was measured during voltage-controlled deposition experiments, and these data exhibit a distinctive “dip” in current near the end of the experiments. The current transients are pictured in Figure 26 with their corresponding samples.[1] During constant-voltage plating, the level of Cu^{2+} replenishment high up in the TSV features causes an increased deposition rate compared to farther down in the features, where ion depletion occurs. As the Cu electrodeposit grows in the TSVs during constant-voltage plating, current increases because of increased metal ion replenishment and

eventually reaches a local maximum. When deposition reaches the top of the vias, further Cu ion reduction is hindered by the high local suppressor concentration, which leads to a decrease in current, and a local minimum in current is observed. When suppressor is eventually desorbed from the field surface area, Cu deposition rate increases again and current rises, and this deposition creates Cu overburden. Sample (A) exhibits Cu deposition that did not reach the top of the features, since plating was terminated prior to the current reaching a local minimum. Samples (B) and (C) exhibit Cu overburden, and the corresponding current data show that deposition for these samples continued on the field surface area after the current minima were reached. Tracking the current data during deposition can be used for electrical endpoint detection to ensure that deposition terminates when the vias are completely filled and can mitigate Cu overburden formation.[1]

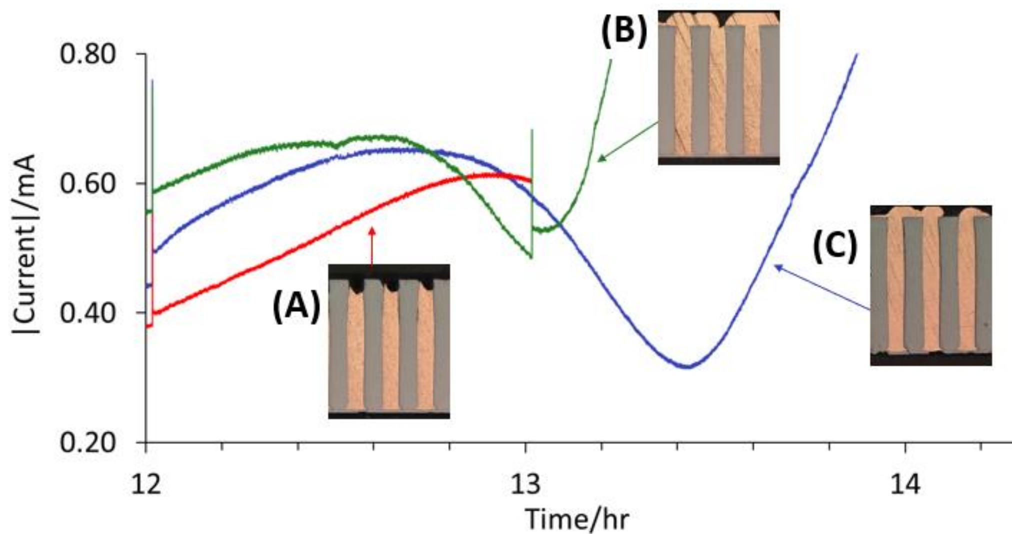


Figure 27. Current transients and corresponding Cu plated samples. The current minima indicate that Cu fill completion in the TSV features and can be used as an endpoint detection method. (A) A cross-sectioned sample that is slightly underfilled due to early deposition termination. (B) and (B) ECD continued after the current minima were reached, and the corresponding samples exhibit Cu overburden.[1]

4.3 A Future Path for Automated ECD Termination when Vias are Filled

The repeatable characteristics in the measured current data at the end of deposition will make it possible to automatically terminate deposition when the current transient is detected. As a summary of the experimental data, during the voltage-controlled deposition process, current is measured over time, and a characteristic transient in the measured current data indicates that Cu deposition has reached the top of the vias. The features of this current transient include the following: 1) a local maximum in the current data caused by a decrease in system impedance as Cu fills the vias, 2) a decrease in current followed by a local minimum, which results from Cu reduction being inhibited by suppressor molecules near the field surface, and 3) increased current, as suppressor behavior is overcome and Cu reduction occurs on the sample's top surface. Recognizing the characteristic transient in measured current data allows for process control, and termination of the deposition experiment at the current minimum leads to perfectly filled vias with minimal Cu overburden.[1] Future work will implement a python code to recognize the current minimum and terminate the voltage-controlled deposition by automatically turning off the potentiostat.

4.4 Potential Impact for Future Wafer Level Plating

Monitoring either current (during voltage-controlled deposition) or voltage (during current-controlled deposition) can be used to inform when the ECD process is complete, since both methods will provide a fluctuation in the measured data when Cu deposition reaches the top of the features. For wafer level plating tools that do not have reference electrodes and rely on current-controlled plating, there is a space to

incorporate a Cu endpoint detection method in which the voltage is monitored for a voltage fluctuation (analogous to the measured current dip during voltage-controlled plating).[2] This signal is observed as a spike in voltage at the end of the deposition experiment and has been observed when plating with a sustained current in this work. During current-controlled plating, when the Cu deposit reaches the top of the TSVs, further Cu deposition is inhibited by the increased presence of suppressor molecules. At this point, increased overpotential is required to maintain the same current and Cu deposition rate. When the vias are filled and suppressor is desorbed from the top surface of the sample, Cu plating continues, and the voltage required to maintain constant current decreases.

Chapter 5: Transitioning from Die Level to Wafer Level Plating

5.1 Die Level Experiments to Inform Full Wafer Deposition Parameters

Bottom-up, void-free filling was achieved for die level 10:1 AR TSVs samples in a suppressor-additive electrolyte using voltage-controlled plating with a reference electrode. Scaling these processes from die level plating experiments, in a small electrochemical cell, to a production scale full wafer plating tool requires development of a current-controlled plating method, because production plating systems do not have reference electrodes. The required applied current for a wafer level process must be determined experimentally, because a greater applied current magnitude will be required for a large full wafer sample compared to a small 1 cm^2 die. Furthermore, the developed plating process cannot be highly sensitive to sample rotation rate, because vias at different radial positions across a wafer move at different speeds. In this work, a current-controlled deposition process for bottom-up, void-free filling is developed, and rotation rate and die size scaling studies are performed to transition the plating process from 1 cm^2 sample sizes to a full wafer.[2]

5.2 Deriving a Current-controlled Die Level Deposition Method

Voltage-controlled ECD parameters were first established with die level plating experiments, in which vias were successfully filled with a potential stepping recipe in which the voltage started at -500 mV (MSE) and was gradually incremented to -560 mV (MSE) using 10 mV steps for various time durations. During these voltage-controlled Cu deposition experiments, the resulting current was measured. Subsequent plating

experiments were executed by applying current, as opposed to voltage, to mimic the measured current values, and this current-controlled ECD process also achieved void-free filling. Figure 28 illustrates the development process from voltage-controlled to current-controlled ECD and corresponding mechanical cross-sections. As shown in the sample cross-sections, these electroplating processes result in suppressed deposition on the field area, even though the field is part of the total conducting surface.[2]

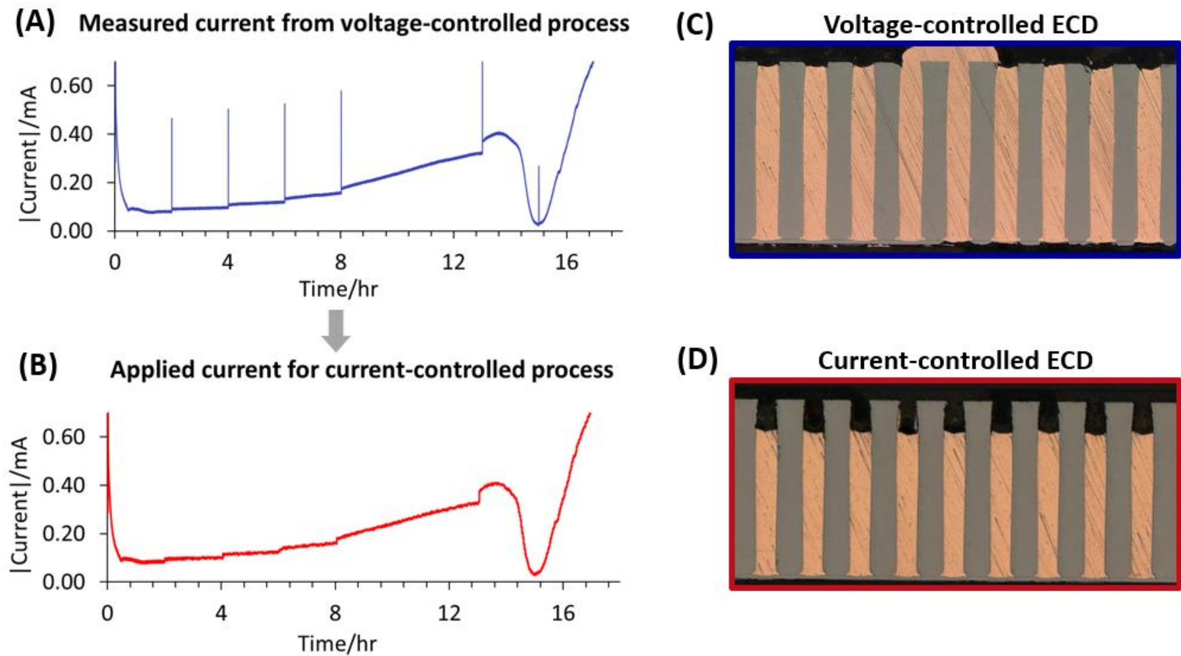


Figure 28. (A) Measured current from a voltage-controlled experiment. (B) The measured current was used as the applied current in a subsequent experiment. Both the (C) voltage-controlled and (D) current-controlled samples produced void-free plating results, but this particular current-controlled sample deposited at a slightly slower rate.[2]

During current-controlled deposition, resulting voltage data were collected. Figure 29 shows the measured voltage from the current-controlled deposition compared to the applied voltage from voltage-controlled ECD. The measured voltage

data tracks well with the applied voltage for steps 1-4. Around 15 hours, there is a drastic decrease in the measured voltage. Based on Figure 28, current-controlled deposition occurred at a slightly slower rate than the voltage-controlled deposition, and the forced current drop during current-controlled deposition occurred prematurely to Cu deposition reaching the top of the vias. The decrease in the measured voltage data at 15 hours (Figure 29) corresponds to the forced current drop observed around 15 hours (Figure 28 (B)), in accordance with Ohm's law. Instead of decreasing current during the current-controlled deposition, sustaining current around 0.40 mA would likely complete deposition in the vias, and the measured voltage could be monitored for a characteristic voltage transient, much like the current minima shown in Figure 27 in Section 4.2. The transient in the measured voltage data can function as an endpoint detection method during current-controlled deposition.[2]

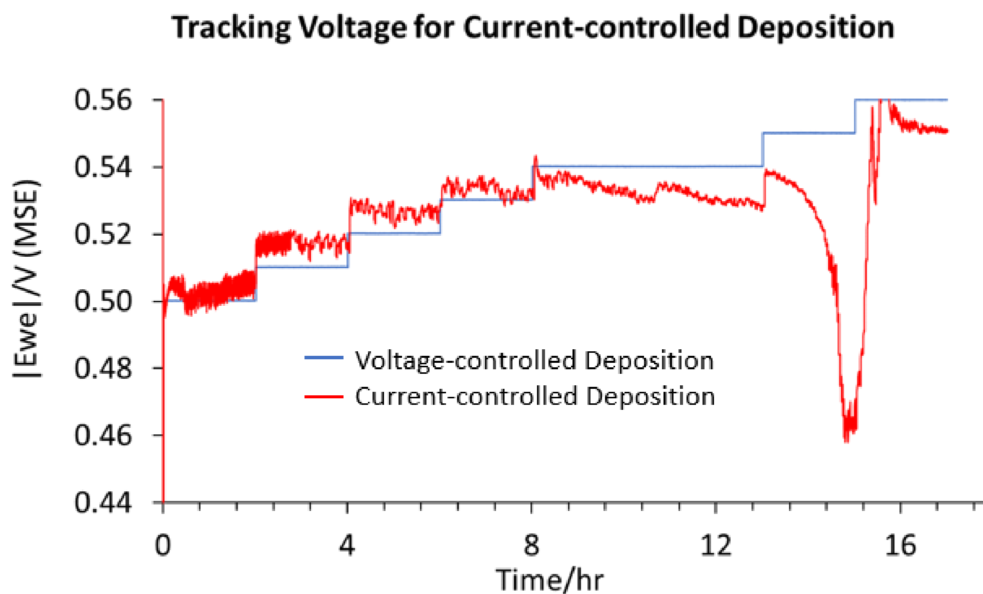


Figure 29. Comparison between applied voltage in voltage-controlled deposition and resulting voltage during current-controlled ECD. The resulting voltage tracks with the applied voltage for steps 1-4. The voltage dip around 15 hours corresponds to the forced current drop in Figure 28 (B).[2]

5.3 Impact of Rotation Rate and Solution Replenishment on Filling Results

5.3.1 Fluid Flow over a Flat Plate Approximation for TSV Samples

The fluid flow along the TSV sample surface can be compared to the fluid flow over a flat plate, which is depicted in Figure 30.[17] The velocity at the leading edge of the TSV sample, v_e, is based on the distance between the TSVs and axis of rotation, r, and angular velocity, ω (Equation 5.1). Blasius's solution for laminar boundary layer thickness on a flat plate, δ, is given in Equation 5.2, where ν is the kinematic viscosity of the electrolyte and x is the distance from the leading edge of the sample.[25] From these two equations, it can be shown that $\delta \propto \omega^{-1/2}$ and that the boundary layer thins with increasing rotation rate (as is the case for the RDE hydrodynamic boundary layer from Section 1.4.2), which ultimately impacts mass transport into the vias.

$$v_e = 2\pi r\omega \tag{5.1}$$

$$\delta = 5\sqrt{\frac{\nu x}{v_e}} \tag{5.2}$$

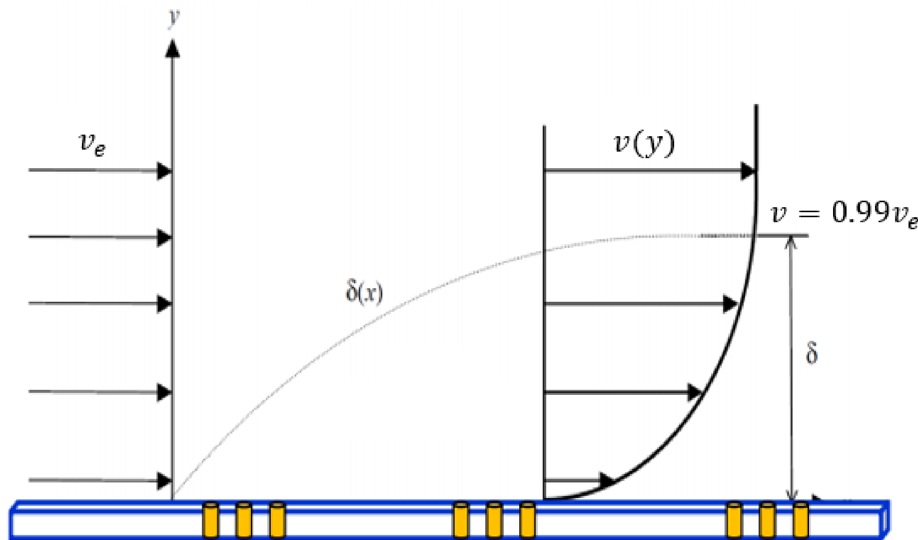


Figure 30. Fluid flow over a TSV sample modeled as a flat plate.[17] Reproduced with permission.

5.3.2 Impact of Rotation Rate and Electrolyte Replenishment on Cu Fill Profile

With a wafer rotating about its center, solution replenishment within each TSV is dependent on the via's radial position. To understand the dependence on solution replenishment and applied bias in a given electrolyte, a series of investigations were performed on samples rotated at different rates. At a given applied voltage, sufficient Cu^{2+} ion transport must occur to balance Cu^{2+} depletion in the vias. Rotation rate experiments were conducted on die level TSV samples using the voltage-controlled profile shown in Figure 31, and this profile was implemented for samples rotating at 100, 200, and 400 rpm. The measured current data indicate higher current flow for the 400-rpm sample compared to the other samples, because the faster rotation rate facilitates more Cu^{2+} ion replenishment into the vias. The increased metal ion replenishment for the 400 rpm sample results in a higher deposition rate compared to the more slowly rotating samples, which have less available Cu^{2+} ions for reduction due to ion depletion. Cu deposition in the 400-rpm sample reached the vias before the 100 and 200 rpm samples, as indicated by the current transient around 15 hours; the current transients for the other two samples indicate that deposition completed around 16.5 to 17 hours. These results indicate that the samples with lower rotation rates have less Cu^{2+} replenishment and slower deposition times.[2]

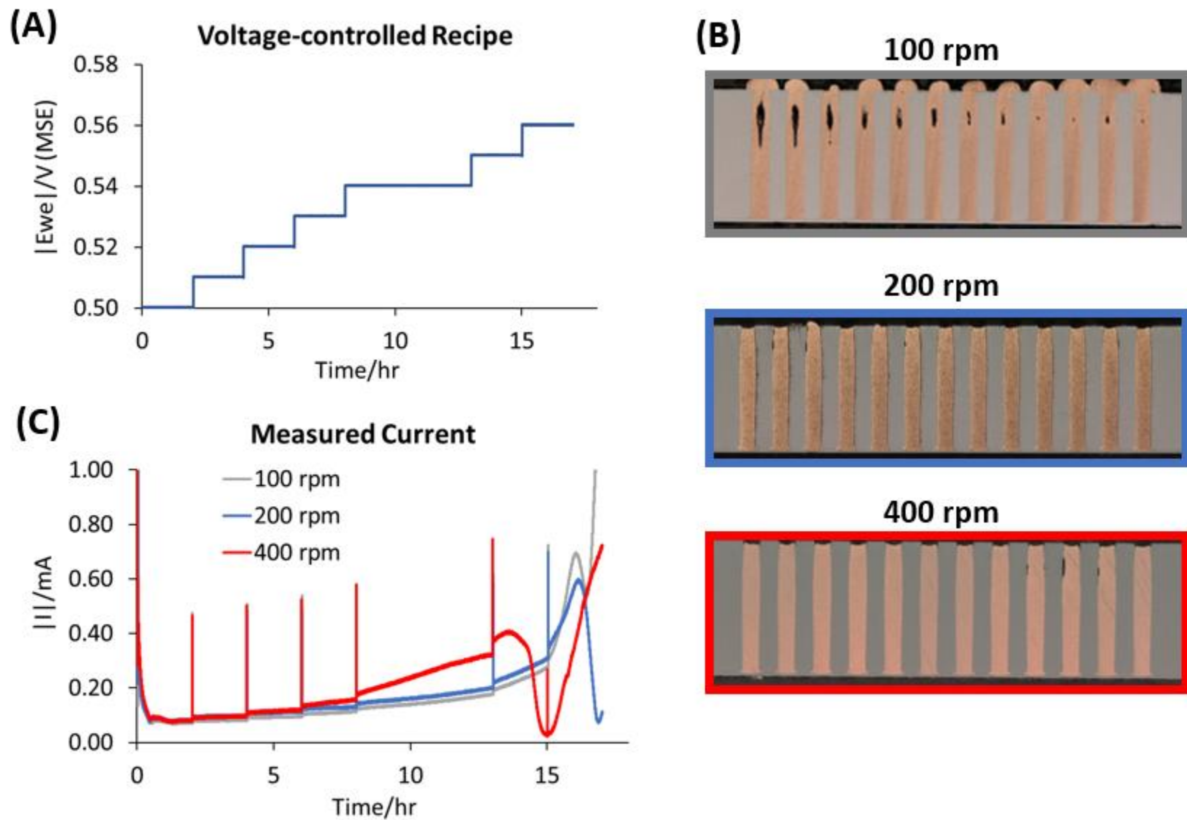


Figure 31. (A) Voltage-controlled recipe for rotation rate experiments. (B) Cross-sections for 100, 200, and 400 rpm samples. (C) Measured current for each sample during voltage-controlled deposition.[2]

For each sample, the row of vias furthest from the axis of rotation were cross-sectioned, and this row is approximately 1.5 cm from the axis of rotation. Using Equation 5.3, the TSV linear velocity, v_{TSV}, can be calculated from angular velocity, ω, and distance from the axis of rotation, r, generating linear velocity values of about 15.7 cm/s, 31.4 cm/s, and 62.8 cm/s for TSVs rotating at 100 rpm, 200 rpm and 400 rpm, respectively (Table 2). Figure 31 (B) shows that the 400 rpm and 200 rpm sample cross-sections appear to have uniform, void-free Cu deposition. Some voiding is present at the top of the 100-rpm sample, which could be removed by performing void formation analysis and altering time duration of each sustained potential in the recipe.

Additionally, during wafer level plating, current could be allocated accordingly to ensure these voids do not form. Alternatively, it could be ensured that the majority of the TSVs on the rotating wafer are rotating faster than ~15.7 cm/s to allow for adequate solution replenishment. This study provides an operational window for linear velocities that produce samples with void-free Cu deposition, and this operational window can be used when determining rotation rate for wafer level plating. Further studies will be performed to observe the relationship between solution replenishment and Cu fill profile at faster rotation rates (> 400 rpm).[2]

$$v_{TSV} = 2\pi r\omega \tag{5.3}$$

Table 2. TSV linear velocities for die level rotation rate experiments.

Sample	TSV Velocity (cm s^{-1})
100 rpm	15.7
200 rpm	31.4
400 rpm	62.8

5.3 Current Scaling with Increasing Die Size

Scaling experiments were performed both to evaluate the efficacy of the voltage-controlled recipe with variable sample size and to understand the relationship between measured current density, total conductive surface area, and active via area. Figure 32 depicts 1, 2, and 3 die samples which were run using the voltage-controlled recipe in Figure 31 (A). Samples from each row crossed-sectioned appear to be completely void-free, indicating the feasibility of applying the voltage-controlled recipe to samples of varying size. The measured current data show that current increases with sample

plating area, as the highest current is observed for the 3 die sample, and the lowest current is measured for the 1 die sample. At a given voltage, larger current will be observed for samples with larger available conductive plating area. The current minimum around 15 hours for the 1, 2, and 3 die samples indicates that deposition reached the top of the vias around the same time for each sample. Further scaling studies will be conducted in the future with more sample areas to evaluate if current scales with total conductive surface area or active via cross-sectional area. These results will determine a predictable relationship between sample size and resulting current, and these data will be used to determine applied current for future wafer level plating applications.[2]

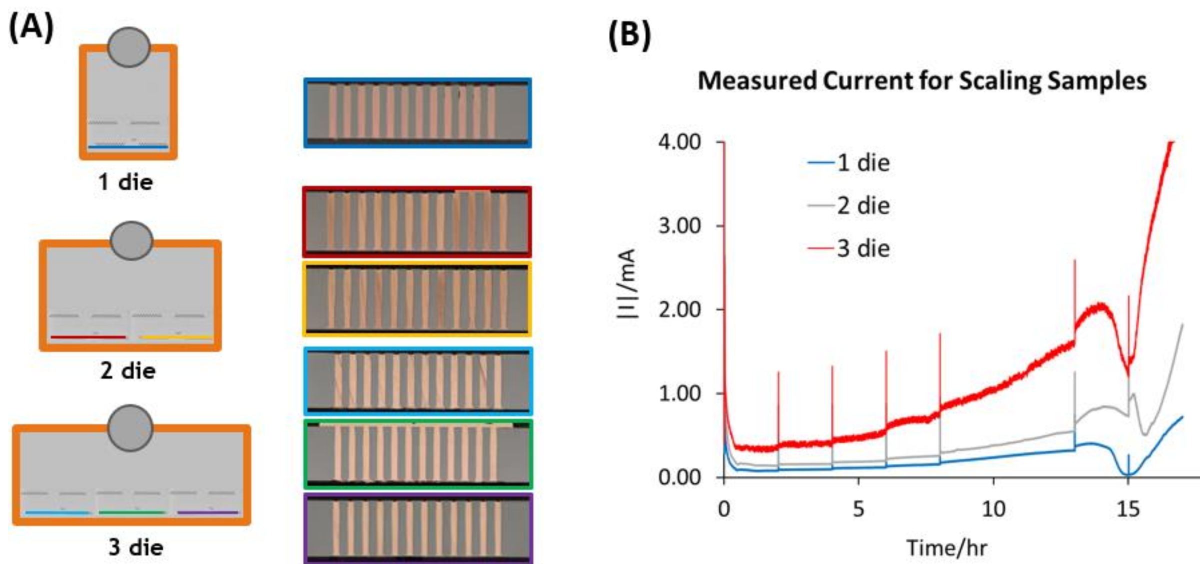


Figure 32. (A) Scaling experiment sample representations for 1, 2, and 3 die samples and corresponding cross-sections. (B) Measured current scales with sample size for voltage-controlled deposition.[2]

Chapter 6: Summary and Future Work

6.1 Summary

In this work, void-free Cu ECD in high aspect ratio, full wafer thickness TSVs was achieved in a suppressor-based $CuSO_4$ electrolyte through both voltage-controlled and current-controlled methods. Parameters for successful filling of 5:1 AR vias did not directly translate to produce void-free filling results in 10:1 AR vias, illustrating the delicate relationship among TSV geometry, electrolyte composition, and applied electrical bias. After scanning various combinations of plating electrolyte, applied bias, and fluid flow options, a low chloride, H_2SO_4-$CuSO_4$ electrolyte with Tetronic 701 suppressor additive was implemented. RDE voltammetry identified a potential window for experimentation, and voltage stepping was implemented to move active deposition through the TSVs. Ideal time durations for each voltage step were identified through sample characterization using mechanically polished cross-sections and X-ray CT scans. Using the measured current data during voltage-controlled deposition, a characteristic current dip was identified that will be utilized as an endpoint detection method for Cu plating in these features.[1]

Studies for wafer level plating development were performed to evaluate current-controlled deposition, since full wafer ECD tools are not equipped with reference electrodes. Sample rotation rate experiments were conducted to evaluate Cu fill profile and solution replenishment at a given rotation rate. These studies generated an operational window for TSV linear velocities that produce uniform, void-free filling,

which will translate to future wafer level plating development. Scaling studies demonstrated the voltage-controlled recipe’s ability to produce void-free filling results for multi-die samples and indicated that current roughly scales proportionally to active plating area.[2]

6.2 Future Work

Additional scaling studies will be conducted to further evaluate the relationship of measured current with active plating area and will specifically evaluate whether current scales with the via cross-sectional area or total conductive surface area. Rotation rate and solution replenishment analysis will also be performed at the die level for higher rotation rates (> 400 rpm) to determine the full fluid replenishment operational window for wafer level plating. The Cu endpoint detection method, discussed in Chapter 4, will be implemented into current experimental processes to terminate Cu deposition at the top of the vias and eliminate subsequent processing steps for removing Cu overburden. Ultimately, future work will translate these results into a robust wafer level plating process for MEMS and other microelectronics applications.

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy’s National Nuclear Security Administration under contract DE-NA0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government. SAND2020-12041 O

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APPENDIX A

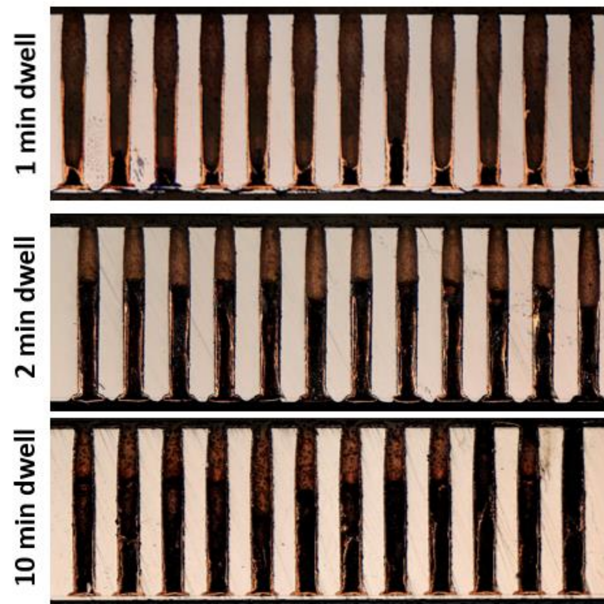

Figure 33. Dwell time experiments were performed at -620 mV (MSE) in the 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 μM Tetronic 701.

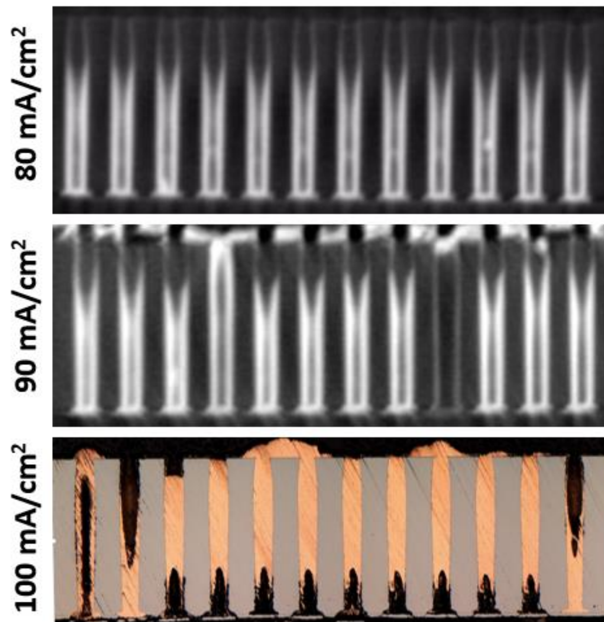

Figure 34. Galvanostatic experiments 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 50 μM Tetronic 701. The defined area (in cm^2) is the via circular cross-section.

APPENDIX B

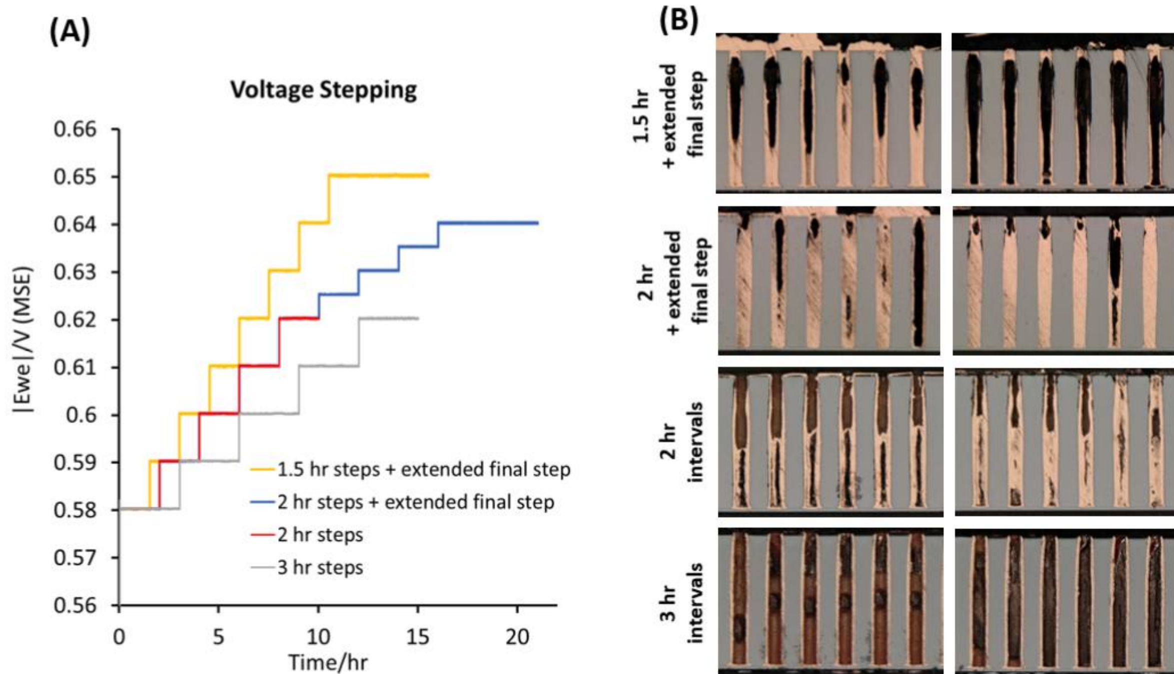

Figure 35. Voltage stepping experiments in the 1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, and 25 µM Tetronic 701 electrolyte. The voltage was stepped in 10 mV increments, and each step was held for 1.5-hour, 2-hour, or 3-hour intervals, with the duration of the final step extended for some of the experiments.

APPENDIX C

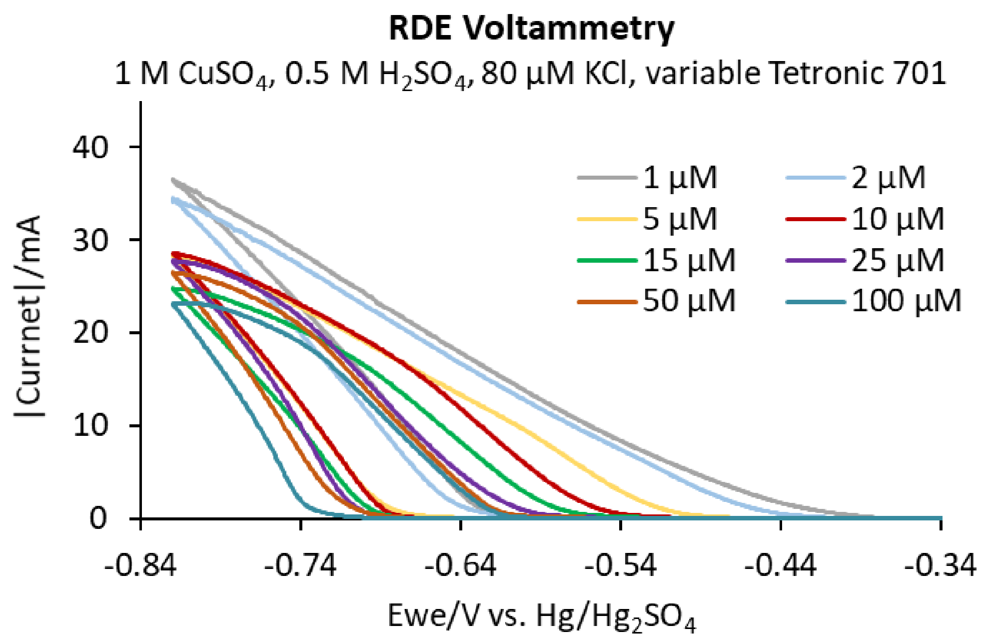

Figure 36. RDE voltammetry on electrolytes containing 1 M $CuSO_4$, 0.5 M H_2SO_4, 80 µM KCl, and variable Tetronic 701.