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Conditional Effects in the Transistor Distributed Amplifier

Herbert D. Arlowe

CONDITIONAL EFFECTS IN THE TRANSISTOR DISTRIBUTED AMPLIFIER - ARLOWE

NAME AND ADDRESS	DATE

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By

Herbert D. Arlowe

A Thesis
Submitted in Partial Fulfillment of the
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This thesis, directed and approved by the candidate's committee, has been accepted by the Graduate Committee of the University of New Mexico in partial fulfillment of the requirements for the degree of

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ABSTRACT

This thesis describes some of the difficulties encountered in the application of transistors to distributed amplifier circuits. When an attempt was made to construct a useful distributed amplifier, it was noted that the input signal was severely attenuated along the input line. The primary concern of the thesis is this severe loading effect sometimes observed on the distributed amplifier circuit by the input parameters of the transistor.

The thesis first reviews the principles and objectives of the distributed amplifier. The effects of various basic types of amplifying devices are analyzed in order to demonstrate the application limits of the distributed amplifier.

With these limits in mind, the input characteristics of a specific transistor are measured and the generalized real and imaginary impedance components are determined as functions of frequency for a commonly accepted transistor equivalent circuit. Since the loading of the distributed amplifier circuits is directly dependent on the Q of the components involved, this parameter is treated with special concern.

The allowable limit for amplifying device loading is next derived in a simplified analysis of the gain in a distributed amplifier having non-zero losses.

A theoretical analysis of one method of applying an idealized resistive transistor to a distributed amplifier shows that, even if impedance matching is observed, the principle of distribution does not contribute an advantage.

Finally, an analysis is made of one type of compensating network which can raise the input Q of a transistor amplifier to the point where it may be used to advantage in a distributed amplifier.

As part of the appendix, special techniques in the measurement of transistor input parameters at low signal levels are discussed. Data are also given on measurements taken of the input parameters of the 2N384 transistor, which show their variation due to external circuit parameters and manufacturers tolerances.

ACKNOWLEDGEMENT

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Herbert D. Arlowe

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CHAPTER I -- INTRODUCTION

A primary goal of the electronics industry is to increase the performance of electronic equipment. One particular area of investigation has been to make signal amplifiers as independent of frequency as possible. The amount of information that can be packed into a signal has become closely linked with frequency bandwidth. There are many effects in present amplifying devices which tend to restrict the maximum frequency at which they are useful. These effects can be divided into two rough catagories.

The first group consists of circuit parameters, such as interelectrode and stray capacitances, and lead wire inductances. These parameters are not really necessary for the theoretical operation of the amplifying device, but occur due to its physical nature.

The second group of effects results directly from the nature of the amplifying mechanism. In vacuum tubes, this effect includes transit time and grid loading; in transistors, it is charge storage and drift velocities. In both devices, this second group of effects takes hold at somewhat higher frequencies than in the first group. For pentode tube amplifiers, the capacitance from plate to ground (C_p) and from grid to ground (C_g) cause a reactive shunting of the signal to ground at radio frequencies. This effect has long been overcome at specific frequencies by utilizing the capacitance as a part of a tuned circuit. However, if one is to keep the circuit response independent of frequence, it is necessary to have the amplifier "see" a load which is independent of frequency. If a resistive load is used, a maximum gain-bandwidth product can be specified, sometimes called Wheeler's "figure of merit"

for a tube:

$$Gf_2 = \frac{g_m}{\pi\sqrt{C_p C_g}} \tag{1}$$

Where:

G is the gain

f_2 is the upper frequency limit

g_m is the mutual conductance of the tube

As shown by Equation 1, the size of the shunt capacitances limits the gain bandwidth product.

The bandwidth f_2 can be increased only at the expense of gain. When the gain drops below unity, these amplifiers are useless in themselves and cannot be cascaded due to the multiplying effect therein. If these tubes are placed in parallel, in order to make their g_m's add, one finds that the C_g and the C_p's also add, so that the overall gain bandwidth product remains the same.

Here is where the distributed amplifier technique is helpful. Its use allows the paralleling of the tubes in a manner such as to cause the g_m's to be additive while holding the shunt capacitance to that of a single tube. As shown in Figure 1, the grid and plate capacitances form the shunt elements of low pass filter networks.

If there were no losses in these filter networks, the new expression for gain bandwidth would be:

$$Gf_2 = \left(\frac{1}{2}\right)\frac{ng_m}{\pi\sqrt{C_p C_g}} \tag{2}$$

(Note: 1/2 of low frequency gain is lost at the reverse termination of the output line Z_{or})

Where:

n is the number filter sections and tubes used.

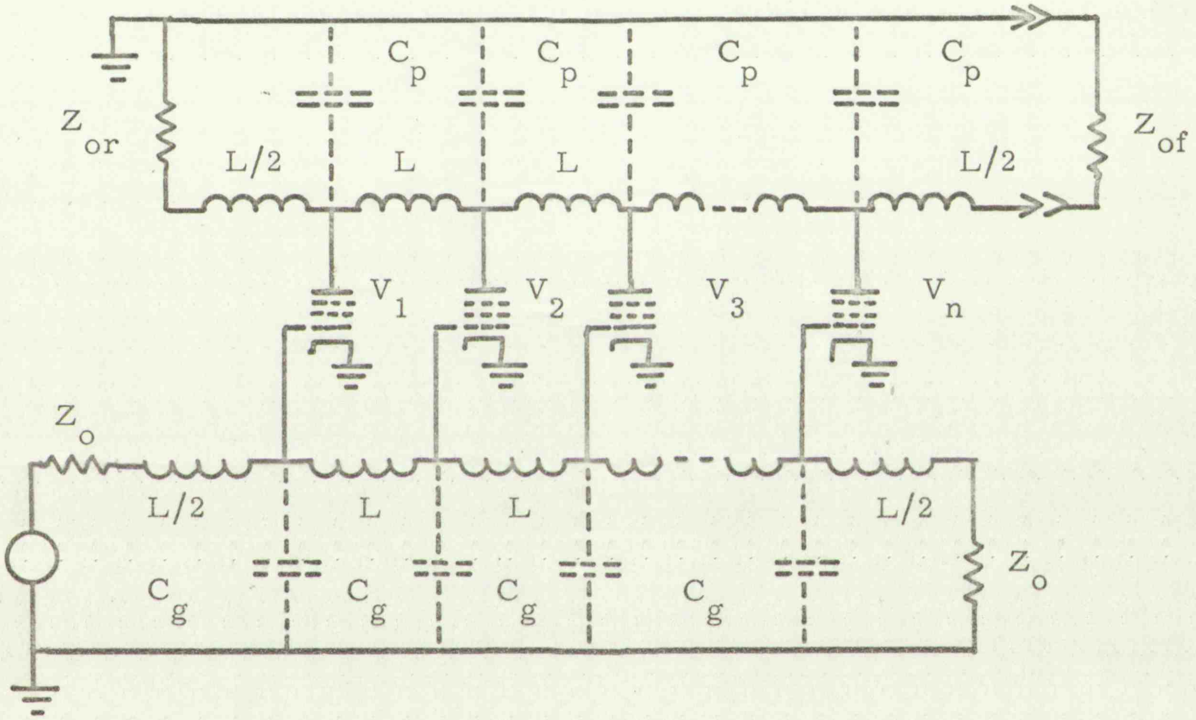

Figure 1

It would seem then that almost any gain-bandwidth could be achieved by using a sufficiently large number of tubes. However, there are losses associated with these filter networks, and, at higher frequencies, with the tubes also. This results in a new but larger gain-bandwidth product [4] concept:

$$f_2 = \frac{1}{2\pi}\sqrt{\frac{G_m}{AG_o}} \qquad (3)$$

Where:

G_o is the grid conductance

A is the gain of the distributed amplifier

G_m is the mutual conductance of the tube used

As shown in Figure 1, the distributed amplifier consists of two filter networks, usually having constant K sections, with either m derived end sections or else regular half sections for terminations. The tubes are placed at the filter junctions so that the grid and plate capacitances are in fact the shunt reactances for the filters and so that the voltages which appear at each grid will be amplified and inserted into the output line. The voltage "wave fronts" introduced into the output line will travel in both the forward and reverse directions. This wave front will experience a phase shift as it travels along the filter lines. The signal contribution from each tube will arrive at the forward output termination "in phase" and, in general, will arrive "out of phase" at the reverse termination. The energy arriving at the reverse termination is not normally utilized and accounts for the loss in gain of 1/2 that appears in the gain Equation 2. This power must be absorbed as much as possible, however, to reduce reflections.

In order that the input signal experience the same phase shift regardless of which tube amplifies it, the phase shift per input line section must be the same as for the output line sections. This is accomplished by making the lines identical, or at least by making the product LC the same for both. This procedure is indicated by the following equations:

$$R_o = \sqrt{L/C} \qquad (4)$$

$$Z_o = \sqrt{\frac{L/C}{\left[1 - \left(\frac{f}{f_c}\right)^2\right]}} \tag{5}$$

$$\beta = 2 \text{ arc sin } (f/f_c) \tag{6}$$

$$f_c = 1/\pi\sqrt{LC} = \frac{1}{\pi\sqrt{LC}} \tag{7}$$

The nominal gain of a distributed amplifier, considering that the lines are terminated in their characteristic impedance Z_o, would be:

$$A = ng_m \frac{Z_o}{2} \tag{8}$$

In a distributed amplifier whose input and output lines were not equal in terms of an iterative amplifier, the theoretical gain would be modified by the characteristics of an ideal impedance matching transformer.

$$A = ng_m \left(\frac{Z_o}{2}\right)\sqrt{\frac{Z_{o2}}{Z_o}} = \frac{n}{2} \; g_m\sqrt{Z_{o1} \; Z_{o2}} \tag{9}$$

In review, the main advantage of using the distributed amplifier with vacuum tubes is in the addition of individual tube gains without increasing the effective shunt capacitance.

CHAPTER II -- EFFECTIVE AMPLIFYING DEVICES

Although they may often be overlooked, certain properties are necessary in an amplifying device before it can be used to advantage in a distributed amplifier.

First of all, the term "amplifying device" should be explained: it is a general active network which exhibits a power gain and may consist of passive as well as active components, or, specifically, a vacuum tube or transistor with passive compensation networks at the input and/or output terminals.

To be useful in a distributed amplifier, this device must have a generally imaginary input impedance as will be demonstrated. (The same statement applies to the output impedance of these devices, but this factor will not be a problem in the subsequent analysis).

We will now consider the result of trying to use the distributed principle when the amplifying device has one of the following characteristics:

1. pure shunt capacitance
2. pure shunt inductance
3. pure shunt resistance

The case of the shunt capacitance is the one mentioned in the simplified analysis of the lossless tube distributed amplifier. Repeating for comparison, the gain bandwidth product of the single device is limited by the input (and output) shunt capacitances. The distributed amplifier allows an adding of individual device gains without increasing the effective shunt capacitance.

The instance of a device having purely shunt inductance is mentioned not for its practical value, but to complete the overall picture. Such a device, if it were dependent on its input voltage for its gain, would have a loss of gain at low frequencies when used with a resistive driving source. A distributed amplifier could then be built using high pass filter sections as the input and output lines. Again, this distribution would be used not for the frequency characteristic of the filters but because this type of filter uses inductances as shunt reactive elements. The result, of course, is the achievement of a higher gain at a low frequency by adding the individual device gains without decreasing the shunt inductance.

The third case occurs when the device has a purely resistive input. This case is of primary importance because many transistors exhibit this characteristic over a large part of their useful frequency range (see Chapter III). From a power standpoint, if the amplifying devices all absorb real power as a part of their operation, placing them in parallel cannot increase the overall power gain of the system. It will next be shown that, in general, no type of passive network, whether distributed or not, can be conceived which would allow k such amplifying devices to produce more power gain (when connected in parallel) than a single such device can.

1. Let each of these devices amplify power with a gain of G.

2. The power delivered to these devices (P) collectively is equal to the power into the input network (P_{in}), less the network power losses (P_{il}).

$$P'_i + P'_2 + P'_3 + \ldots + P'_n + \ldots P'_k = P_{in} - P_{il} \tag{10}$$

3. The power delivered at the output of the individual amplifying devices will be GP'_n, or collectively,

$$GP'_1 + GP'_2 + \ldots + GP'_n + \ldots GP'_k \text{ or } G\,(P_{in} - P_{il}) \tag{11}$$

4. The power reaching the output termination of the output passive network will be equal to the collective device power output less output network losses (P_{ol}).

$$P_{out} = G\,(P_{in} - P_{ie}) - P_{ol} \tag{12}$$

5. Then the total power gain ($G_T = P_{out}/P_{in}$) follows:

$$G_T = \frac{GP_{in} - G\,P_{il} - P_{ol}}{P_{in}} \tag{13}$$

$$G_T = G - \frac{(GP_{ie} + P_{ol})}{P_{in}} \tag{14}$$

As a limiting case, if there are no losses in the input and output filters themselves, $G_T = G$, or the total gain is equal to the gain of a single amplifying device.

Now if these resistive input devices were not merely placed in parallel but were placed at the nodes of a low pass filter network, the principle effect would be to add the characteristics of the filter to those of the amplifying devices. The primary effects would be to increase signal losses and to cause a phase shift near the cutoff frequency of the filters. This phase shift in itself does nothing to increase the performance of the system.

As will be shown in the next chapter, the input of most transistors is a combination of both the resistive and capacitative situations, thus causing a compromise in performance between two of the special situations covered above.

CHAPTER III -- TRANSISTOR INPUT CHARACTERISTICS

In order to visualize more easily the effect that the transistor input parameters will have in a distributed amplifier, an equivalent circuit is used. The following circuit is given by a transistor manufacturer as being valid in the useful frequency range of the drift type transistor (grounded emitter configuration) (Figure 2).

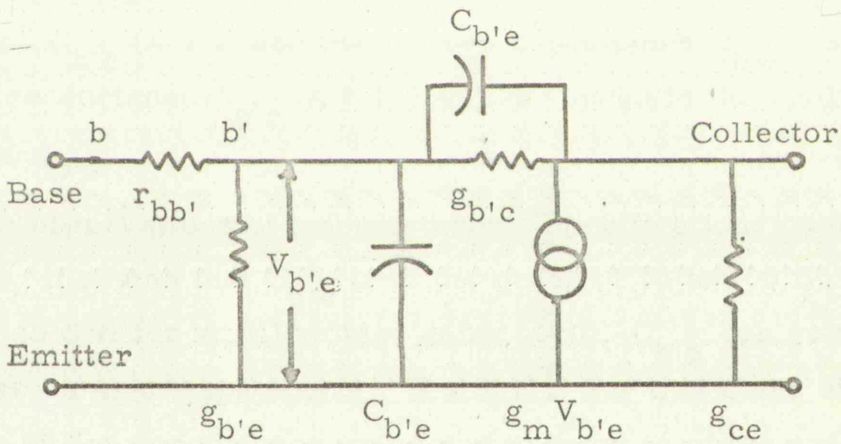

Figure 2

This equivalent circuit shows the bilateral nature of the transistor. This characteristic can be reduced by using neutralization [3], however the most effective circuit for this requires that the output be isolated from the input. For any particular gain (A), the following unilateralization seems feaseable (Figure 3).

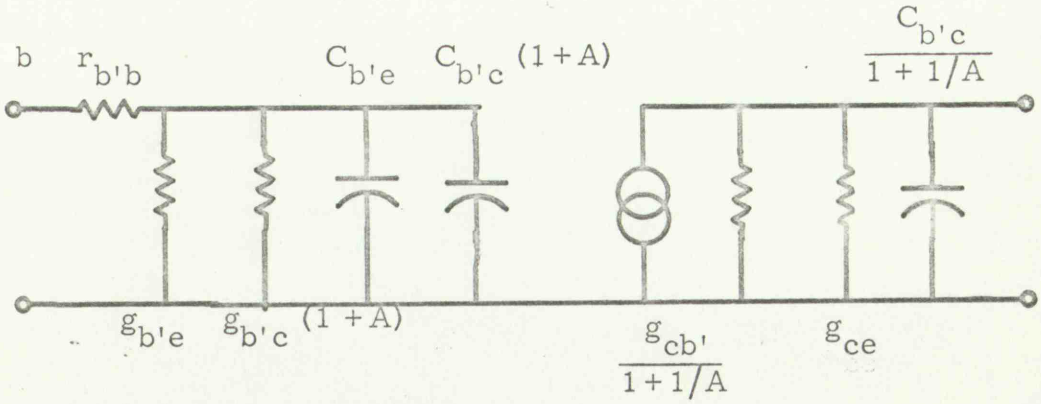

Figure 3

The input capacitance is now a shunt combination of the Miller capacitance* $C_{b'c}$ (A + 1) and the storage capacitance $C_{b'e}$. Similarly the Miller conductance $G_{b'c}$ (A + 1) has been added to the emitter conductance $g_{b'e}$.

From observations of manufacturer's specifications on drift RF transistors, it seems that $C_{b'e}$ is of the order of 50 to 100 times larger than $C_{b'c}$, so that for small voltage gains (< 10), $C_{b'c}$ can actually be neglected as an input capacitance. Similarly, for this class of transistor, the Miller conductance (collector to base) is of the order of 1000 to 2000 times less than the emitter to base conductance, and thus may be neglected for low voltage gains. The simplified unilateral equivalent circuit is now reduced to that of Figure 4.

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*The Miller effect is the apparent increase in grid to plate capacitance (conductance) at the grid of a triode tube due to the negative voltage gain at the plate.

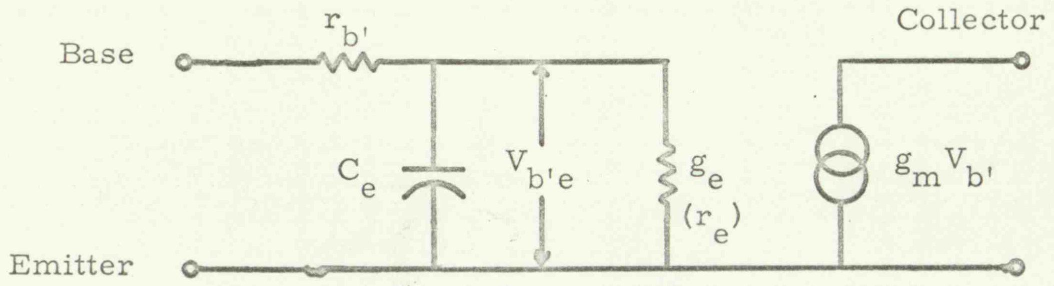

Figure 4

It was mentioned at the end of the last chapter that the input circuit to the transistor was a combination of shunt resistance and capacitance. One of the first goals of this thesis was to undertake the measurement of these values for a particular transistor. The methods and results are given in the appendix.

The input impedance can be taken as a complex quantity $Z_{in} = R_{in} + JX_{in}$ or in polar coordinates $|Z| \underline{|\theta}$ where $|Z|$ is the absolute value of the impedance and θ is the reactive angle:

$$\theta = \text{arc tan} \left|\frac{X}{R}\right| \tag{15}$$

This ratio of X/R is also the Q of the input capacitance. As can be anticipated from the equivalent circuit (Figure 4), both the real and imaginary components are frequency dependent:

$$R_{in} = r_{b'} + \frac{r_e}{(\omega C_e r_e)^2 + 1} \tag{16}$$

$$X_{in} = \frac{\omega C_e r_e^2}{(\omega C_e r_e)^2 + 1} \tag{17}$$

Where:

$r_{b'}$ is the base resistance

r_e is the emitter resistance

ω is the radian frequency

C_e is the emitter to base capacitance

As the Q is dependent on both of these parameters, it too can be expected to vary with frequency according to the equation

$$Q = \left|\frac{X}{R}\right| = \frac{r_e \omega C_e}{r_{b'}/r_e \left[(r_e \omega C_e)^2 + 1 \right] + 1} \tag{18}$$

Since the successful operation of the distributed amplifier is dependent on the Q of the reactances, arc tan Q has been plotted versus frequency for six 2N384 transistors in the appendix.

The formulae above can be worked out to yield the maximum Q and the frequency at which it occurs (derivation in Appendix B).

$$Q_{max} = \frac{\sqrt{1 + r_e/r_{b'}}}{2(r_{b'}/r_e + 1)} \tag{19}$$

$$f_{Qmax} = \frac{1}{2\pi C_e}\sqrt{\frac{r_{b'}/r_e + 1}{r_{b'} r_e}} \tag{20}$$

In the above equation, the maximum Q is dependent only on the relation of $r_{b'}$ to r_e and is not at all dependent on C_e. The frequency at which this maximum Q occurs is of course directly dependent on the capacitance C_e.

For the 2N384 transistor, the maximum Q for the manufacturers specifications amounts to 2.14. This is reasonably close to the results obtained experimentally. A rough plot of the variation of Q with frequency is shown in Figure 5.

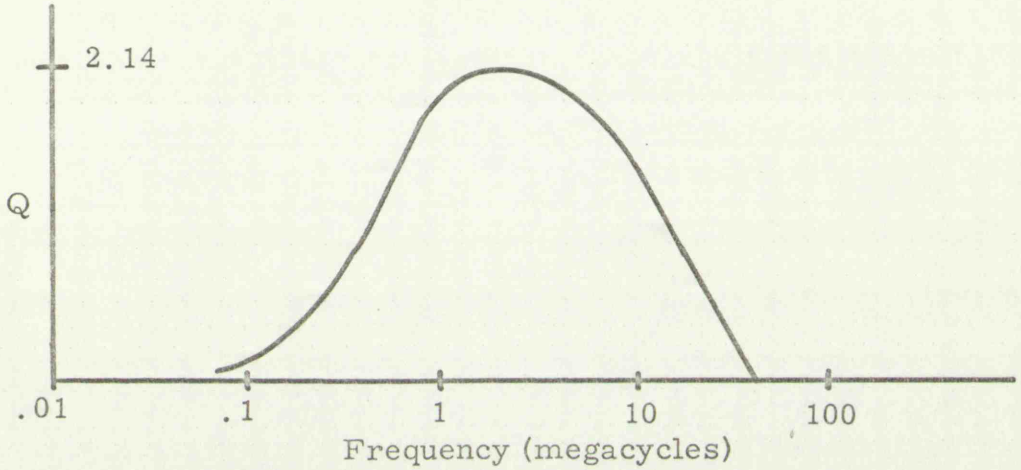

Figure 5

As can be seen, the Q approaches zero for low as well as high frequencies. The maximum Q is about 2 and it occurs at approximately 4 mc. The alpha cutoff frequency* of this transistor is 100 mc, and it can give useful gain up to 250 mc.

In conclusion, it can be seen that the input capacitance to a grounded emitter transistor is of significance only at the "middle" frequencies and then only at a very poor Q.

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*The frequency at which alpha, the forward current transfer ratio for a common base transistor, drops to 70.7 percent of its low frequency value.

CHAPTER IV -- EFFECT OF AMPLIFIER LOSSES

This chapter investigates the maximum power loss allowable at the input to an amplifying device before this device is no longer useable in a distributed amplifier. The approach used will be that of comparing the gain of a single device (such as a transistor video amplifier) with the gain of a distributed amplifier using these gain devices.

It has been shown, that for vacuum tube distributed amplifiers, circuit losses definitely introduced a new, although much higher, gain-bandwidth "product" [4] (see Equation 3). It will be shown here that similar losses occur in a transistor distributed amplifier at the very frequency range in which distribution would be expected to do some good.

In comparing a transistor distributed amplifier to any other type of transistor video amplifier, full advantage will be given to the distributed case by allowing the use of the comparison amplifier as the active part of the distributed amplifier. To repeat, if a transistor video circuit "D" is to be used as a comparison, then the distributed amplifier will use "n" of these "D" circuits along its input and output filter nodes.

Now, if one takes the propagation function $\gamma = \alpha + j\beta$ where α is the attenuation constant in nepers per input filter section and β is the phase shift per section, and allows the gain per amplifying device "D" to be A, then the total gain of the resulting distributed amplifier (neglecting phase shift and losses in the output line) will be:

$$A_d = \frac{Ae^{\frac{-\alpha}{2}}}{2} + \frac{Ae^{\frac{-3\alpha}{2}}}{2} + \ldots + \frac{Ae^{-\left(\frac{2n+1}{2}\right)\alpha}}{2} \qquad (21)$$

$$A_d = \frac{A}{2} e^{-\alpha} (1 + e^{-\alpha} + e^{-2\alpha} + \ldots e^{-n\alpha}) \tag{22}$$

for an infinite number of transistors

$$A_d = \left(\frac{Ae^{\frac{-\alpha}{2}}}{2} \right) \left(\frac{1}{1 - e^{-\alpha}} \right) \tag{23}$$

Now α, in the pass band of a simple filter structure, is determined primarily by the Q's of the inductors and capacitors used. Normally the Q of the capacitors will be much higher than that of the coils. The coil Q is then the only one considered. However the Q of the input shunt capacity to a grounded emitter transistor (2N384) does not generally exceed a value of two (the Q varies among transistors of the same type). A theoretical solution based on the manufacturer's equivalent circuit yields this value (see Appendix A). Therefore, the Q of the shunt capacitance will be the only loss considered at this point. The solution for the distributed gain (A_d) follows.

$$\alpha = \frac{1}{2} \left(\frac{1}{Q_C} + \frac{1}{Q_C} \right) \frac{\partial \beta}{\partial (f/f_c)} \tag{24}$$

Since

$$\beta = 2 \text{ arc sin } (f/f_c)$$

Then

$$\frac{\partial \beta}{\partial (f/f_c)} = \frac{2}{\sqrt{1 - (f/f_c)^2}} \geq 2 \text{ for all } f < f_c \tag{26}$$

So

$$\alpha \geq \frac{1}{2}\left(\frac{1}{Q_C}\right)(2) = 1/Q_C \qquad (27)$$

Assume

$\alpha = 1/Q_C$ and $Q_C = 2$, then $\alpha = .5$

$$e^{-.5} = .607, \quad e^{-\alpha/2} = .779 \qquad (28)$$

$$A_d = \frac{A}{2}\left(.779 \frac{1}{1-.607}\right) = \frac{A}{2}\,\frac{.779}{.393} = \boxed{.99A = A_d} \qquad (29)$$

Therefore, if transistors alone are used (of the type tried) more gain would be obtained by using a single transistor. On the other hand, if a transistor amplifying circuit were found which had an input capacitive Q greater than two, and if the Q's of the other filter components (neglected in above analysis) were sufficiently high, then the distribution principle might yield an advantage.

CHAPTER V -- DIFFICULTIES OF ONE FILTER CONFIGURATION

It has been suggested that complete filter sections be used between transistor bases in order to cope with their resistive natures. Each of these filter sections would be terminated with m-derived half-sections in order to match a resistive transistor between filters. Each filter on the input line would have a different characteristic impedance such that there would be minimum mismatch at the transistor junction (see Figure 6).

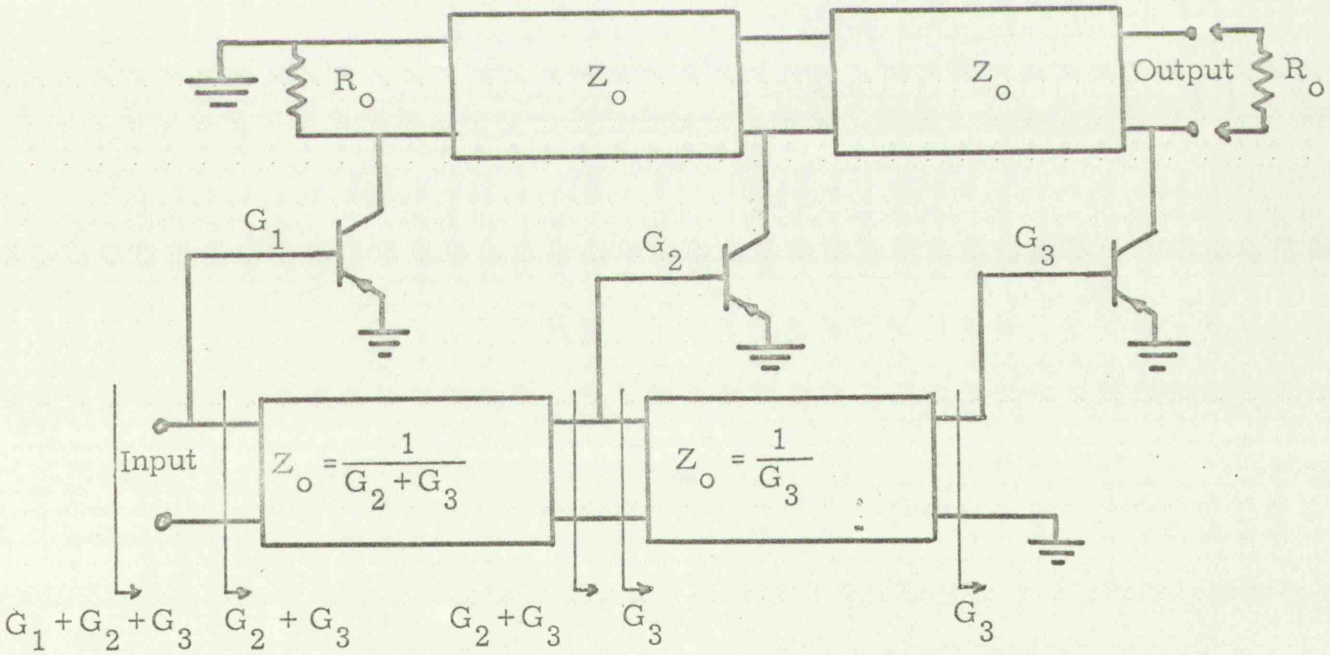


Figure 6

To determine the theoretical feaseability of such a design, a gain solution based on an ideal filter and an ideal resistive transistor will be made. The equivalent circuit shown at the right will be used to represent the transistor. The filter groups will all be lossless and constructed to match the resistive terminations appearing at each end. Each filter will have the same phase shift with respect to frequency. Accordingly, the transistorized distributed amplifier will appear as in Figure 8.

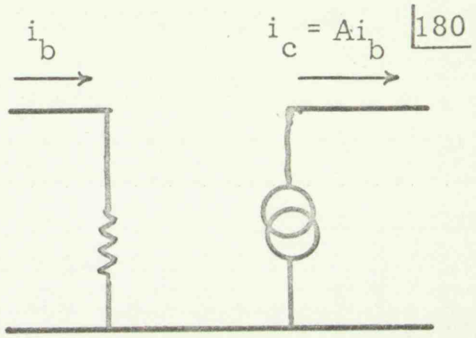


Figure 7

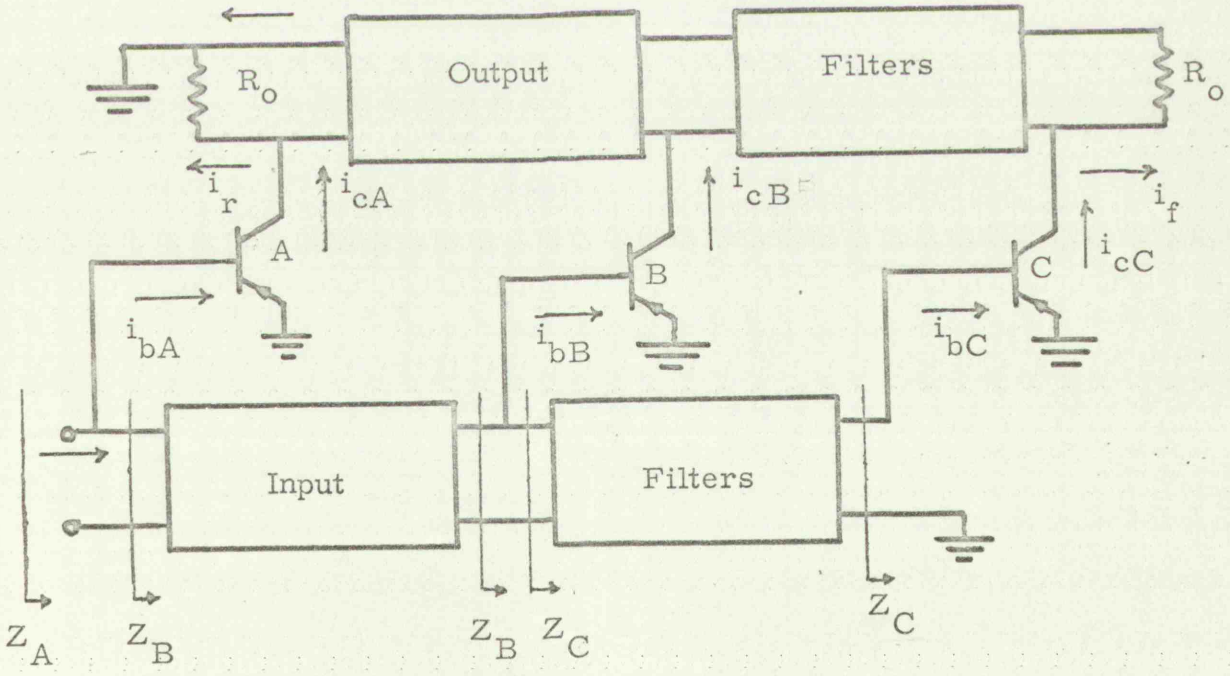


Figure 8

The proposed design was such that the impedance seen by each filter matched its characteristic impedance, as shown in Figure 7. Z_c = 50 ohms for a 50 ohm transistor, Z_b = 50 ohms in parallel with a 50 ohm filter or 25 ohms, and likewise, Z_a = 50/3 or 16.7 ohms. One third of the input current i_{in} flows into each of the three transistors, or i_{in}/k flows into each of k transistors. The current into the second transistor has been delayed θ degrees, or, referenced to i_{in},

$$i_{bB} = \frac{1}{3} i_{in} \underline{\left| \theta \right.} \ , \quad i_{bC} = \frac{1}{3} i_{in} \underline{\left| 2\theta \right.}$$

or in general,

$$i_{bn} = \frac{1}{k} (i_{in}) \underline{\left| (n-1)\theta \right.}$$

where i_{bn} is the base current for the nth transistor in an amplifier having a total of k transistors.

On the output line, there will be no loss in current since the output terminals of the transistor are taken to be current sources having zero shunt conductance. The collector current flowing from each transistor will be equally divided at low frequencies, each half flowing in opposite directions along the output filter lines, the currents from the individual transistors will add to each other vectorally at the forward and reverse filter terminations. As shall be shown, those arriving at the forward termination will be in phase, while in general, those at the reverse termination shall be out of phase.

The forward termination current for a three-transistor amplifier will be

$$\frac{1}{2} i_{c1} \underline{\left| 2\theta \right.} + \frac{1}{2} i_{c2} \underline{\left| \theta \right.} + \frac{1}{2} i_{c3} \tag{30}$$

Where I ... with ... having
... of k transistors

On the output ... there will be no loss in current since the output terminals of the transistors ... taken to be current sources having zero shunt conductance. ... current flowing from each transistor ... be equally divided ... two directions, each half flowing in opposite directions along the ... , the currents from the individual transistors will ... at the forward and reverse terminations. ... those arriving at the forward termination will be in phase, while in general, those at the reverse termination shall be out of phase.

... forward termination ... for a three-transistor amplifier ...

or in general,

$$i_f = \frac{1}{2}\sum_{n=1}^{k} i_{cn} \underline{\lfloor (k-n)\,\theta} \tag{31}$$

if there a a total of k transistors. At the reverse termination the current is

$$\frac{1}{2}\, i_{c1} + \frac{1}{2}\, i_{c2} \underline{\lfloor \theta} + \frac{1}{2}\, i_{c3} \underline{\lfloor 2\theta} \tag{32}$$

or in general,

$$i_r = \frac{1}{2}\sum_{n=1}^{k} i_{cn} \underline{\lfloor (n-1)\,\theta} \tag{33}$$

Now, substituting in the value for i_{cn},

$$i_{cn} = A\, i_{bn} \underline{\lfloor 180}$$

$$i_{cn} = A\,\frac{i_{in}}{n} \underline{\lfloor 180 + (n-1)\,\theta} \quad \text{for three transistors.} \tag{34}$$

$$i_f = \frac{1}{2}\left(\frac{1}{3}\, i_{in}\right) A \underline{\lfloor 180} \underline{\lfloor 2\theta} + \frac{1}{2}\left(\frac{1}{3} i_{in} \underline{\lfloor \theta}\right)\left(A \underline{\lfloor 180} \underline{\lfloor \theta}\right)$$

$$+ \frac{1}{2}\left(\frac{1}{3}\, i_{in} \underline{\lfloor 2\theta}\right)\left(A \underline{\lfloor 180}\right) \tag{35}$$

$$i_f = \frac{1}{2} A \underline{\lfloor 180} \left(\frac{1}{3}\, i_{in} \underline{\lfloor 2\theta} + \frac{1}{3}\, i_{in} \underline{\lfloor 2\theta} + \frac{1}{3}\, i_{in} \cdot \underline{\lfloor 2\theta}\right) \tag{36}$$

$$i_f = \frac{1}{2}\, i_{in}\, A \underline{\lfloor 180 + 2\theta}\,. \tag{37}$$

The total amplifier gain

$$A_t = if/i_{in} = \frac{1}{2} A \angle 180 + 2\theta \qquad (38)$$

At the reverse termination, the current is given by:

$$i_r = \frac{1}{2} A \angle 180 \left(\frac{1}{3} i_{in} \angle \theta + \frac{1}{3} i_{in} \angle 2\theta + \frac{1}{3} i_{in} \angle 4\theta \right) \qquad (39)$$

In other words, at the forward terminal of the output filter (for the ideal situation) one obtains 1/2 of the gain of an individual transistor shifted by a multiple of the filter phase characteristic. At the reverse termination, the individual currents do not arrive in phase unless $\theta = n\,\pi$. The forward output current is in general for k transistors:

$$i_f = \sum_{n=1}^{k} \left[\frac{1}{k} i_{in} \angle (n-1)\theta \right] \left[A \angle 180 \right] \left[\frac{1}{2} \angle (k-n)\theta \right] \qquad (40)$$

$$= \sum_{n=1}^{k} \frac{1}{2k} i_{in} A \angle 180 + (n - 1 + k - n)\,\theta \qquad (41)$$

$$= \frac{1}{2} \sum_{n=1}^{k} \frac{1}{k} i_{in} A \angle 180 + (k-1)\,\theta = \frac{1}{2} i_{in} A \angle 180 + (k-1)\,\theta \qquad (42)$$

The total generalized gain is:

$$A_t = \frac{1}{2} A \angle 180 + (k-1)\,\theta \qquad (43)$$

In conclusion, for the idealization above, the overall current gain was 1/2 of that for a single transistor, regardless of the number of transistors used; whereas, for tubes (ideally non-resistive on input), the total mutual conductance is n/2 times that for a single tube where n is the number of tubes used (see Equation 9).

CHAPTER VI -- EFFECTS OF AMPLIFIER COMPENSATION

As derived in Chapter III, the maximum Q is a function of $r_{b'}$ and r_e.

$$Q_{max} = \frac{\sqrt{1 + r_e/r_{b'}}}{2(r_{b'}/r_e + 1)} \tag{44}$$

and the frequency at which this maximum occurs is given by:

$$f_{Qmax} = 2\pi C_e \sqrt{\frac{r_{b'}/r_e + 1}{r_{b'} r_e}} \tag{45}$$

Now if an R-C compensating network is added to the input of the transistor such that the overall input Q is sufficiently raised, and if its maxima is shifted upward in frequency, then it seems possible that an advantage can be realized when used in a distributed amplifier.

One circuit which has been tried by a transistor manufacturer [1] is shown below in Figure 9.

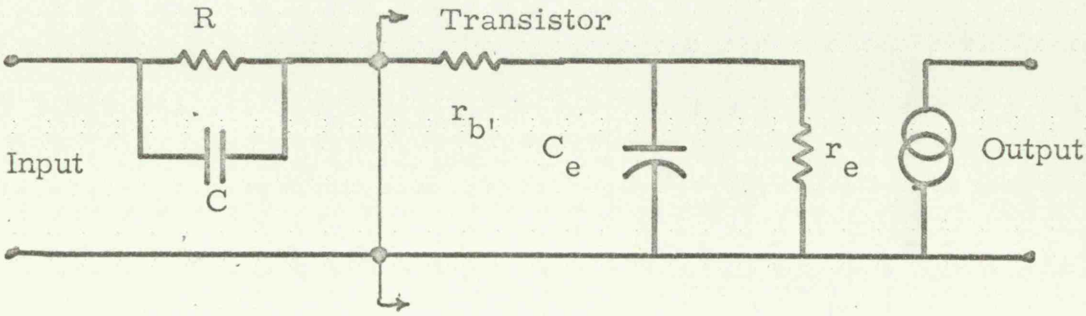


Figure 9

The primary reason given for the use of this circuit was that it would compensate for the high frequency roll-off of beta (the grounded emitter forward current gain). It was mentioned in the literature [1] that the special transistor used did not conform to the standard equivalent circuit (Figure 2). In lieu of this information (input parameters), it was not possible to speculate on the Q of this transistor input (Fairchild 2N706).

This circuit will have a similar frequency compensating effect on the 2N384, but it also has the effect of increasing the maximum Q and raising the frequency at which it occurs. Of course the gain is reduced by this procedure, but this may be compensated for by the additive gain character of the distributed amplifier.

If one applies such a frequency compensating circuit as shown in Figure 9, and chooses $R = nr_e$ and $C = 1/n\ C_e$, the circuit can be re-drawn as shown in Figure 10.

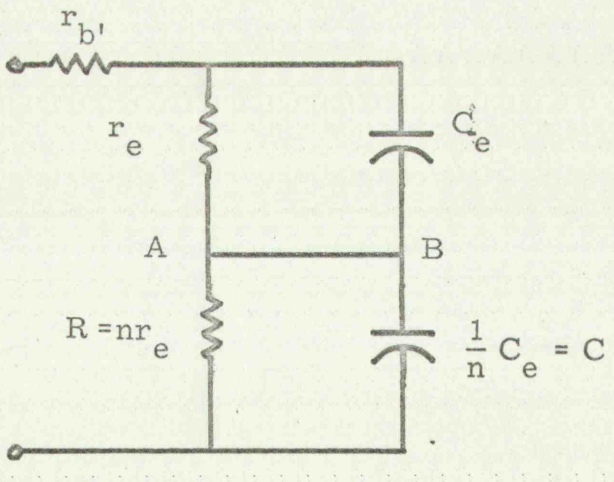
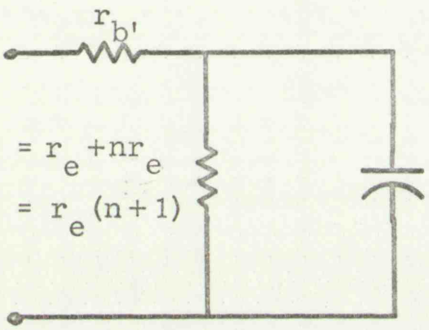


Figure 10

The right-hand side of this network appears as, and acts like, a frequency compensated attenuator. Since the voltage amplitudes and phases at A and B are equal whether or not A and B are connected directly, the connection AB can be disregarded and the circuit becomes that shown in Figure 11.



$$R' = r_e + nr_e$$
$$R' = r_e (n+1)$$

$$C' = \frac{C_e \left(\frac{1}{n} C_e\right)}{C_e + \frac{1}{n} C_e} \quad 6.3$$

$$C' = \frac{C_e}{n+1} \tag{46}$$

Figure 11

From Equation 45 we see that the substitution of C' for C will raise the frequency of maximum Q by (n + 1).

$$f' = \frac{1}{2\pi} \left(\frac{n+1}{C_e}\right) \sqrt{\frac{r_{b'}/r_e + 1}{r_{b'} r_e}} \tag{47}$$

$$f' = (n+1) f \tag{48}$$

Due to the voltage divider characteristic, the gain will be reduced by the ratio of component values:

$$\frac{A'}{A} = \frac{r_{b'} + r_e}{r_{b'} + r_e + nr_e} = \frac{r_{b'} + r_e}{r_{b'} + r_e (n+1)} \, . \tag{49}$$

if $r_e >> r_{b'}$ then $r_{b'}$ can be neglected, giving:

$$\frac{A'}{A} \approx \frac{r_e}{r_e(n+1)} = \frac{1}{n+1} \tag{50}$$

Note, however that as X_{ce} becomes small at high frequencies, that this approximation is not valid.

So, if an amplifier design bandwidth is based on the frequency of maximum capacitor Q, then the gain decreases as the bandwidth increases such that:

$$(A')(f_c') = \left(\frac{A}{n+1}\right)(n+1)\, f_c = Af_c \tag{51}$$

In other words, the gain-bandwidth product remains approximately constant. However the payoff to this method lies in the increase in Q. This increase occurs as follows:

$$Q_{max} = \frac{\sqrt{1 + r_e/r_{b'}}}{2\,(r_{b'}/r_e + 1)} \tag{52}$$

As an approximation, $r_e/r_{b'}$ is normally 20 or greater and increases as r_e or its equivalent, so that the assumption that $r_e/r_b >> 1$ introduces an error less than 5 percent. Therefore:

$$Q_{max} \approx \frac{1}{2}\sqrt{r_e/r_{b'}} \tag{53}$$

The Q of the new circuit,

$$Q' = \frac{1}{2}\sqrt{\frac{r_e\,(n+1)}{r_{b'}}} \tag{54}$$

the improvement in Q

$$\frac{Q'}{Q} = \frac{\frac{1}{2}\sqrt{\dfrac{r_e\,(n+1)}{r_{b'}}}}{\frac{1}{2}\sqrt{r_e/r_{b'}}} = \sqrt{n+1} \tag{55}$$

This says then that the RC compensating network discussed can increase the Q of the input of the amplifying device by approximately the square root of (n + 1). The higher the n, the better the approximation.

Therefore, if a transistor alone does not have sufficient Q to enable its direct use in a distributed amplifier (see Chapter IV, it may be possible to increase the Q sufficiently by the use of an RC compensating network.

CHAPTER VII -- CONCLUSION

The input characteristics of some transistors prevent their direct use in a distributed amplifier. The concept of distributed amplification demands that the input to the amplifying device be a reactance of sufficient Q to be used as one of the shunt elements of a filter chain (or artificial transmission line). If this Q is too low, then the loss of the filter network cannot be compensated by the use of additional "parallel" amplifying devices.

One possible solution has already been suggested, that of an RC compensating network that will raise the Q and reduce the capacitance of the input to a grounded emitter transistor. Another solution is to find a transistor having the necessary input "quality."

APPENDIX A

DERIVATIONS OF INPUT PARAMETERS

For symbols, see equivalent input circuit for transistor, Figure 4.

$$Z_{in} = r_b + \frac{r_e/j\omega c}{r_e + 1/j\omega c} = \frac{r_b - (jr_e/\omega c)\,(r_e + j/\omega c)}{r_e - j/\omega c\,(r_e + j/\omega c}$$

$$= r_b = \frac{jr_e^{\,2}/\omega c + r_e/\omega^2 c^2}{r_e^{\,2} + 1/\omega^2 c^2}$$

$$Z_{in} = \frac{r_b\left(r_e^{\,2} + 1/\omega^2 c^2\right) + \left(r_e/\omega^2 c^2\right)}{(\qquad)} - \frac{jr_e^{\,2}/\omega c}{(\qquad)}$$

$$Q = \frac{|X|}{|R|} = \frac{r_e^{\,2}/\omega c}{r_b\left(r_e^{\,2} + 1/\omega^2 c^2\right) + r_e/\omega^2 c^2}$$

$$= \frac{r_e^{\,2}}{r_b\omega c\left(r_e^{\,2} + 1/\omega^2 c^2\right) + r_e/\omega c}$$

$$= \frac{r_e^{\,2}\omega c}{r_b\omega^2 c^2\left(r_e^{\,2} + 1/\omega^2 c^2\right) + r_e}$$

$$= \frac{r_e^{\,2}\omega c}{r_b\omega^2 c^2\left(r_e^{\,2} + 1/\omega^2 c^2\right) + r_e}$$

$$Q = \frac{r_e \omega c}{r_b/r_e \left[\left(r_e \omega c\right)^2 + 1\right] + 1}$$

$$Q = \frac{r_e \omega c}{r_b/r_e \left[\left(r_e \omega c\right)^2 + 1\right] + 1} = \frac{r_e \omega c}{r_b r_e c^2 \omega^2 + r_b/r_e + 1}$$

taking first derivative with respect to ω and setting equal to zero.

$$\frac{\partial Q}{\partial \omega} = \frac{r_e \omega c \left(r_b r_e c^2 2\omega\right) - \left(r_b r_e c^2 \omega^2 + r_b/r_e + 1\right) r_e c}{\left(r_b r_e c^2 \omega^2 + r_b/r_e + 1\right)^2} = 0$$

$$0 = \left(r_b r_e c^2 2\omega\right) - \left(r_b r_e c^2 \omega^2 + r_b/r_e + 1\right)$$

$$0 = r_b r_e c^2 2\omega^2 - r_b r_e c^2 \omega^2 - r_b/r_e - 1$$

$$c^2 \omega^2 = \frac{r_b/r_e + 1}{2r_b r_e - r_b r_e}$$

$$c\omega_2 = \sqrt{\frac{r_b/r_e + 1}{r_b + e}} \qquad \omega_2 = 1/c \sqrt{\frac{r_b/r_e + 1}{r_b + e}}$$

for 2N384 $r_b = 50$, $r_e = 1000$, $c = 100 \times 10^{-12}$

$$\omega_2 = 1/100 \times 10^{-12} \sqrt{\frac{50/1000 + 1}{50{,}000}} = 10^{12}/100 \sqrt{\frac{1.05}{50{,}000}}$$

$$= 10^{12}/100 \sqrt{21 \times 10^{-6}}$$

$\omega_2 = 45.8 \times 10^6$ radians = 7.3 mc = frequency of maximum Q

$$Q = \frac{r_{e\omega c}}{r_b/r_e\left[\left(r_e\omega c\right)^2 + 1\right] + 1}$$

$$= \frac{1000 \times 45.8 \times 10^6 \times 100 \times 10^{-12}}{50/100\left[(1000 \times 45.8 \times 10^6 \times 100 \times 10^{-2})^2 + 1\right] + 1}$$

$$Q = \frac{4.58}{.05\left[21 + 1\right] + 1} = 4.58/2.1 = 2.14$$

Derivation of maximum input Q

From previous page

$$Q = \frac{r_e\omega c}{r_b/r_e\left[\left(r_e\omega c\right)^2 + 1\right] + 1}$$

Also maximum Q occurs at $\omega_2 = 1/c \sqrt{\dfrac{r_b/r_e + 1}{r_b r_e}}$

$$Q_{max} = \frac{r_e c \cdot 1/c \sqrt{\dfrac{r_b/r_e + 1}{r_b r_e}}}{r_b/r_e\left[\left(r_e c \; 1/c \sqrt{\dfrac{r_b/r_e + 1}{r_b r_e}}\right)^2 + 1\right] + 1}$$

$$Q_{max} = \frac{\sqrt{\dfrac{r_b r_e^3/r_e + r_e^2}{r_e}}}{r_b/r_e\left[\dfrac{r_e^2(r_b/r_e + 1)}{r_b r_e} + 1\right] + 1}$$

$$Q_{max} = \frac{\sqrt{\dfrac{r_b + r_e}{r_b}}}{r_b/r_e + 1 + r_b/r_e + 1} = \frac{\sqrt{1 + r_e/r_b}}{2(r_b/r_e + 1)} \longleftarrow Q_{max}$$

for $r_b = 50\Omega$, $r_e = 1000$

$$Q_{max} = \frac{\sqrt{1 + 1000/50}}{2(50/1000 + 1)} = \frac{\sqrt{21}}{2(1.05)} = \frac{4.58}{2.1} = 2.14$$

$$Q_{2N384\ max} = 2.14$$

APPENDIX B

MEASUREMENT METHODS

I. Voltage Measurements

Essentially all forms of electronic measurement depend upon the reaction of the unknown quantity to a voltage. The measured response is also often in terms of a voltage. Similarly, the measurements made for this thesis involved the use of a device which could measure radio frequency voltages with reasonable accuracy. Because of the frequencies involved, this device must have a very wide bandpass and, due to the nature of the transistors, must be sensitive to voltages in the range of 1 to 10 millivolts. The Tektronix oscilloscope available had neither sufficient bandwidth nor sensitivity.

The first attempt at using germanium diode demodulators driving a 20 microampere movement meter satisfied the wide frequency requirement but needed too much radio frequency power and was not sensitive enough to the low voltages.

The low voltage requirement may need explanation. When small signal theory is involved, the signal must be small enough not to upset bias voltages, and it must remain in the linear operating region of the transistor. It was found that the measured input resistance apparently decreased with smaller signal voltages until the region of 10 millivolts was reached. This effect is due to the nonlinearity involved when the signal voltage is greater than the low bias voltage (around 20 millivolts).

[illegible] millivolts. The Tektronix oscilloscope available had neither sufficient bandwidth [illegible]

The first attempt at using germanium diode demodulators driving a 20 microampere [illegible] meter [illegible] the wide frequency range required but needed too much radio frequency power and was not sensitive enough to the low voltages.

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In the measurement methods used, it was not convenient to use a DC amplifier in conjunction with the diode demodulator, although this probably would have worked very well.

Instead, a pulsed radio frequency source was used (as from an RF sweep generator with the sweep width adjusted to zero). The resulting signal from the demodulator was a low frequency AC signal which was easily amplified by a conventional low noise amplifier and displayed on an oscilloscope and/or a peak reading vacuum tube voltmeter. In respect to this method, it should be mentioned that the low frequency noise generated by the transistor will also appear at the demodulator and on the scope trace. Thus the amplitude of the RF test voltage must be a compromise between the noise voltage and the nonlinearity voltage limit.

The next problem came about due to the extreme nonlinearity of the diode demodulator at low signal amplitudes. Table B. 1 shows the relative demodulator outputs for various known RF voltages. The output resulting from a 100 millivolt RF input is taken as the reference. The last column indicates the error induced by the nonlinearity.

TABLE B. 1

RF ratio (db)	RF voltage	Measured ratios	Output	Error
0	100 mv	1	100 mv	0
-10	31. 6	. 215	21. 5	-31. 6%
-20	10	. 133	2. 0	-80%
-30	3. 16	. 1	. 23	-93%

The problem of detector nonlinearity was circumvented by making all voltage measurements occur at one constant voltage (around 8 millivolts RF).

The effect of frequency dependent loading by the detector was next investigated. As will be explained later, some of the voltages were measured at points having an RF source impedance of 200 ohms. The stray

shunt capacitance of the detector caused a loading of the RF source at higher frequencies. It was calculated that the capacitance needed to cause this amount of shunting was about 10 micromicrofarads. The variation of loading with frequency is indicated for two conditions in Figure B. 1.

In conclusion, considering the drop in the circuit impedances at the higher frequencies, the error would not be appreciable at any frequency of interest.

II. Impedance Measurements

As indicated in the body of the thesis, a prime concern was the input impedance of the transistor. This measurement was accomplished by obtaining the ratio of V_T to V_Q in the circuit shown in Figure B-2.

The RF voltage would first be adjusted to give a near full scale reading on the VTVM. Next the switch S1 would be thrown to the other position and the RF step attenuator adjusted until the vacuum tube voltmeter read the same as before. The amount of signal change required in db, gave the ratio of voltages between points T and Q.

This ratio will give the input impedance of the transistor in terms of the series resistance for real or resistive impedances as follows:

$$\frac{E_T}{E_Q} = \frac{r_{input}}{r_{input} + R} \qquad \text{(B. 1)}$$

A plot of this relation for a 200 ohm series resistor and the ratio expressed in db is given in Figure B. 3.

A check was next made on the accuracy of the measurement method and equipment. Most of the error must be attributable to the RF db attenuator. It had been used by the military for fairly accurate RF attenuation. A home made attenuator having 10- and 20-db steps was constructed and

Loading Effects of RF Voltmeter

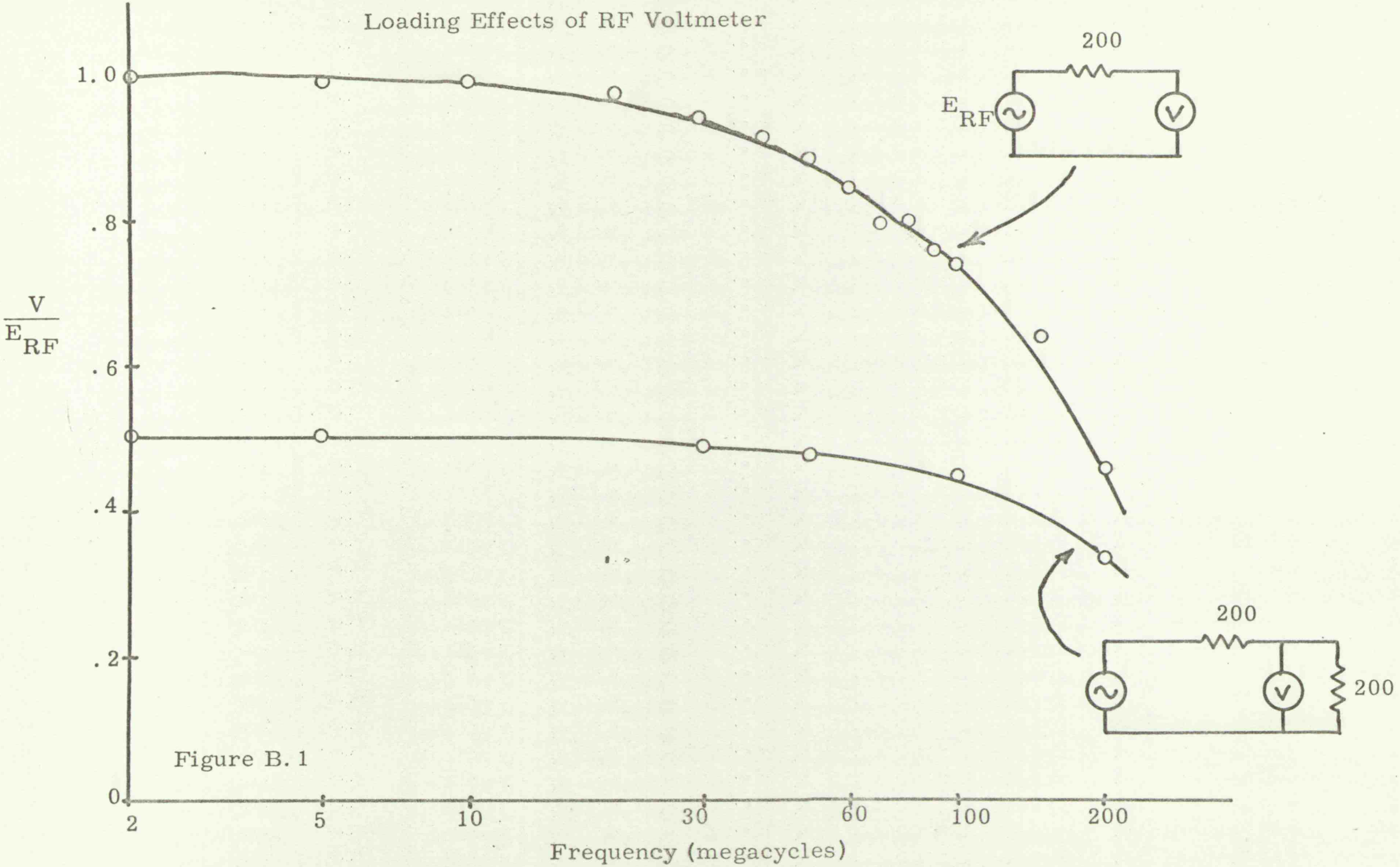
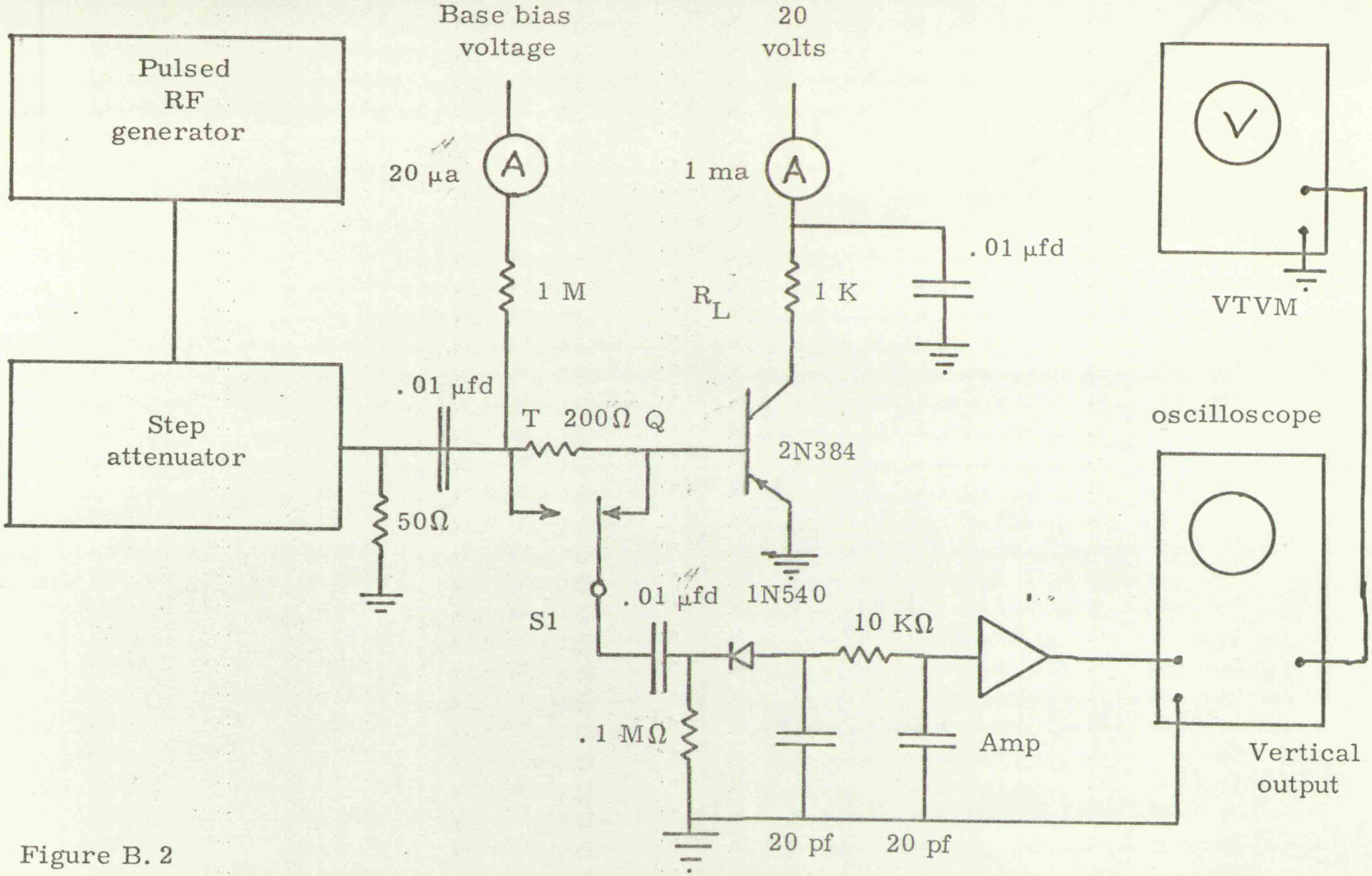
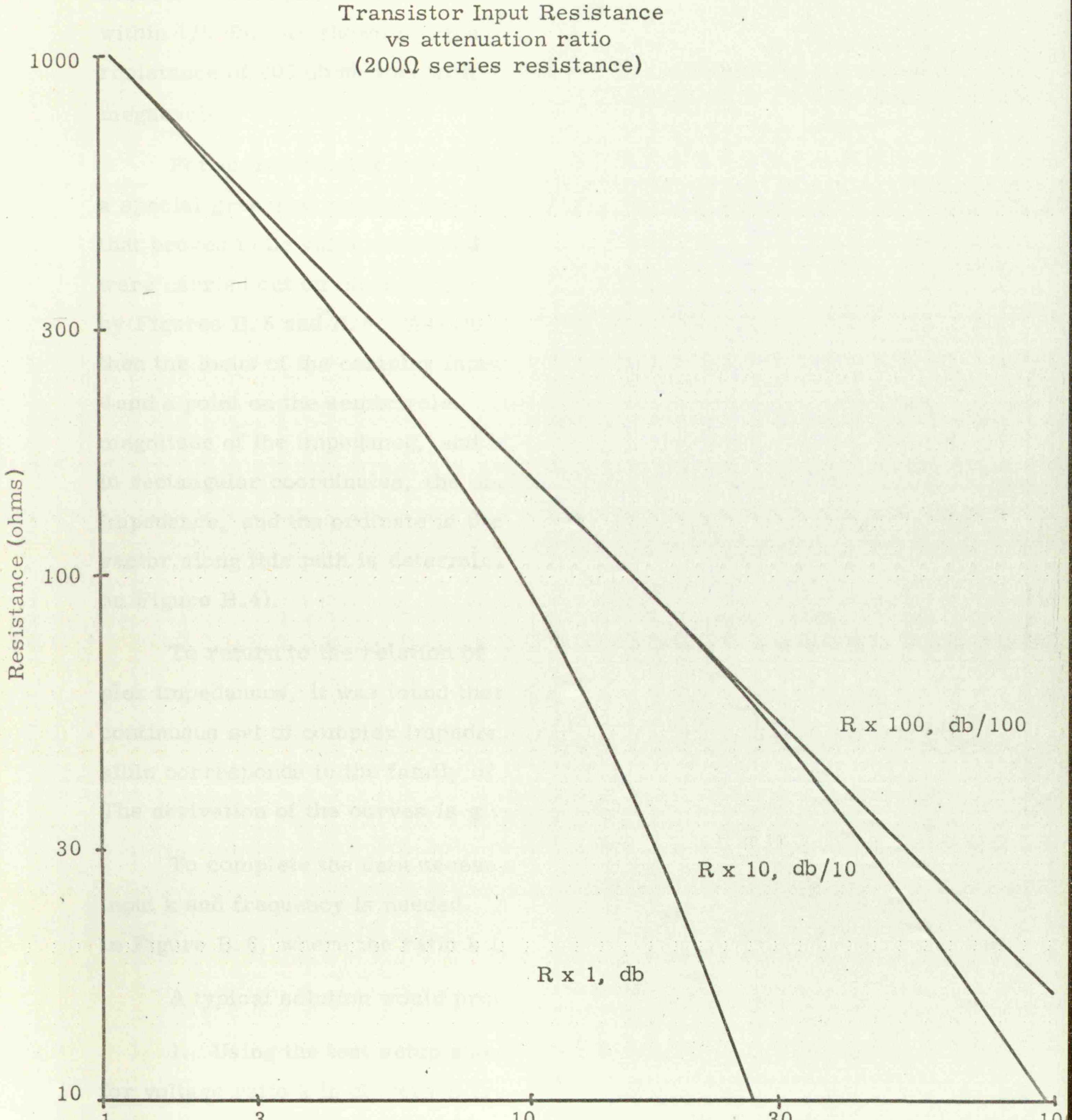


Figure B.1



Pulsed RF generator
Step attenuator
Base bias voltage
20 μa
1 M
. 01 μfd
50Ω
T 200Ω Q
S1
20 volts
1 ma
R_L
1 K
. 01 μfd
2N384
. 01 μfd
1N540
. 1 MΩ
10 KΩ
20 pf
20 pf
Amp
VTVM
oscilloscope
Vertical output

Figure B. 2



Transistor Input Resistance
vs attenuation ratio
(200Ω series resistance)
1000
300
100
30
10
Resistance (ohms)
1
3
10
30
100
Attenuation Ratio (db)
R x 100, db/100
R x 10, db/10
R x 1, db

Figure B. 3

checked against the military model. It is felt that these measurements are accurate within plus or minus one db, but readings were generally taken to within 1/5 db. As shown in Figure B. 1 the voltage ratio caused by a shunt resistance of 200 ohms was with 2 percent of . 5 at frequencies up to 30 megacycles.

For more complex impedance (namely that of the input to a transistor), a special graphical method was worked out which, under certain assumptions that proved to be valid, provided rapid solutions. Although these solutions were carried out on much larger sheets of paper, the method is demonstrated by Figures B. 5 and B. 6. Assuming an equivalent circuit (also Figure B. 4), then the locus of the complex input impedance vector must lie between point 0 and a point on the semicircle. The length of the vector represents the magnitude of the impedance, and the angle is the phase associated with it. In rectangular coordinates, the abscissa is the real or resistive part of the impedance, and the ordinate is the imaginary part. The position of the vector along this path is determined by the frequency involved (see equation on Figure B. 4).

To return to the relation of the voltage ratio to the ratio of two complex impedances, it was found that each voltage ratio was satisfied by a continuous set of complex impedances. Thus the set of voltage ratios possible corresponds to the family of impedance curves shown in Figure B. 5. The derivation of the curves is given at the end of this appendix.

To complete the data necessary to this method, the relation between input k and frequency is needed. A typical plot for a transistor is shown in Figure B. 6, where the ratio k is given in db.

A typical solution would proceed as follows:

1. Using the test setup shown in Figure B. 2, data is taken and plotted for voltage ratio k in db versus frequency. (See Figures B. 6 through B. 11).

2. At low and high frequencies, the voltage ratio is not a function of frequency, hence the impedance must be resistive. At these points, then,

absci[illegible]

about[illegible]

within [illegible]

resisti[illegible]

imaginary [illegible]

[illegible]

a [illegible]

the [illegible]

were [illegible]

by [illegible]

then the [illegible] of the complex input impedance vector which [illegible]

Z and a [illegible]. The length of the vector [illegible]

magnit[illegible] impedance, [illegible] is the phase angle [illegible]

in rectangular coordinates, the abscissa is the real or resis[illegible]

impedance, and the ordinate is the imaginary part. The [illegible]

vector along this path is determined by the frequency [illegible]

in Figure B.4[illegible].

To return to the relation of the voltage ratio to [illegible]

[illegible]impedances, it was found that each voltage [illegible]

continuous set of complex impedances. Thus the se[illegible]

which corresponds to the family of impedance curves [illegible]

The derivation of the curves is given at the end of [illegible]

To complete the data necessary to this [illegible]

[illegible] frequency is needed. A [illegible]

in Figure B.6, where the ratio A is given in db.

A typical solution would proceed as follows:

[illegible] Using the test setup shown in Figure B.[illegible]

[illegible] voltage ratio A in db versus frequency. (See Fig[illegible]

[illegible]

[illegible]

Loci of Transistor input impedance

$$Z_Q = r_b' + \frac{r_e}{\omega^2 c^2 r_e^2 + 1} - j \frac{\omega c r_e^2}{\omega^2 c^2 r_e^2 + 1}$$

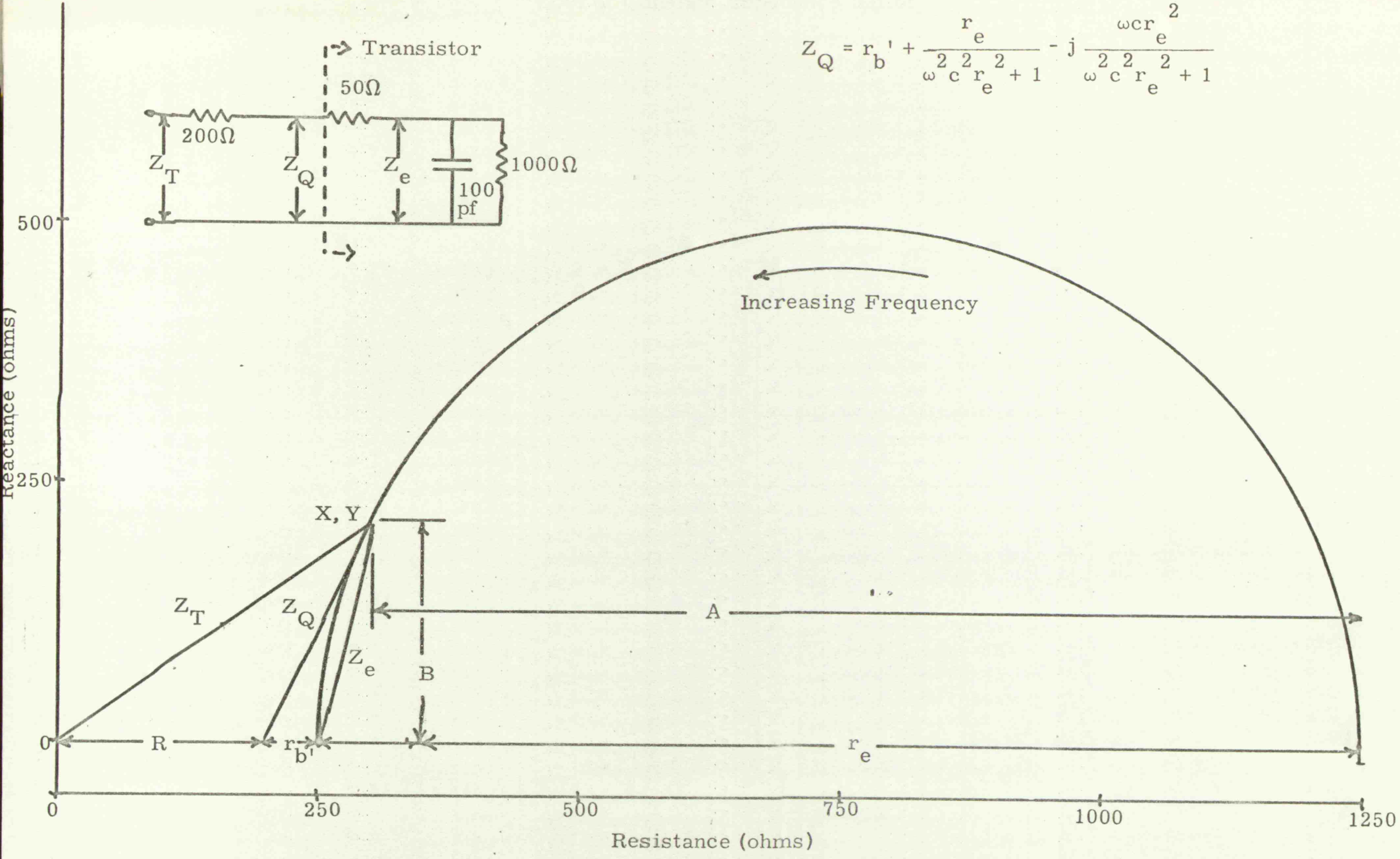


Figure B.4

Loci of Constant Impedance Ratios

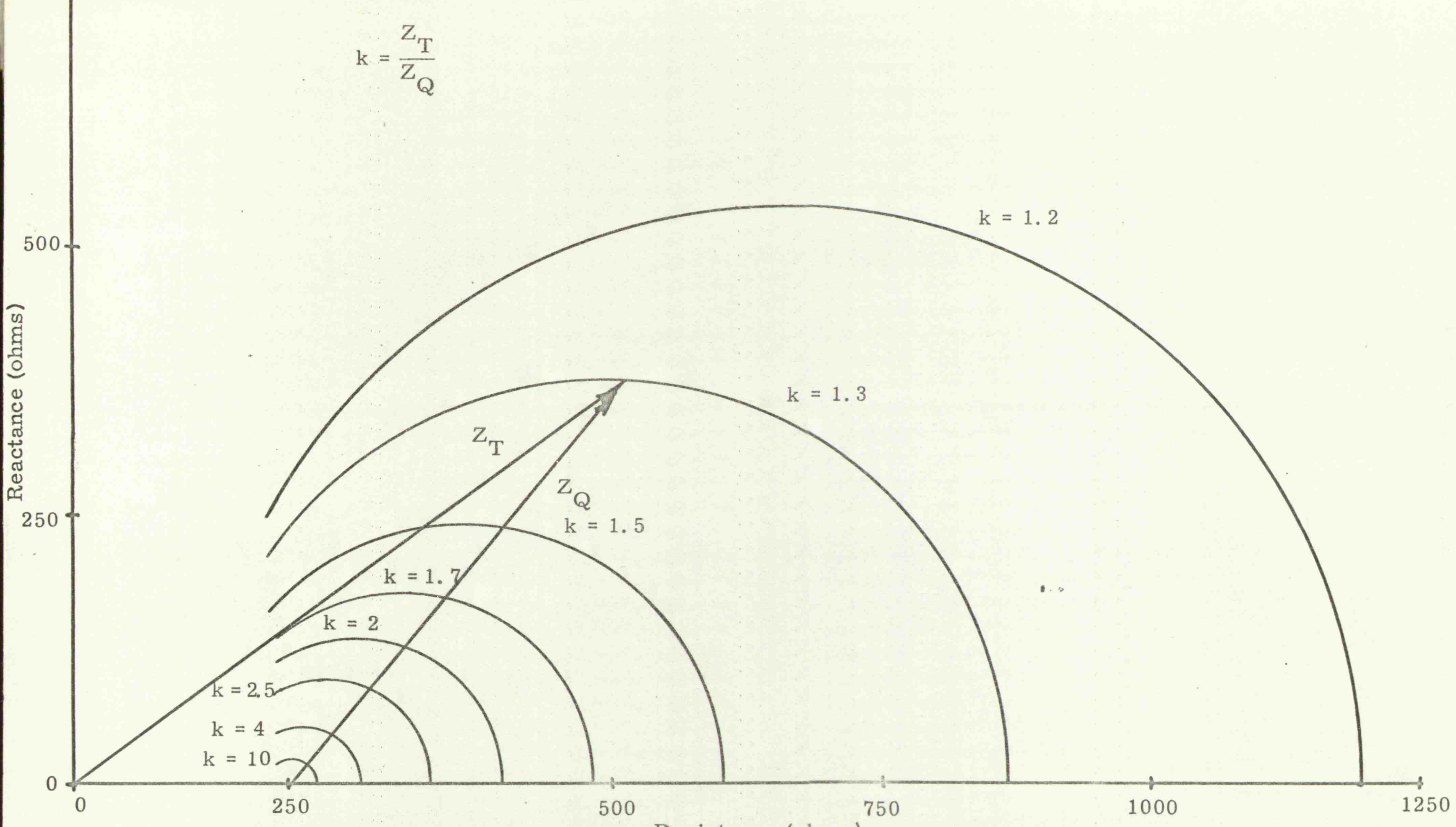


Figure B. 5

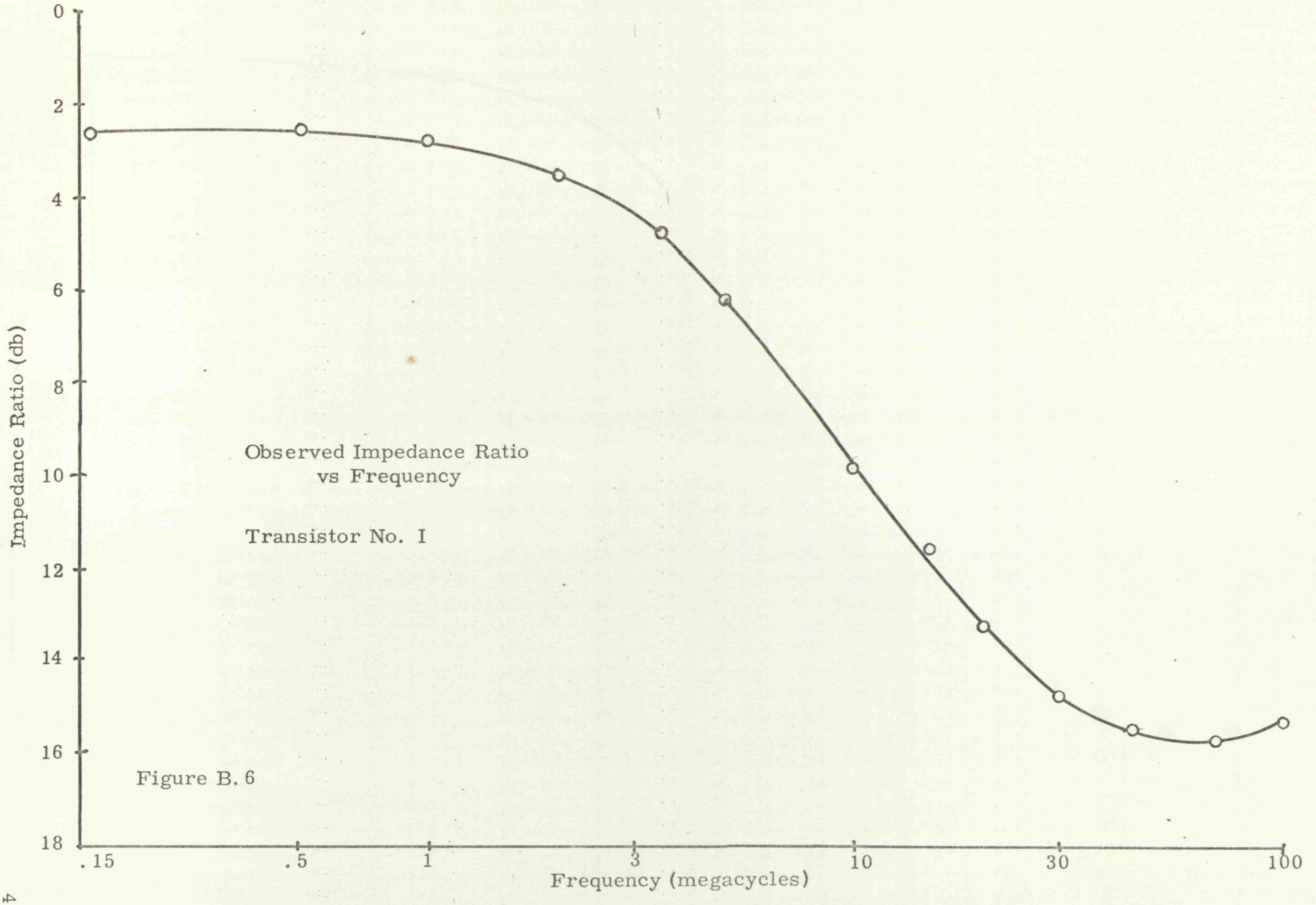
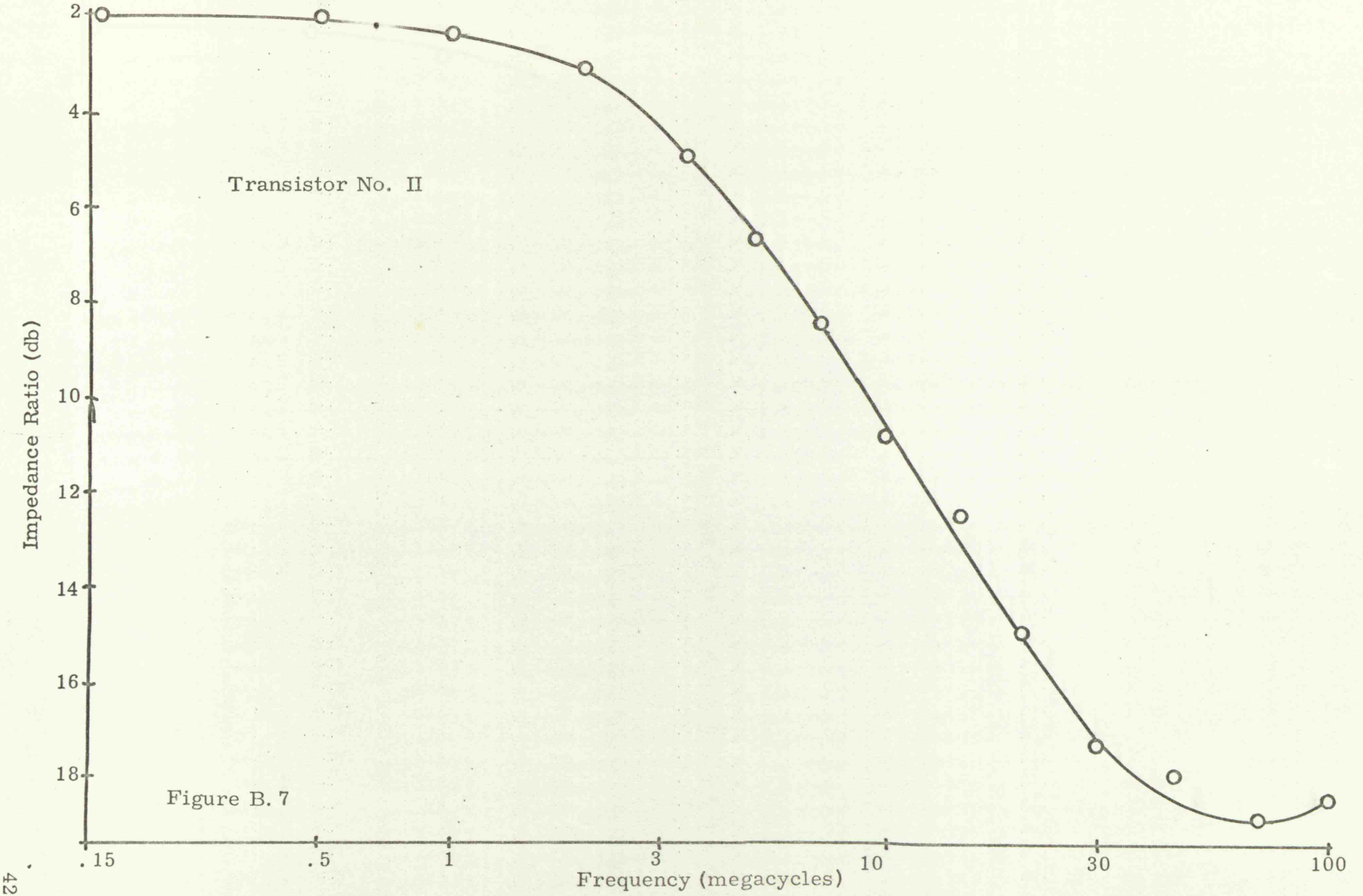

Impedance Ratio (db)
0
2
4
6
8
10
12
14
16
18
.15
.5
1
3
10
30
100
Frequency (megacycles)
Observed Impedance Ratio
vs Frequency
Transistor No. I

Figure B. 6



Transistor No. II
Impedance Ratio (db)
2
4
6
8
10
12
14
16
18
.15
.5
1
3
10
30
100
Frequency (megacycles)

Figure B. 7

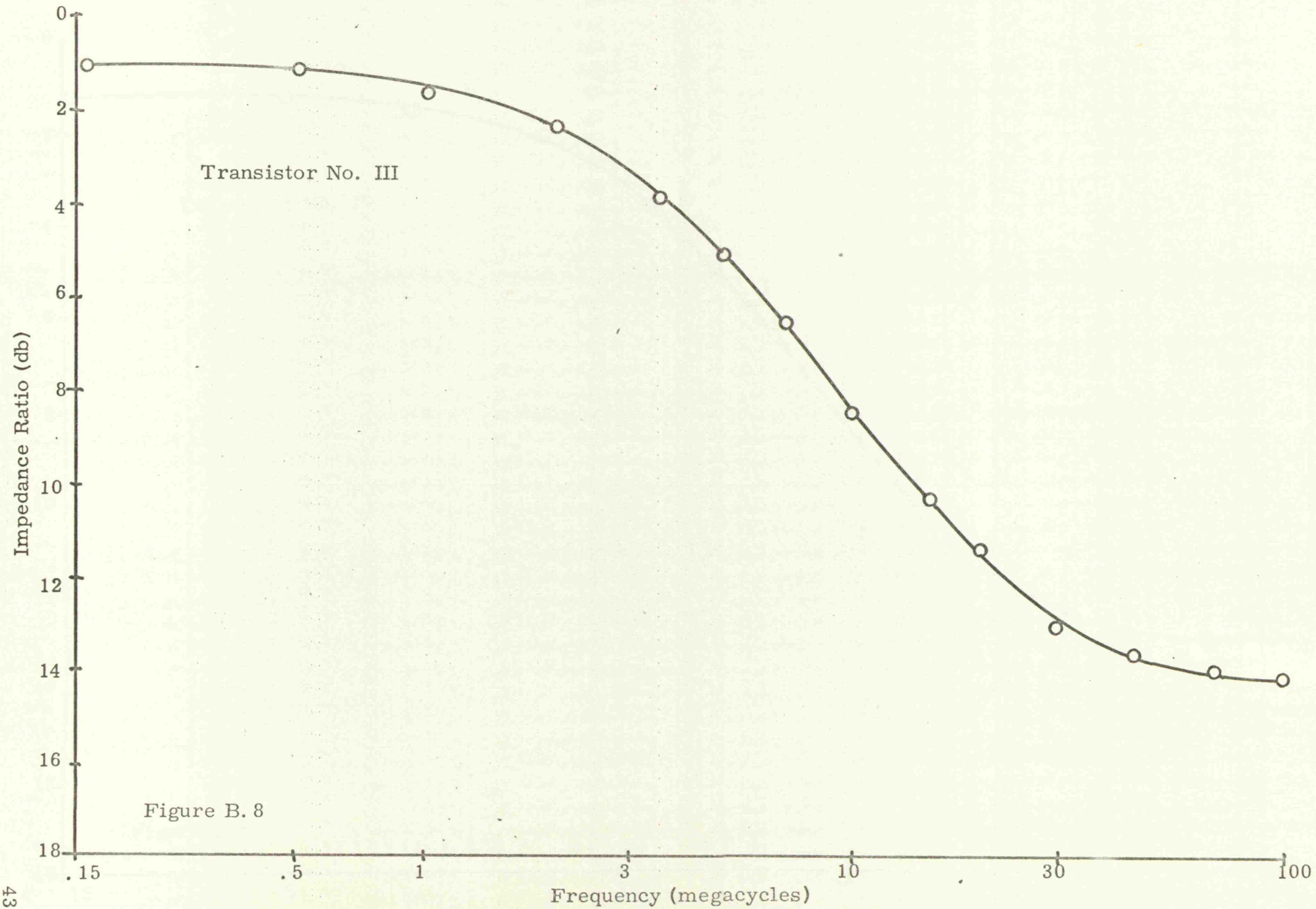

Transistor No. III
Impedance Ratio (db)
0
2
4
6
8
10
12
14
16
18
.15
.5
1
3
10
30
100
Frequency (megacycles)

Figure B. 8

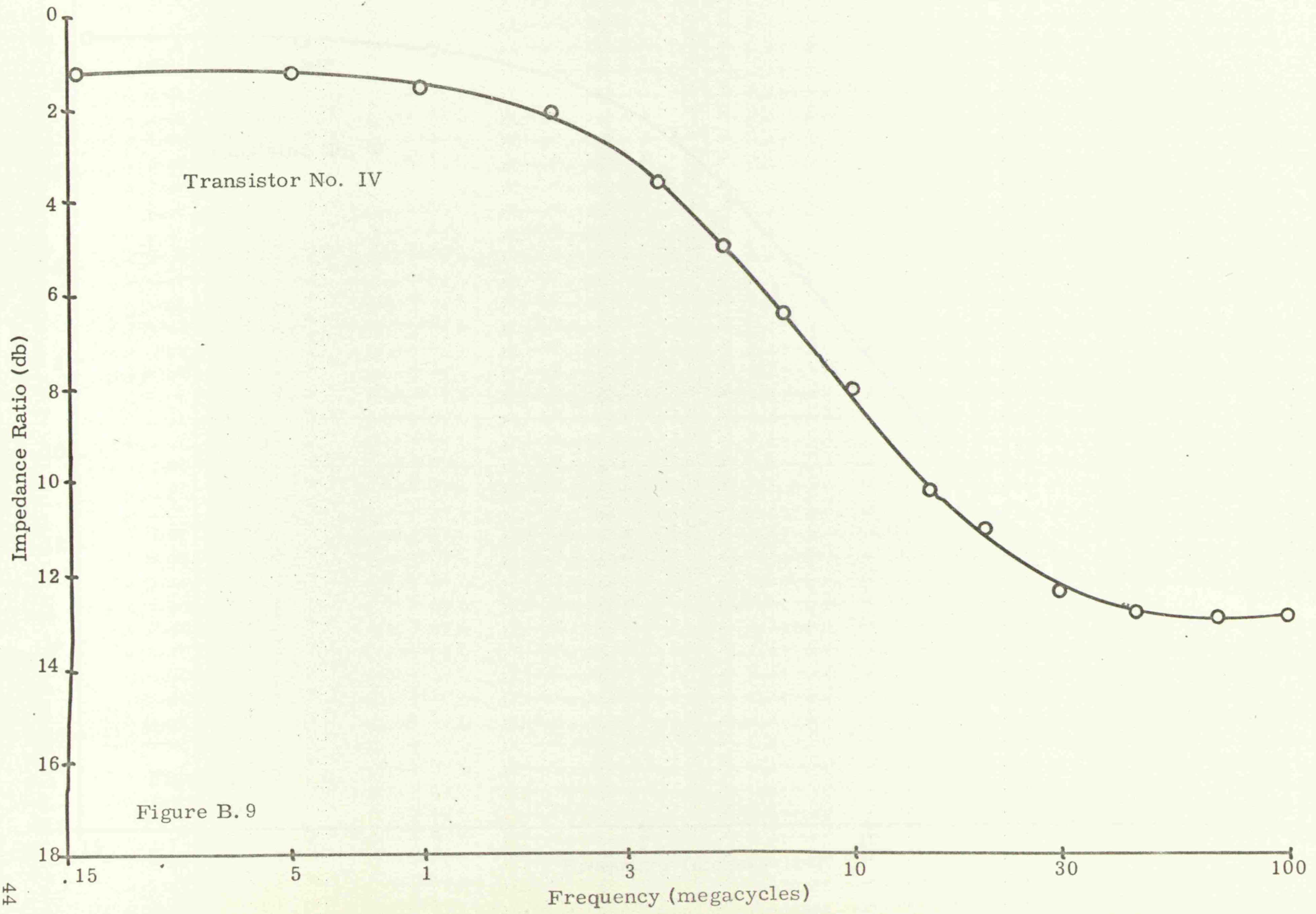

Transistor No. IV
Impedance Ratio (db)
0
2
4
6
8
10
12
14
16
18
.15
5
1
3
10
30
100
Frequency (megacycles)

Figure B. 9

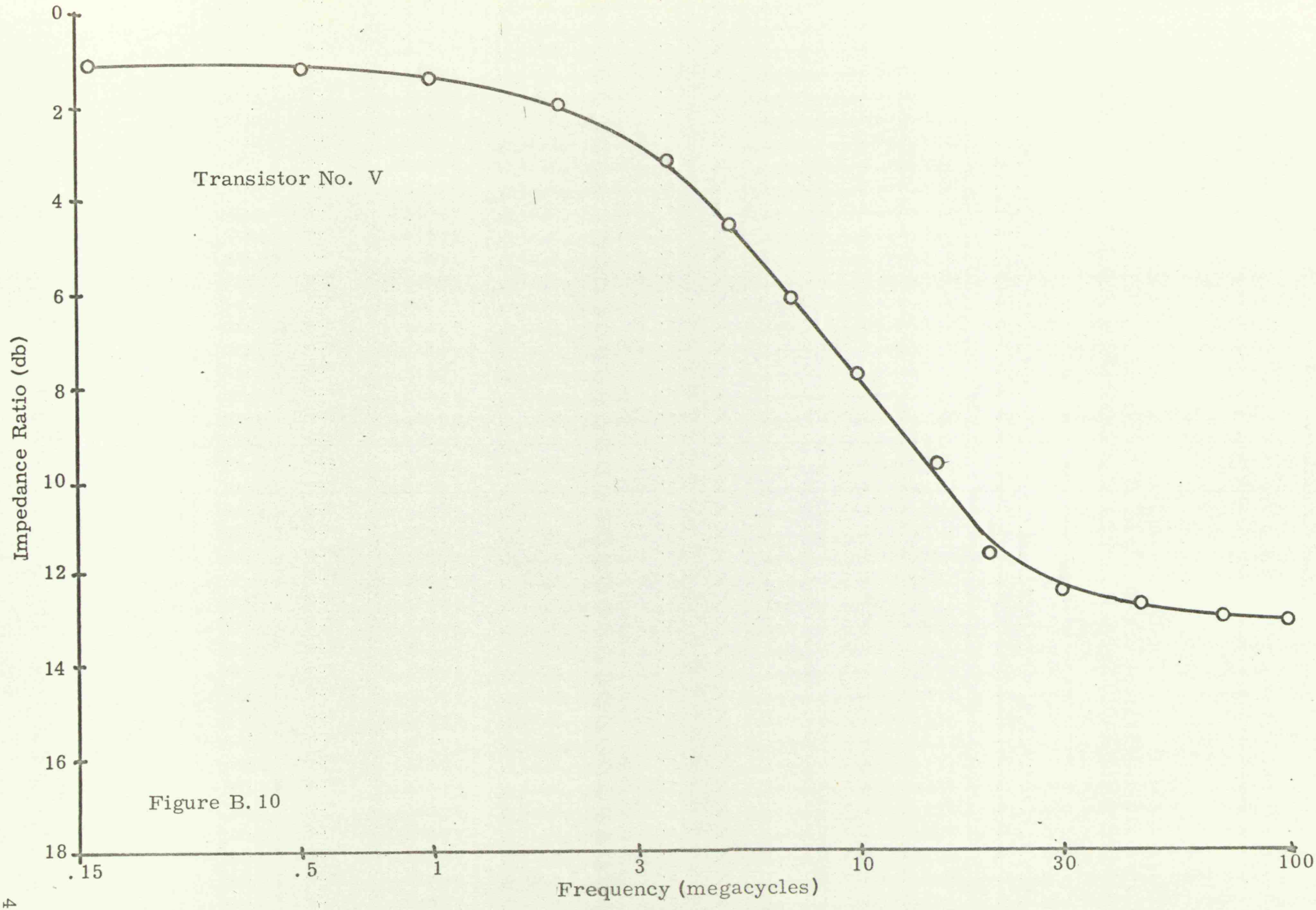

Transistor No. V
Impedance Ratio (db)
0
2
4
6
8
10
12
14
16
18
.15
.5
1
3
10
30
100
Frequency (megacycles)

Figure B. 10

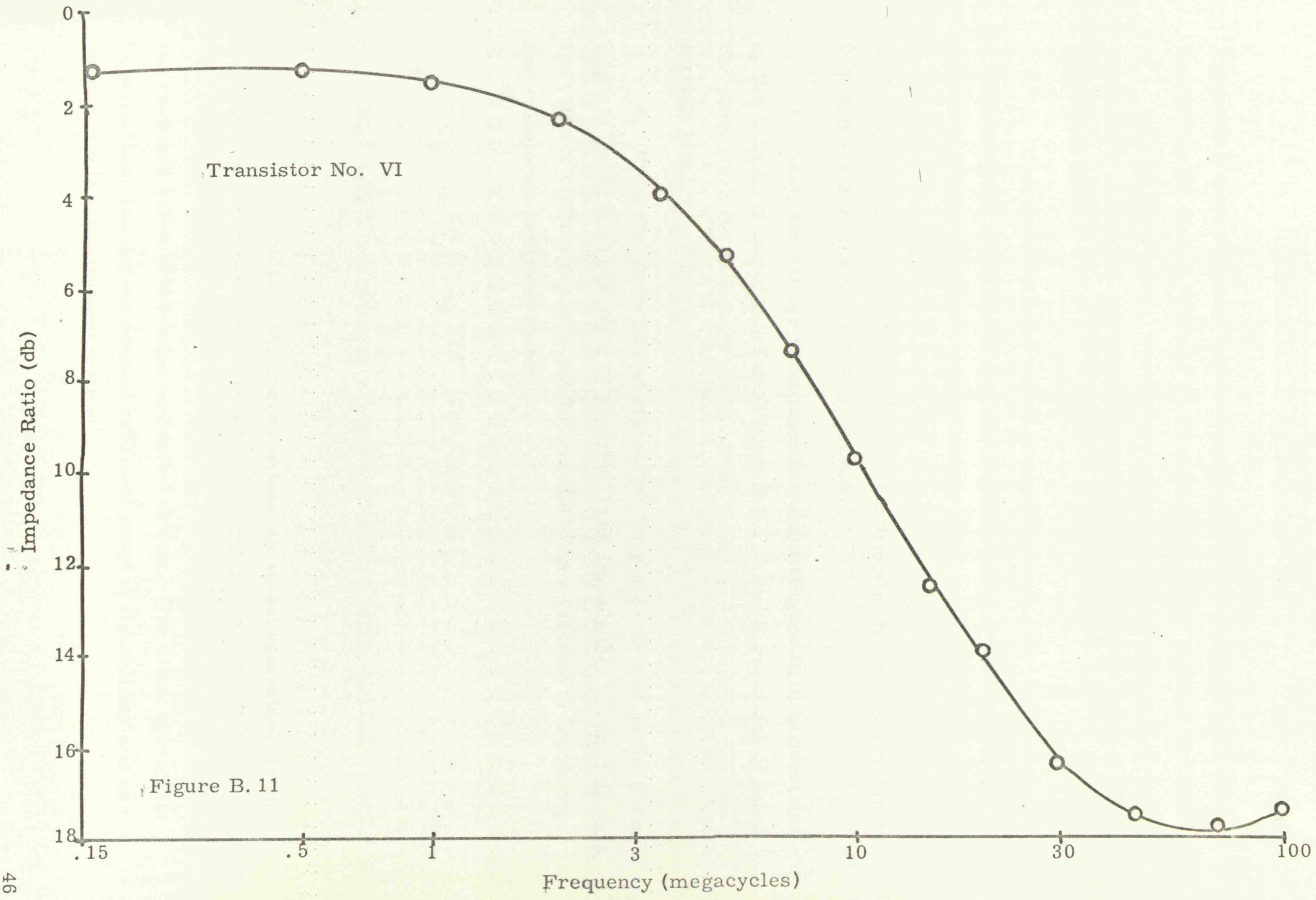

Transistor No. VI
Impedance Ratio (db)
0
2
4
6
8
10
12
14
16
18
.15
.5
1
3
10
30
100
Frequency (megacycles)

Figure B. 11

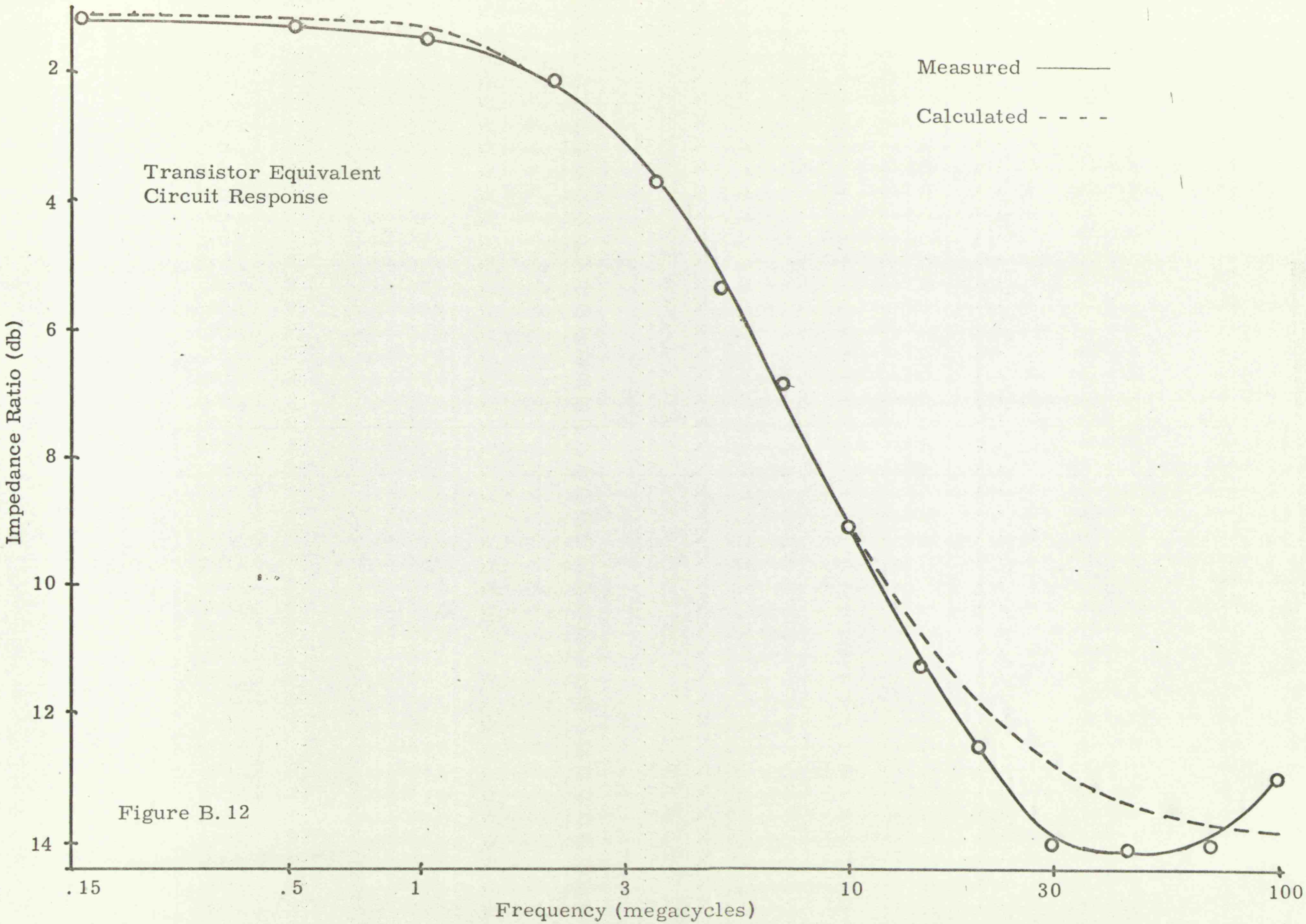

Measured
Calculated
Transistor Equivalent
Circuit Response
Impedance Ratio (db)
2
4
6
8
10
12
14
.15
.5
1
3
10
30
100
Frequency (megacycles)

Figure B. 12

It will be noticed that at frequencies above 100 megacyles, or so, the impedance begins to increase (see Figures B. 6 through B. 12). This was assumed to be due to the inductance of the transistor lead-in wires. On this assumption, a similar impedance response curve was run on small loops of wire which were approximately the same length as the transistor leads. As seen in Figure B. 13, the 3 db point calculation resulted in a measured inductance of about . 1 microhenry.

Other measurements included the base bias current which was indicated by a 20 microampere Weston meter, and the collector current which was monitored by a 1 milliampere Weston panel meter. The collector voltage supply was read on a 1 milliampere movement, 50 volt, sealed military meter.

Derivation of Equation for Loci of Constant Impedance Ratio Curves

Let

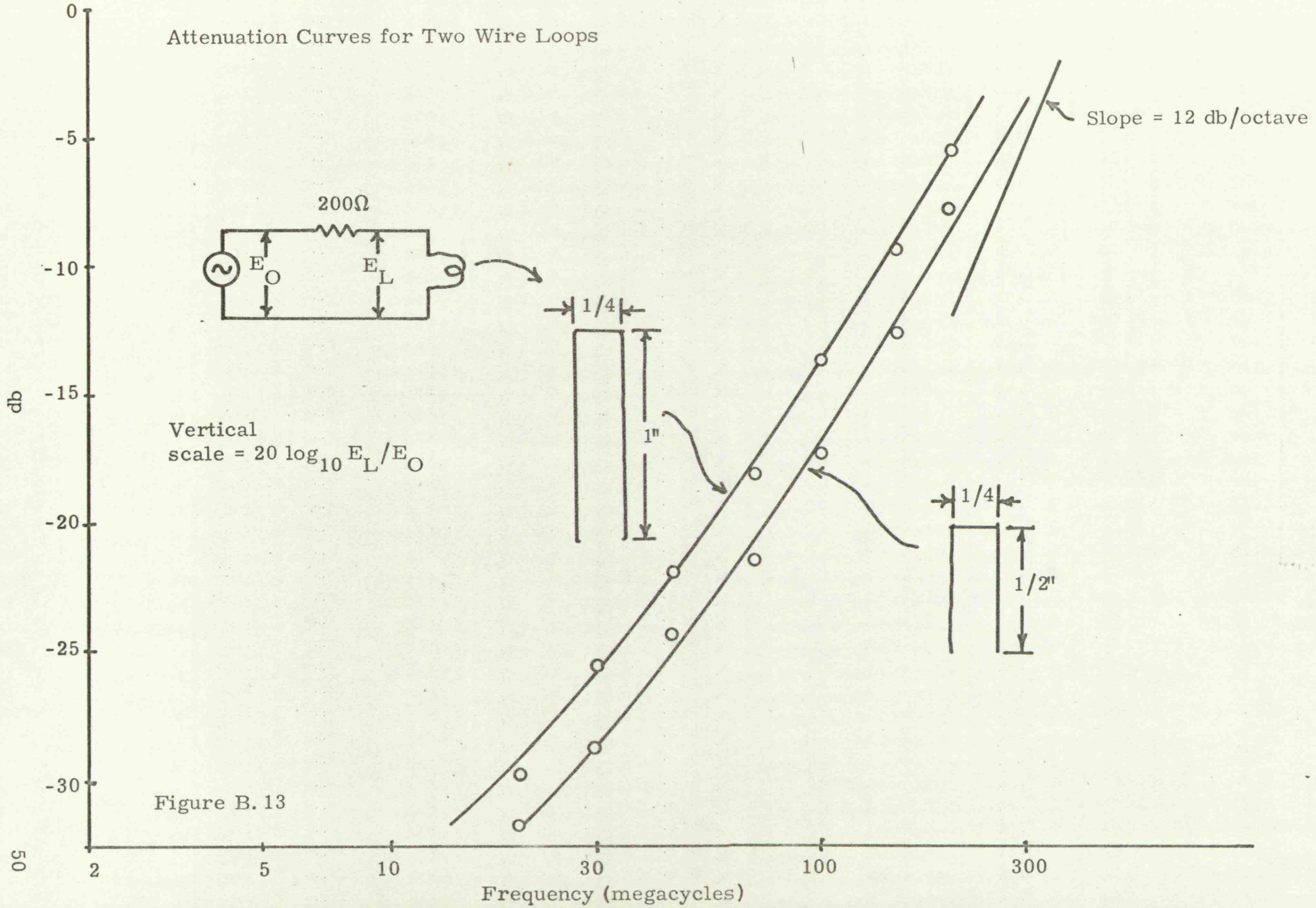
$$\frac{Z_T}{Z_Q} = \frac{\sqrt{X^2 + Y^2}}{\sqrt{(X - R)^2 + Y^2}} \quad \text{(see Figure B. 5)}$$

$$k^2 (X - R)^2 + k^2 Y^2 = X^2 + Y^2$$

$$k^2 X^2 - 2k^2 RX + k^2 R + k^2 Y^2 = X^2 + Y^2$$

$$(k^2 - 1) X^2 - 2k^2 RX + k^2 R^2 + (k^2 - 1) Y^2 = 0$$

$$X^2 - \frac{2k^2}{(k^2 - 1)} RX - \frac{k^2}{(k^2 - 1)} R^2 + Y^2 = 0$$



Attenuation Curves for Two Wire Loops
db
0
-5
-10
-15
-20
-25
-30
200Ω
E_O
E_L
1/4
1"
1/4
1/2"
Slope = 12 db/octave
Vertical
scale = 20 $\log_{10} E_L/E_O$
2
5
10
30
100
300
Frequency (megacycles)

Figure B. 13

$$X^2 - 2\frac{k^2}{(k^2-1)}RX + \left(\frac{k^2}{k^2-1}\right)^2 R^2 + Y^2 = \left(\frac{k^2}{k^2-1}\right)^2 R^2 - \left(\frac{k^2}{k^2-1}\right)R^2$$

$$\left(X - \frac{Rk^2}{k^2-1}\right)^2 + Y^2 = \frac{R^2k^2}{k^2-1}\left(\frac{k^2}{k^2-1} - 1\right) = \frac{R^2k^2}{\left(k^2-1\right)^2}$$

This is the equation of a family of circles, a different circle for each value of k.

The center of each circle is $Y = 0$, $X = \dfrac{R}{1 - 1/k^2}$.

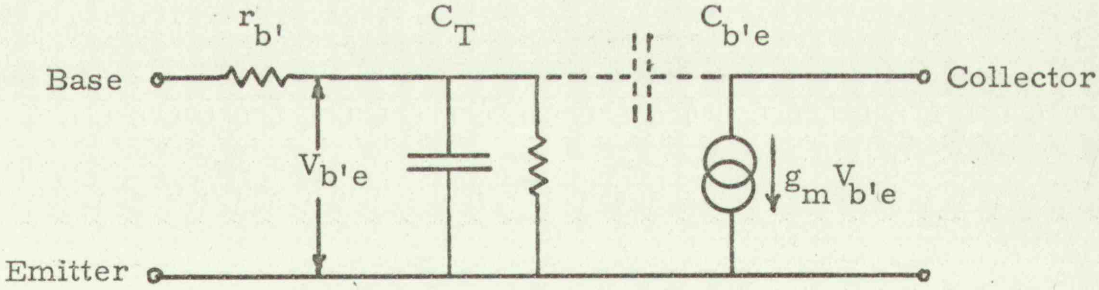
The radius of each is given by $\dfrac{R}{k - 1/k}$.

APPENDIX C

Having found a suitable measurement method, a check was made on the input parameters for several transistors of the same type. It had been suspected that wide manufacturing tolerances might be to blame for some of the difficulties encountered in the operation of a transistor distributed amplifier.

Three RCA 2N384 transistors were purchased in the fall of 1959 and labled I, II, and III. During the fall of 1960, three more were purchased of the same type: IV, V, and VI.

The following transistor input parameters are those of the "unilateral" equivalent circuit, repeated here in Figure C. 1.



$$C_T = C_e + (A + 1) C_{b'e}$$

Figure C. 1

The data shown in Table C. 1 was obtained by the methods covered in the previous section and are all taken at a collector current of 1 milliampere, a collector supply voltage of 20 volts, and a collector load resistance of 1000 ohms. The base bias current was adjusted in each case to obtain the proper collector current. The last three columns refer to DC values. The very small voltage biases appearing at the base (calculated from the input resistance and current) should be noted. Any signal voltage which surpasses

TABLE C. 1

Transistor	DC β	$r_{b'}$ ohms	r_e ohms	C_T pfd	I_{bias} μamp	R_{in} ohms	E_{in} mv	Comments
I	20	39	541	224	50	580	29	
II	25	25	775	255	40	800	32	Noisy
III	72	50	1550	185	11	1600	18	
IV	50	58	1222	186	20	1280	26	
V	66	57	1550	181	6	1600	10	High leakage
VI	55	28	1310	211	15.5	1340	21	
Average	48	43	1150	204				
Mfg. spec.	60	50	1040	187				
Average percent deviation	20	14	10	9				
Maximum percent deviation	66	50	49	36				

these values may be distorted and any calculations based on such voltages are liable to be in error.

The next observation was of the range of collector currents of different transistors when they all had the same base bias voltage. (See Table C. 2.)

The variation shown in Table C. 3 concerns the effect that changes in collector currents have upon the three input parameters r_b', r_e, and C_T. Note here how these important transistor parameters all improve with decreasing I_c in such a manner as to increase the Q of the transistor input reactance and to raise the frequency at which this maximum Q occurs. (See Chapters III and VI).

Min[illegible]
[illegible]
deviation [illegible] [illegible] [illegible] [illegible] .15

these values [illegible] and any calculations based on such voltages are liable to be in error.

The [illegible] range of collector currents of [illegible] [illegible] the same base bias voltage. (See Table C.2.)

The variation shown in Table C.3 concerns the effect that changes in collector currents have upon the three input parameters r_b, r_e, and C_{te}. Note here how these important transistor parameters all improve with [illegible] I_c [illegible] the Q of the transistor input [illegible] and to raise the frequency at which the maximum Q occurs (see Chapters III and V).

TABLE C. 2

Base volts	.22	.24	.25	Volts
Transistor				
I	.29	.67	1.37	Milliamperes
II	.49	.98	2.16	Milliamperes
III	.61	1.10	2.43	Milliamperes
IV	.274	.55	1.23	Milliamperes
V	.274	.55	1.25	Milliamperes
VI	.235	.51	1.12	Milliamperes
Average	.36	.72	1.16	Milliamperes
Maximum deviation	70	53	52	Percent

The last Table (C. 4) shows the variation in C_T as the collector load resistance is changed. The effect here is due to the change in voltage gain as the load impedance varies. As the gain changes, the Miller capacitance appearing in shunt with the emitter capacitance also changes (see Chapter III). At zero load resistance (and zero gain), the Miller effect should be zero and the residual capacitance would be nearly all due to the emitter capacitance. Subtracting out the manufacturers value for $C_{b'e}$, we get this variation for the various transistors: 135, 151, 101, 104, 140 pfd average 123, manufacturers stated value is 90, average error +37 percent, maximum deviation -67 percent.

It was found that the input resistances r_b' and r_e did not change with changes in load resistance due to the very low Miller conductance. No data was taken for this reason.

One final variation of concern was whether or not the emitter capacity C_e was constant with frequency. It was constant within the limits of the measurement method for all of the transistors tested except one (No. III).

TABLE C. 3

Effect of Collector Current

I_c (ma)	Min	.25	.5	1	2	
Transistor						
I	30	31.5	34	37	40	Base resistance (ohms)
II	19	20	22.5	24	25.5	
III	42	42	46	48	50	
IV	50	50	53	58	58	
V	45	50	53	56	58	
VI	22.5	24	26	27	30	
I	8000	1600	1000	540	300	Emitter resistance (ohms)
II	8000	2300	1350	800	475	
III	8000	4000	2300	1600	750	
IV	8000	3200	1600	1100	740	
V	8000	3200	2300	1400	830	
VI	8000	3200	1800	1200	870	
I	69	114	150	220	440	Total shunt capacity C_T (pfd)
II	76	127	159	228	360	
III	63	80	110	165	265	
IV	53	83	110	187	380	
V	74	105	124	170	400	
VI	96	122	159	215	350	

TABLE C.4

The Variation of Total Shunt Input Capacity With Changes in Collector Load Resistance

Load (ohms)	0	.47k	1k	3k	10k	
Transistor						
I	137	162	220	284	400	pfd
II	153	177	230	310	935	pfd
III	103	124	167	218	306	pfd
IV	109	135	187	227	318	pfd
V	106	130	169	210	290	pfd
VI	142	164	181	212	306	pfd

Going back now to the variation of input impedance with frequency, Figures C. 2 through C. 7 show the variation of the magnitude and phase of the input impedance for each transistor. This data was taken directly from the individual transistor impedance plots similar to Figure B. 4. To give an idea of the variation of Q with frequency, note that an angle of 63. 5 degrees corresponds to a Q of two.

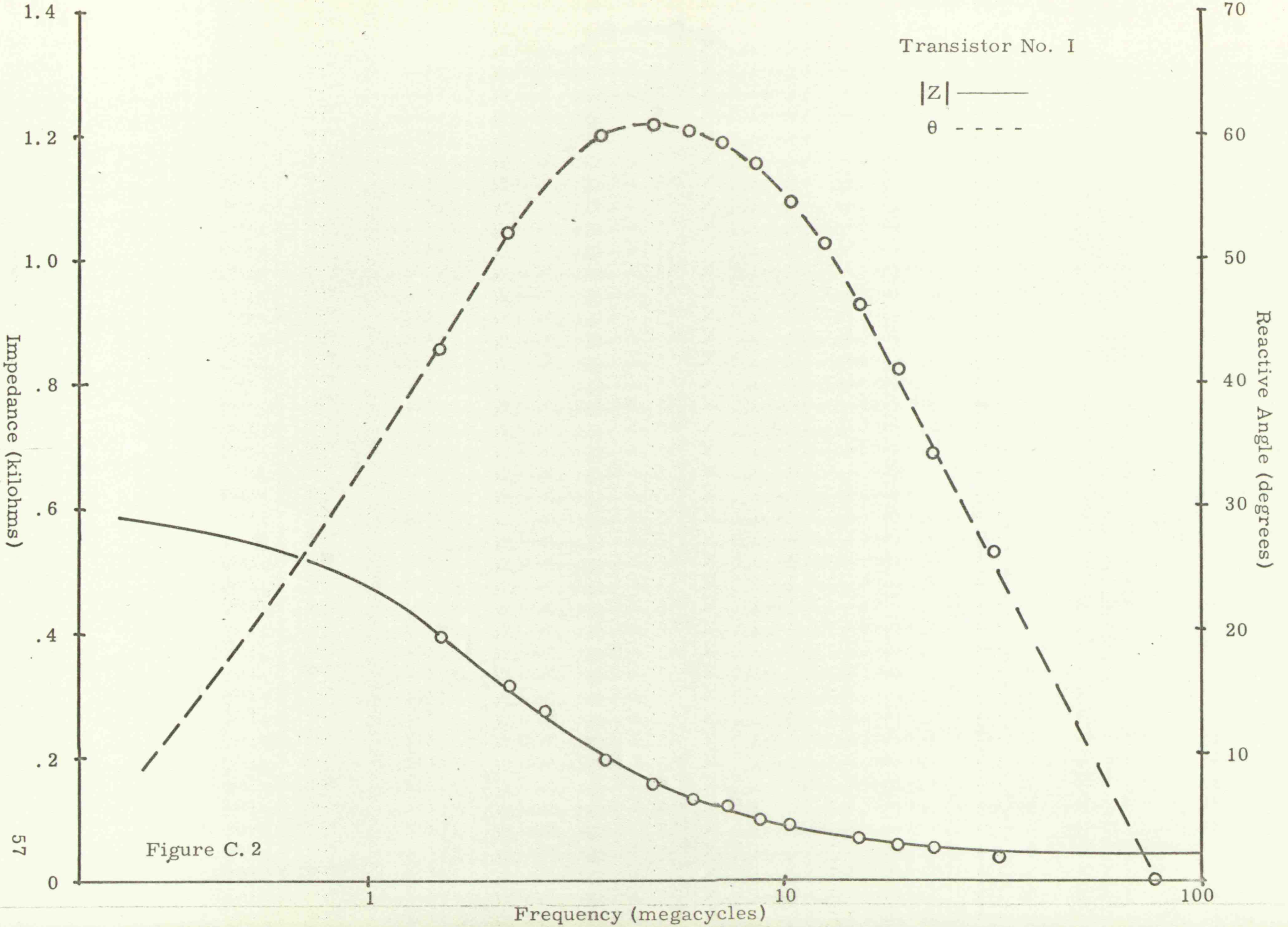

Transistor No. I
|Z|
θ
Impedance (kilohms)
Reactive Angle (degrees)
Frequency (megacycles)
1.4
1.2
1.0
.8
.6
.4
.2
0
70
60
50
40
30
20
10
1
10
100

Figure C. 2

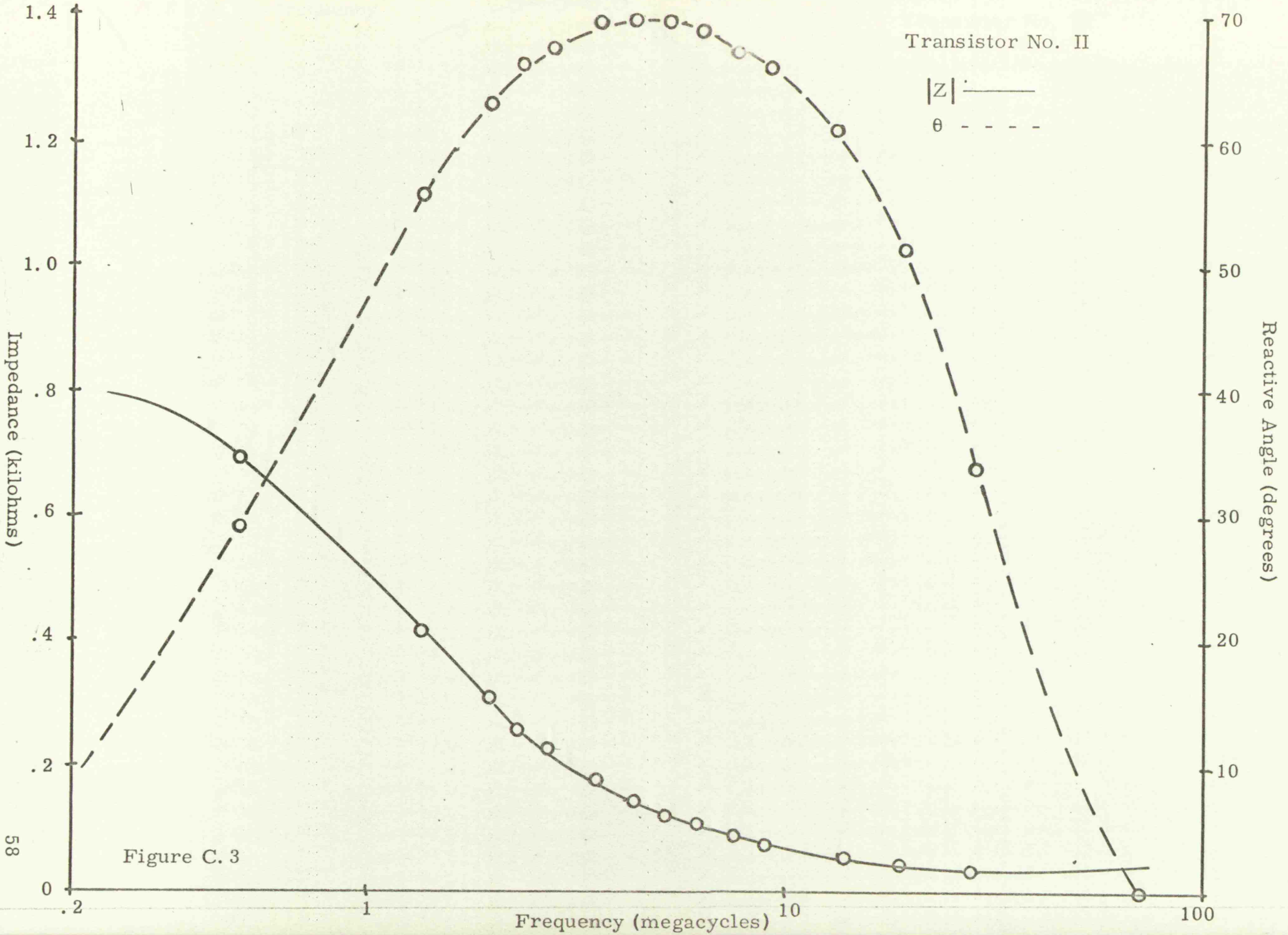
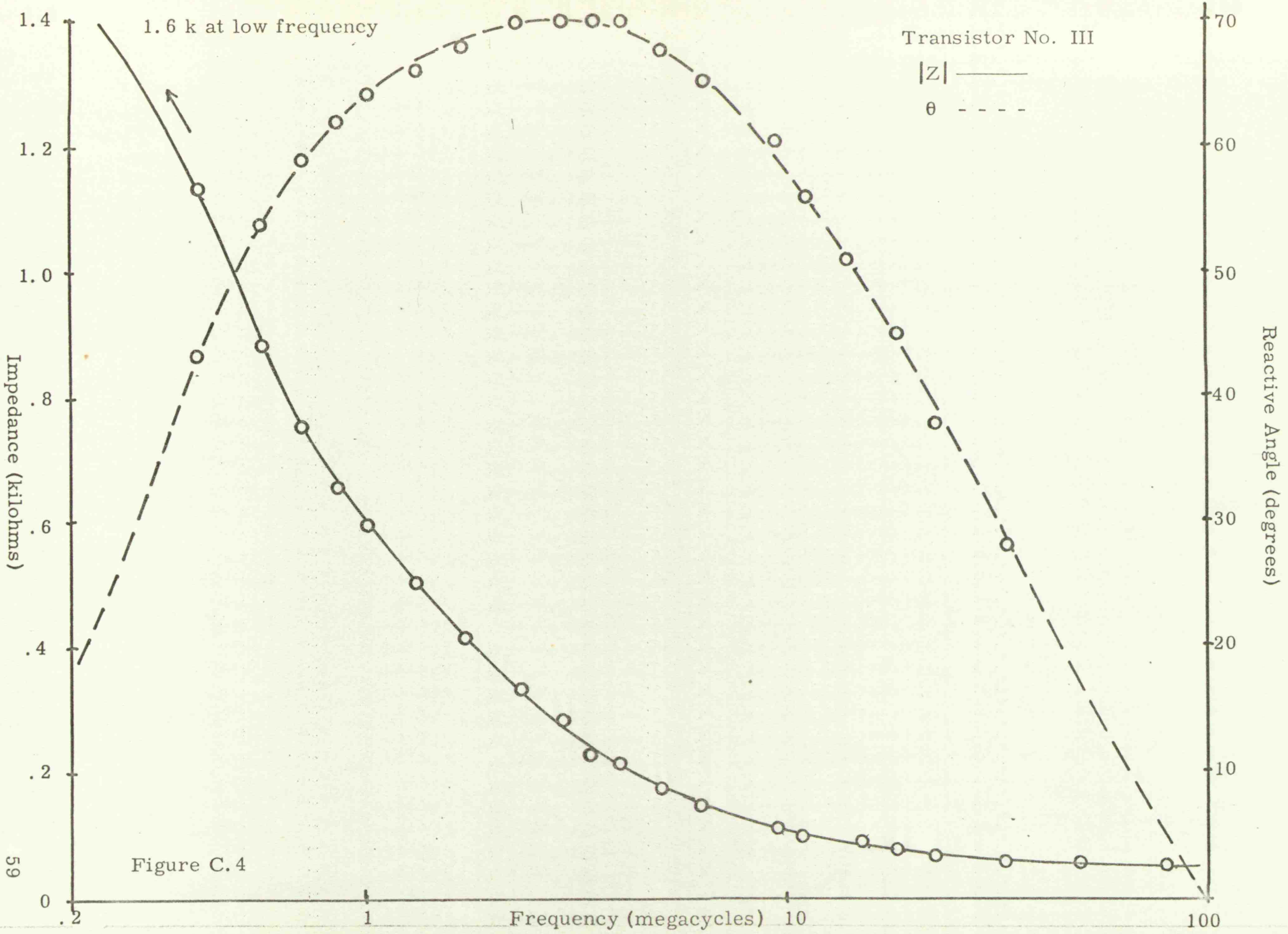

Transistor No. II
|Z| ———
θ - - - -
Impedance (kilohms)
1.4
1.2
1.0
.8
.6
.4
.2
0
Reactive Angle (degrees)
70
60
50
40
30
20
10
Frequency (megacycles)
.2
1
10
100

Figure C. 3



1.6 k at low frequency
Transistor No. III
|Z| ———
θ - - - -
Impedance (kilohms)
Reactive Angle (degrees)
Frequency (megacycles)
1.4
1.2
1.0
.8
.6
.4
.2
0
70
60
50
40
30
20
10
.2
1
10
100

Figure C.4

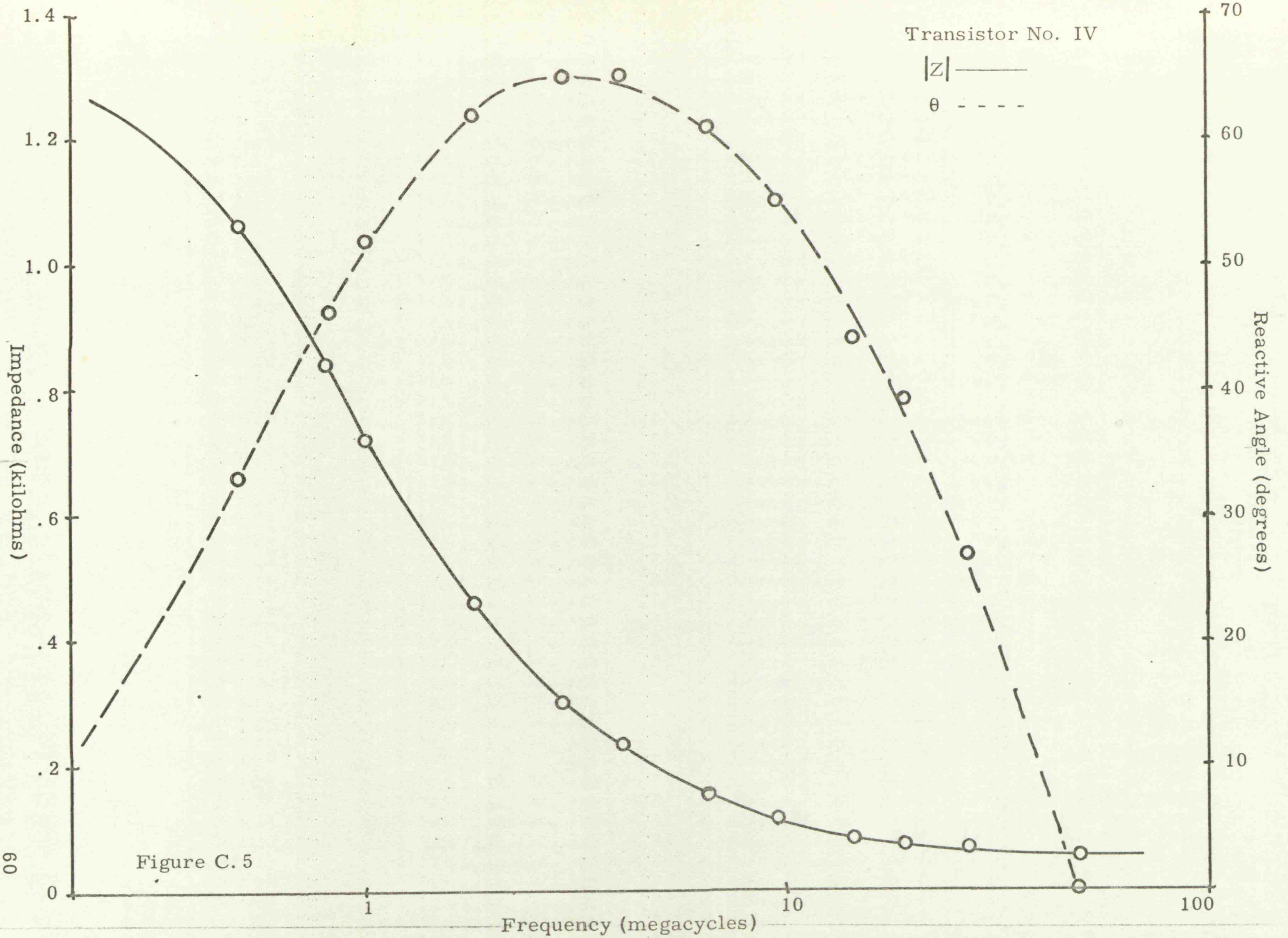
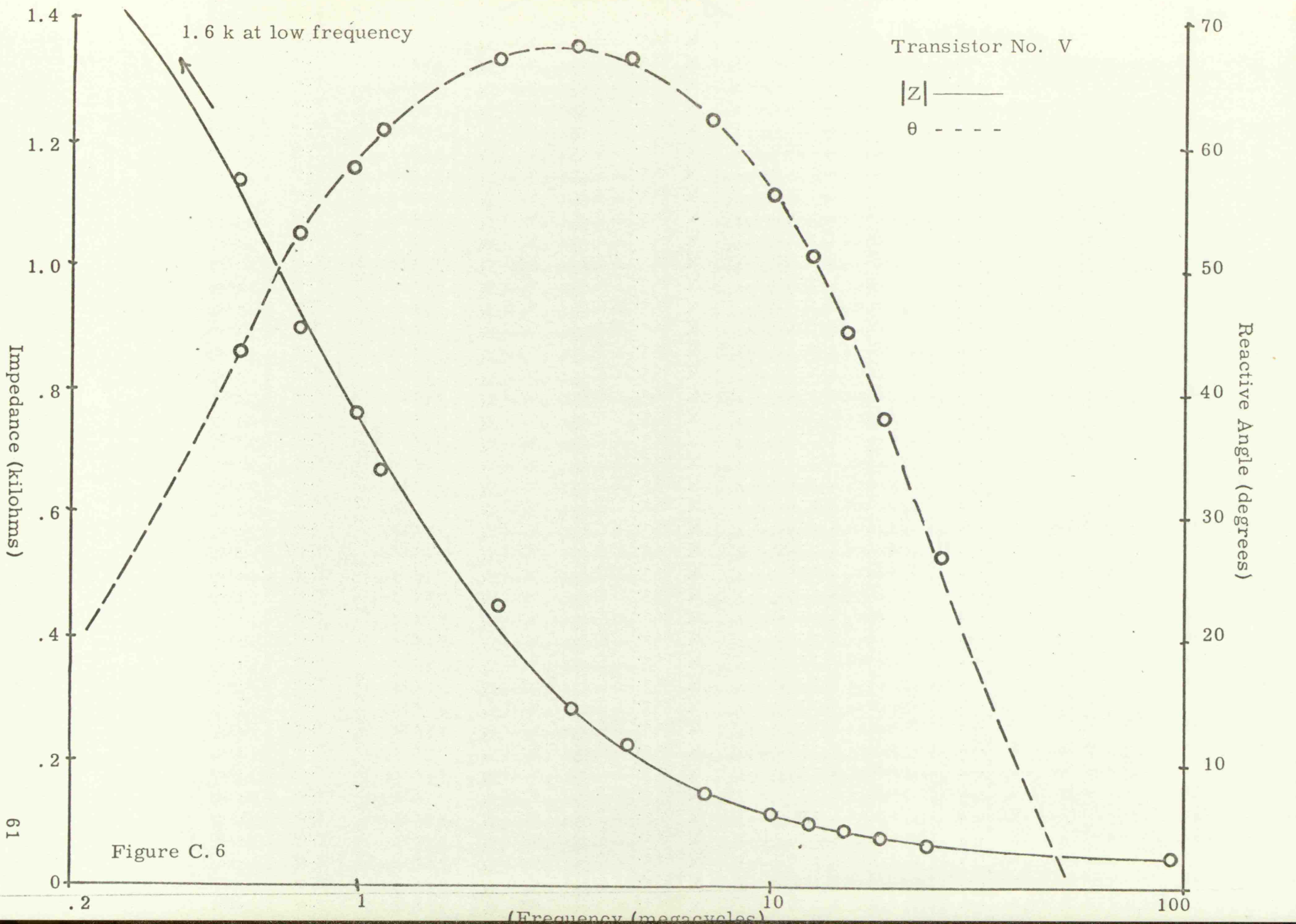
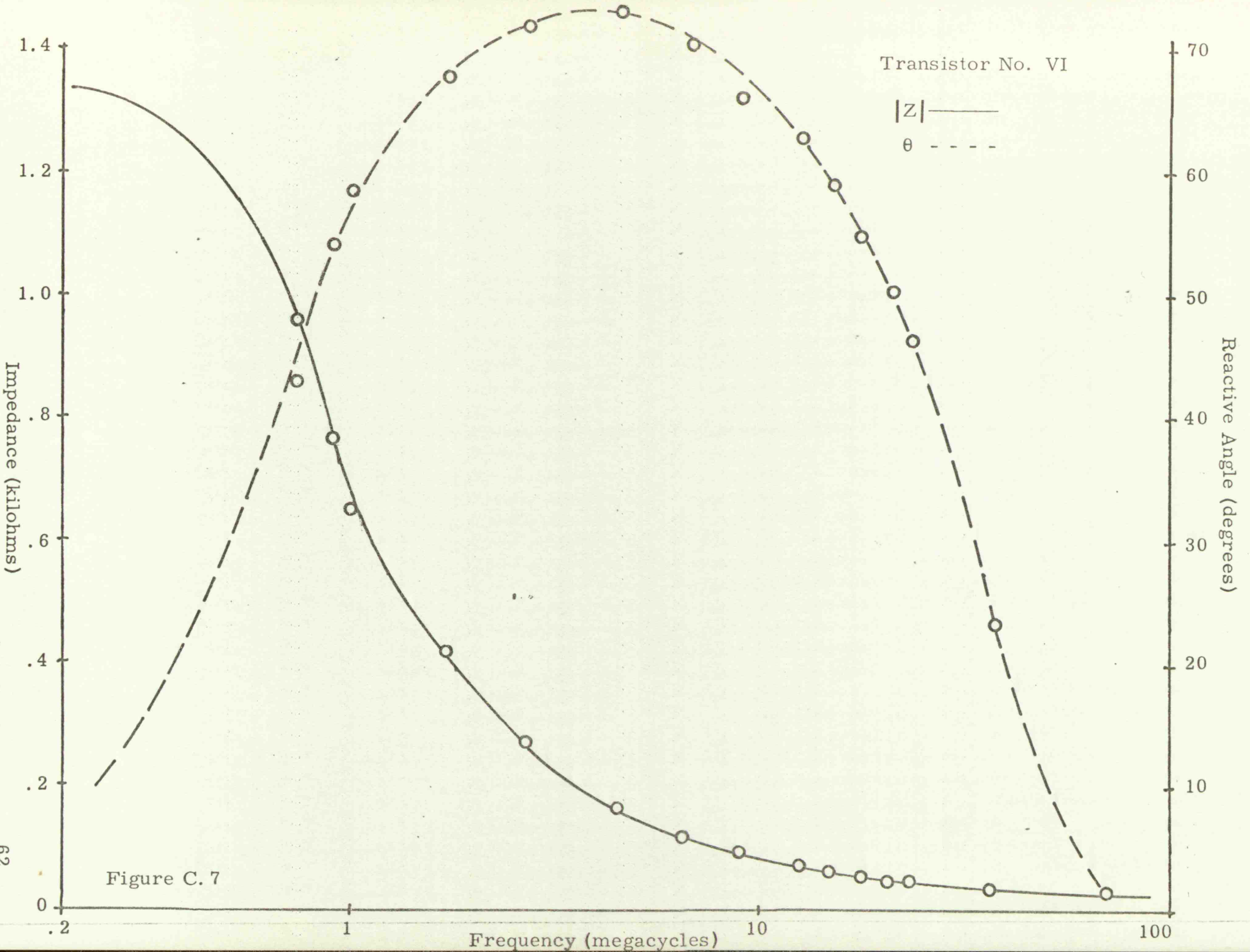

Transistor No. IV
|Z| ———
θ - - - -
Impedance (kilohms)
Reactive Angle (degrees)
Frequency (megacycles)
1.4
1.2
1.0
.8
.6
.4
.2
0
70
60
50
40
30
20
10
1
10
100

Figure C. 5


1.4
1.2
1.0
.8
.6
.4
.2
0
Impedance (kilohms)
1. 6 k at low frequency
Transistor No. V
|Z| ———
θ - - - -
70
60
50
40
30
20
10
Reactive Angle (degrees)
.2
1
10
100
(Frequency (megacycles)
Figure C. 6



Transistor No. VI
|Z|
θ
Impedance (kilohms)
1.4
1.2
1.0
.8
.6
.4
.2
0
Reactive Angle (degrees)
70
60
50
40
30
20
10
Frequency (megacycles)
.2
1
10
100

Figure C. 7

APPENDIX D

CONCLUSIONS TO APPENDIX

Low amplitude RF measurements of sufficient accuracy can be achieved by using relatively simple and inexpensive equipment. The graphical impedance solution simplifies and facilitates data reduction, allowing the measurement of these important transistor characteristics under many changes of external parameters.

As to the specific characteristics of the input to the transistor, there is a much greater deviation from published data than in the case for vacuum tubes. The variation of these characteristics under different circuit conditions may make the difference between whether or not these particular transistors can be used in a distributed amplifier.

BIBLIOGRAPHY

1. Beneteau, Paul J. and Blaser, Larry, "A 175 m.c. Distributed Amplifier using Silicon Mesa Transistors," Application Data, APP-1 Fairchild Semiconductor Corporation.

2. Ginzton, E. L., Hewlett, W. R., Jasberg, J. H., and Noe., J. D., "Distributed Amplification," Proc. IRE, Vol. 36, August 1948, pp 956-969.

3. Harper, Bill J., Transistor Distributed Amplifier, Technical Report EE-19, The University of New Mexico (Engineering Experiment Station) January 1959.

4. Horton, W. H., Jasberg, J. H., and Noe. J. D., "Distributed Amplifiers, Practical Considerations and Experimental Results." Proc. IRE, Vol. 38, July 1950, pp 748-752.

5. RCA Semiconductor Products, Radio Corporation of America, Somerville, New Jersey, Form No. SCD108B, June 1959.

6. Reference Data for Radio Engineers, International Telephone and Telegraph Corporation, New York, 1956, Fourth Edition.

7. Terman, F. E., Radio Engineers Handbook, McGraw-Hill, New York, 1943.