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Investigation into the use of high-efficiency switched-mode class E power amplifiers for high-dynamic range pulse-mode applications

Jesse Lai

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INVESTIGATION INTO THE USE OF HIGH-EFFICIENCY, SWITCHED-MODE CLASS E POWER AMPLIFIERS FOR HIGH-DYNAMIC RANGE, PULSE-MODE APPLICATIONS

BY

JESSE BOGART LAI

B.S., Electrical Engineering, University of Missouri-Rolla, 2002
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DISSERTATION

Submitted in Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY
ENGINEERING

The University of New Mexico
Albuquerque, New Mexico

DECEMBER, 2008
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ABSTRACT

In typical communication and radar systems, the transmitter is operated in either a continuous wave or a pulsed mode where the transmitter is periodically turned on for a portion of time. These systems commonly use a power amplifier in the transmitter to raise the power level of the transmitted signal to a value sufficient to meet system sensitivity requirements. In high-dynamic range systems, the power amplifier pulse must turn off at a rate compatible with the system noise floor at the receive time. Some high-dynamic range systems are sensitive to signals greater than 120 dB below the transmit power level, and correlated energy that exists during the receive time can cause serious system consequences.
The Class E high-efficiency power amplifier is an attractive candidate for pulse-mode systems, but it is unknown if the pulse profile characteristics are compatible with the stringent requirements of these systems. It is shown that the Class E amplifier mode allows generating a high-isolation pulsed signal simply by pulsing the input radio frequency (RF) signal. The unique properties of the switched-mode amplifier cause it to be off when it is not driven.

A technique to characterize the pulse profile of an RF amplifier over a very wide dynamic range under fast-pulsing conditions is presented. A pulse modulated transmitter is used to drive a device under test with a phase coded signal coupled with a correlation technique that allows for an increased measurement range beyond standard techniques. A measurement receiver is described that samples points on the output pulse power profile and performs the necessary signal processing and coherent pulse integration, improving the detectability of low-power signals. A full measurement dynamic range of greater than 160 dB is achieved, extending the current state of the art in pulse profiling techniques. The pulse profiles of example Class E amplifiers are examined and compared to the results for the same amplifiers operating in a linear mode. It is discovered that the inherent trapping properties of the active device technology limit the usefulness of these specific amplifiers in a high-dynamic range pulsed system.
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1. INTRODUCTION AND BACKGROUND

The explosion in the demand for wireless communications systems in the last decade has spawned a great deal of research in the area of power amplifiers. The ubiquitous power amplifier is one of the most critical blocks used in any communications system including (but not limited to) cellular telephones, base station transceivers, global positioning systems (GPS), wireless LAN, radio frequency identification (RFID) interrogators, automobile collision warning and avoidance systems, satellite communications, electronic warfare (EW), weather radar, synthetic aperture radar (SAR), and phased array radar. The purpose of the power amplifier is very clear: increase the signal power to a level that meets the system link margin requirements. However, the actual design and implementation of the essential power amplifier can be fraught with many complications related to stability, bandwidth, gain flatness, power consumption, thermal management, device sensitivity to circuit and environmental variations, reliability, and cost. In the end, a delicate balancing act must be performed to trade-off all of these requirements in a successful system.

In mobile and commercial applications, the power requirements are lower, typically in the range of 0.1 to 1 W. Cellular base stations can have output power requirements in the range of tens to hundreds of watts. One very critical parameter in the design of a power amplifier is its efficiency. Amplifier efficiency is commonly measured in one of two ways: either as drain/collector efficiency, that measures the ratio of output power to DC power, or power added efficiency (PAE), which also accounts for the input
power delivered to the device. PAE becomes more important for lower gain amplifiers (such as power amplifiers) because the input power is larger relative to the output power.

Amplifier PAE is an important parameter because it affects device reliability and drives system cooling requirements. In semiconductor devices, the operating junction temperature is one of the main accelerators to device failure. This relationship follows the well-known Arrhenius equation, where device lifetime is inversely proportional to operating temperature [1]. Therefore, reducing the junction temperature, even by a small amount, translates to a longer mean time to failure (MTTF), which means longer system lifetimes in the field or less warranty repairs. A reduced cooling requirement is a major factor in space applications where size and weight are system drivers. A higher efficiency amplifier experiences less power dissipated as heat, thus a smaller heat sink is required. Efficiency also plays a major role in mobile communications systems that require battery operation. The power amplifier typically consumes a large portion of the power budget in a system. Therefore, a more efficient amplifier can allow for longer battery life or increased capabilities in the system since power can be utilized for other applications.

The interest in high-efficiency amplifiers increased greatly with the first publications on a new class of switched-mode amplifier, dubbed Class E. The Sokals published the first work on switched-mode amplifiers in 1975 [2]-[3]. The switched-mode amplifier is a significant departure from the traditional linear amplifier school of thought where the active device is considered a current source [4]. Instead, in a Class E amplifier, the active device is ideally switched between two binary states: "on" and "off". The input radio frequency (RF) signal effectively changes the switch between its two
states at the period of the input signal. The ideal Class E amplifier experiences high voltage and current waveforms at the device, but not simultaneously in time, as shown in Figure 1.1. Therefore, the theoretical collector/drain efficiency is 100 %, which is an advantage over Class A or B, where the maximum theoretical efficiencies are 50 % and 78 % respectively [4]. Class C also offers a high theoretical efficiency, but at the expense of maximum output power.

The application of Class E principles have previously been limited to amplifiers at lower frequencies in the megahertz range due to active device and package parasitics [5]-[15]. Class E techniques have also been applied to DC/DC power converters that also operate at lower switch frequencies [16]-[23]. It is only recently that Class E principles have been applied to RF and microwave amplifier design, made possible by the high-performance active devices available today in nanoscale CMOS on silicon (Si), gallium arsenide (GaAs), silicon germanium (SiGe), silicon carbide (SiC), and gallium nitride (GaN) [24]-[48].

![Figure 1.1. Ideal class E voltage and current relationship.](image-url)
In typical communication systems, the transmitter is operated in either a continuous wave (CW) or a pulsed mode where the transmitter is periodically turned on for a duration of time. The transmitters that are operated in a pulsed mode typically operate with pulse repetition frequencies (PRF) ranging from hertz to hundreds of kilohertz, while some transmitters even operate into the megahertz range. A slower PRF translates into a longer pulse repetition interval (PRI), or the time interval between successive pulses. The traditional communication system has a slower PRF with lower duty factors, thus there is a long time interval before the receiver is active after a transmit pulse [49]-[55]. In some high-performance communication systems, the system requirements drive the PRF to be in the megahertz range, and the amount of time between successive transmit and receive gates can be measured in nanoseconds, especially in systems with relatively high duty factors. Some systems are reported to utilize fast pulsing, but the duty factor is very low so that the amount of recovery time after each transmitter pulse is appreciable [55].

Class E amplifiers should offer a unique advantage in pulsed mode, similar to Class C operation, where the output RF waveform can be pulsed with a high on-to-off ratio simply by pulsing the input RF signal [55]. In principle, the Class E amplifier is biased at its pinch-off threshold level (for 50% duty cycle operation) and the input RF signal drives the active device into its "on" and "off" states at the period of the input signal. If the input RF signal is pulse modulated, then during the dead time of the input pulse, the Class E stage is effectively "off" and not providing any gain because the switch is DC biased in its "off" state. The pulse output from a Class E stage should follow the input pulse, which can allow for fast pulsing limited ultimately by the speed of the input
pulse. The ability for the output stage to be pulse modulated is important in some high-
dynamic range applications where the receiver is sensitive to signals at or below the
thermal noise floor [49]. If the output stage is biased on so that it is providing
amplification, the output power from the device will be greater than thermal noise by the
gain and noise figure of the stage, even if there is no input signal. This increase of noise
power poses a problem in highly sensitive systems that require the noise power to be at or
near thermal noise during the receive time.

Simple AM modulation and more complicated envelope restoration techniques for
Class E amplifiers have been investigated through the use of supply current
modulation [42], [43], [56]-[59], but an in depth study of pulse-mode operation has not
been performed to date. More importantly, the unique capability of very fast pulse-mode
operation (megahertz PRF) is not considered in the literature to any degree. The ease of
pulsing can be a great advantage because modulating a high-power output stage is
typically much more difficult than modulating a lower power driver stage due to the
amount of current switched, stability issues, etc. A separate driver circuit is typically
required to pulse modulate linear mode amplifiers. The additional circuitry and
integration complexity translates into higher overall amplifier costs and development
time.

Some high-dynamic range systems may be sensitive to signals more than 120 dB
below the transmit power level [60], [61]. In high-dynamic range systems, the power
amplifier pulse must turn off at a rate compatible with the minimum system sensitivity at
the receive time. If the rate of decay of the transmitted energy is not sufficiently high,
then undesired energy can remain in the system at the time the receiver turns on. In some
cases, residual transmit energy can exist in the output of the power amplifier stage for hundreds of nanoseconds, which can coincide with the receive time in high duty factor, fast pulse-mode systems. This residual correlated energy can cause serious system consequences, such as reduced operational range or a drastic increase in bit error rate (BER) due to the increased noise level. The problem is compounded further in single-port antenna systems where a circulator or diplexer is used. The transmit-to-receive isolation is typically less than the case where separate transmitter and receiver antennas are used. The reduced isolation exacerbates the problem by introducing even higher levels of unwanted energy into the receiver.

A technique for measuring amplifier pulse characteristics, such as the amplifier turn-off power behavior, does not currently exist for high-dynamic range systems. Let us consider a 50 Ω system that is sensitive to signals with correlated energy near the noise floor in a system with a bandwidth of 10 MHz. In this case, the system noise floor is at -104 dBm ($kTB = -174 \text{ dBm/Hz} + 70 \text{ dBHz}$). Let us also consider a moderate power application with an output power level of 1 to 10 W (30 to 40 dBm) at the output. Then the overall measurement dynamic range requirement is about 140 dB, at the best case, if signals below the noise are not considered. In some high-dynamic range systems, the receiver can distinguish signals that are 20 to 30 dB below thermal noise, thereby increasing the requirements for dynamic range by this amount. From a linear perspective, these high-dynamic range systems can distinguish signals that are one quadrillionth ($10^{-15}$) of their starting power level.
1.1 Traditional Power Measurement Problems

There are numerous techniques in the microwave world to measure the power of a signal. If the signal is continuous wave, then an average power meter can be used to very accurately measure power with a dynamic range of 50-80 dB for state-of-the-art commercial technologies. The ubiquitous spectrum analyzer is also capable of measuring the power of a CW signal with an even greater dynamic range (80-90 dB). Spectrum analyzers exist that are capable of measuring power over this complete range with acceptable uncertainty results, whereas in previous generations of spectrum analyzers, the power uncertainty increased greatly for signal levels much less than full scale range.

Adding pulse modulation to a signal increases the complexity of instrumentation used to measure the power of a signal. A peak power meter is commonly used to measure pulsed signals, and a dynamic range of 50-80 dB is achievable with commercial state-of-the-art equipment [62], [63]. However, the video bandwidth in these systems is limited so that the capability of measuring very fast pulse-modulated signals is degraded. A simple square-law diode detector is capable of resolving the rise/fall times of fast-pulsed signals, but the dynamic range is limited to less than 30 dB typically [64], [65]. A logarithmic amplifier (logamp) can also be used to measure the power of a pulsed signal over a wider dynamic range. These devices extend the typical range of power detection to approximately 70 dB with a rise time detection of approximately 10 ns [66]-[68].

Traditional vector network analyzers (VNAs) offer impressive dynamic ranges of over 150 dB, but have previously been limited to CW measurements. The latest VNA products from industry leaders, such as Agilent Technologies or Rohde and Schwarz,
include options to allow pulse profile measurements with a dynamic range of 70-80 dB and a time resolution on the order of 10 ns [69], [70].

However, the previously mentioned techniques do not provide enough dynamic range to measure the full pulse profile for high-dynamic range systems. In these systems, the power profile must be accurately measured over a 150 dB dynamic range from the peak power down below the thermal noise floor. This work aims to address this measurement problem by introducing a high-dynamic range pulse profile measurement (HDRPPM) technique capable of measuring signals with a 160 dB dynamic range and time resolution of 5 ns, with the primary focus being measurement performance. Measurement speed is a secondary consideration in this work.

1.2 Basic Classes of Amplifiers

In the linear classes of amplifiers, the transistor is modeled as a current source. Class A operation is the most linear of the various classes of amplifiers when operated in a small signal mode. The transistor is always conducting and the maximum theoretical efficiency in this mode is 50 %. The ideal waveforms and bias point seen at the transistor are shown Figure 1.2. In Class B operation, the transistor is only conducting for half of

![Figure 1.2. Class A amplifier (a) example waveforms and (b) bias point.](image-url)
the time. An example of the waveforms and bias selection point is shown in Figure 1.3. The maximum efficiency is higher in Class B, but the amplifier is more nonlinear. The Class C amplifier expands upon this concept and reduces the conduction angle to less than half of the time. The achievable efficiency is 100 %, but not simultaneously while delivering output power. An example device waveform and bias selection point is shown in Figure 1.4 for a Class C amplifier.

### 1.3 Device Technologies

The mainstream transistor devices fabricated for use in wireless applications typically use silicon or gallium arsenide. Silicon is popular because it is cost effective to
manufacture. Gallium arsenide is used when higher frequency or higher performance devices are required. Alternative technologies exist, including an emerging market for gallium nitride devices.

Gallium nitride is attractive because it can withstand higher temperatures and voltages than competing technologies. A summary of the material properties of common semiconductors is given in Table 1.1 [71]. The key characteristics of GaN are its high bandgap and high breakdown field, as compared to Si or GaAs. A high breakdown field is desirable because it means that an active device can withstand higher voltages over a smaller device area.

There are two main types of field-effect transistor (FET) structures that are fabricated on GaN. The high electron mobility transistor (HEMT), also known as the heterostructure FET (HFET), incorporates a junction between two different materials with different band gaps, known as a heterojunction, as the channel instead of a doped region [72]. The two materials used for the heterojunction ordinarily must have the same

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Unit</th>
<th>Si</th>
<th>GaAs</th>
<th>InP</th>
<th>SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap</td>
<td>eV</td>
<td>1.1</td>
<td>1.42</td>
<td>1.35</td>
<td>3.26</td>
<td>3.49</td>
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<tr>
<td>Electron mobility at 300 K</td>
<td>cm²/Vs</td>
<td>1500</td>
<td>8500</td>
<td>5400</td>
<td>700</td>
<td>1000-2000</td>
</tr>
<tr>
<td>Saturated (peak) electron velocity</td>
<td>x10⁷ cm/s</td>
<td>1.0</td>
<td>2.1</td>
<td>2.3</td>
<td>2.0</td>
<td>2.1</td>
</tr>
<tr>
<td>Critical breakdown field</td>
<td>MV/cm</td>
<td>0.3</td>
<td>0.4</td>
<td>0.5</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>W/cm·K</td>
<td>1.5</td>
<td>0.5</td>
<td>0.7</td>
<td>4.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Relative dielectric constant</td>
<td>εᵣ</td>
<td>11.8</td>
<td>12.8</td>
<td>12.5</td>
<td>10.0</td>
<td>9.0</td>
</tr>
</tbody>
</table>
lattice constant, or the spacing between atoms. However, a pseudomorphic HEMT (pHEMT) bypasses this issue by using an extremely thin layer for one of the materials. The layer is so thin that the crystal lattice stretches to fit the other material.

1.4 Amplifier Problems

Pulsed amplifiers based on field-effect transistor technologies, such as MESFET, pHEMT, or HFET, can experience turn on/off problems in multiple ways. The first phenomenon that degrades pulse behavior is gate or drain lag, depending on whether the amplifier is pulse modulated at the gate or drain [73], [74]. The drain voltage/current waveform may respond very fast for the first portion of the transition, then a slow time constant effect takes over, limiting the turn on/off time. It is demonstrated in MESFETs that the gate lag is coupled to the presence of surface traps in the FET, and the drain lag is related to buffer layer and substrate traps [74].

The second phenomenon that can degrade pulse behavior is the instability of the FET amplifier at bias conditions near the "off" state, corresponding to low drain voltages for drain modulation and gate voltages near pinch-off for gate modulation. Amplifier design and stabilization is often only considered at the quiescent operation point. However, as the amplifier transitions through the various bias conditions while pulsing, it can enter an unstable region of operation and tend to oscillate for a brief amount of time. These oscillations are difficult to detect because they are very short in duration for fast-pulsed systems and have low power levels compared to the carrier signal. The problem is further compounded by the fact that the frequency spectrum of a pulsed signal is a \( \sin \frac{x}{x} \), or sinc, function containing sidelobes at multiples of the PRF away from the center frequency. These spectral components make diagnosis of a low-level oscillation on
a spectrum analyzer difficult. A turn-off oscillation is problematic for high-dynamic range pulsed systems because it can hold correlated energy for a time longer than otherwise expected and cause discontinuities or kinks in the turn-off power characteristics.

1.5 Transmission Lines

There are multiple types of transmission lines that are useful in this work. The fundamental nature of the coaxial line, microstrip line, coplanar waveguide (CPW), and grounded coplanar waveguide (CPWG) are discussed here. The details of the synthesis procedure for achieving the desired characteristic impedance and electrical length are not included. A more detailed theoretical background on these transmission line structures is addressed in [75]-[77].

1.5.1 Coaxial Line

One of the simplest types of transmission lines is the coaxial line [75], [76]. The basic geometry and fields within a coaxial line are shown in Figure 1.5. The coaxial line consists of an inner and outer conductor separated by a dielectric filling. The structure supports a single transverse electromagnetic (TEM) mode with a large operational bandwidth before the propagation of higher-order modes become possible. In most common coaxial lines, a form of polytetrafluoroethylene (PTFE), more commonly known as Teflon (\( \varepsilon_r = 2.2 \)), is used, which leads to a \( b/a \) ratio of approximately 3.4 to achieve a 50 ohm characteristic impedance.

Miniature coaxial lines exist with outer diameters down to 8 mil. Semi-rigid coaxial lines with an outer diameter of 20 mil are readily available from different
manufacturers that can be easily bent for use in planar systems. These miniature coaxial lines are attractive because they provide a shielded transmission line capable of operating with a relatively large bandwidth without dispersion.

1.5.2 Microstrip Lines

The microstrip transmission line consists of a single conductor trace over a ground plane, as shown in Figure 1.6. The microstrip line does not support a TEM mode due to the total field existing in an inhomogeneous dielectric (i.e., dielectric substrate and free-space). However, the substrates are typically very thin, and a quasi-TEM mode analysis can be performed [75]-[76].

The microstrip transmission line is popular due to its ease of fabrication, probing, and component connection. Series component connections are easy to fabricate in a microstrip topology, but a shunt connection to ground is more difficult due to the need for via holes (i.e., connections between layers).
The introduction of microwave monolithic integrated circuits (MMICs) has led to increasingly smaller component and pin dimensions. The pins on current MMICs have dimensions approximately 0.2 mm or smaller. A microstrip transmission line with a characteristic impedance of 50 ohm typically has a width much larger than these pin dimensions. The microstrip line can be tapered to match the width of the pin. However, tapering leads to a change in characteristic impedance and increased connection inductance, and thus an increased mismatch to a 50 ohm device. These shortcomings have been solved with other types of printed transmission lines [78].

1.5.3 Coplanar Waveguide

A coplanar waveguide transmission line consists of a strip conductor on a dielectric substrate, separated from a topside ground layer by a small gap, as shown in Figure 1.7. The characteristic impedance of the transmission line is set by both the width of the line and the gap for a fixed substrate (thickness and dielectric constant). Both series and shunt connections are easy to fabricate due to the close proximity of the ground plane. CPW has the advantage, over traditional microstrip lines, that it does not require an additional ground plane on the reverse side of the substrate.
It is possible to taper the trace and gap while maintaining a 50 ohm characteristic impedance on a substrate of fixed thickness, resulting in a better match to devices with relatively small pin sizes. It is possible to integrate both CPW and microstrip technology with properly designed transitions [78], [79].

1.5.4 Grounded Coplanar Waveguide

The grounded coplanar waveguide transmission line is similar to a CPW line with the addition of a bottom ground plane, as shown in Figure 1.8. The width of a trace in a CPWG system is smaller than that in a CPW system for the same characteristic impedance, making it attractive for high-frequency circuits and MMIC designs.

It is possible to achieve a 30 % size reduction or greater using CPWG over microstrip lines. Therefore, it is possible to place a larger ground plane between trace lines, resulting in increased isolation and reduced leakage. However, CPWG suffers from higher loss than other planar transmission line types due to the reduced trace width. In general, a large number of via holes should be used to connect the top and bottom ground planes. Guidelines suggest that the vias should be placed with a separation of λ/20 or less to achieve maximum performance by suppressing the parallel plate mode [80].
1.6 Motivation and Thesis Outline

Class E mode amplifiers may offer an advantage in systems that operate in a pulsed mode, particularly in the case where fast pulsing is employed. The topic of amplifiers operating in Class E mode in fast pulse-mode, high duty factor environments is not addressed to date. Furthermore, the application of these amplifiers in high-dynamic range systems is not fully considered in the literature due to the lack of an accurate measurement technique capable of measuring pulse characteristics over a wide dynamic range. This work aims to design and analyze Class E amplifiers operating in these conditions for application in high-dynamic range systems.

This thesis is organized as follows. The research goals for investigating Class E amplifiers in fast pulsed, high-dynamic range applications are outlined in Section 2. The high-dynamic range pulse profile measurement system is introduced in Section 3. The technique extends the state of the art in pulse profile measurement techniques. The design of a Class E amplifier optimized for pulse-mode applications is given in Section 4. The amplifiers are fully characterized and the results are presented in Section 5. Finally, a general summary of the work is presented in Section 6 along with possible future work.
2. RESEARCH GOALS

The overall purpose of this research is to investigate the potential use of pulse-mode Class E amplifiers in high-dynamic range applications. The research is divided into two main areas of interest that address the fundamental topic. The first aspect of this work focuses on a method to perform a high-dynamic range pulse characterization since this capability does not currently exist, as described in the previous section. The second aspect of this research is to investigate the applicability of high-efficiency Class E amplifiers in fast pulse-mode environments. The primary frequency range of interest in this work is the S-band (2 – 4 GHz) due to the large number of commercial and military applications in this range. Specifically, different types of switched-mode amplifiers are considered using a gallium nitride heterojunction field-effect transistor. Gallium nitride allows operation at higher voltages and higher operating temperatures compared to gallium arsenide.

2.1 High-Dynamic Range Pulse Characterization

A method of performing a pulse power profile measurement with over 150 dB dynamic range does not currently exist and has not been addressed in the literature. The techniques proposed in this work fill the critical need for this type of measurement. The method developed is not unique to Class E amplifier measurements, but general to all types of pulse measurements, whether it is a power amplifier, switch, limiter, etc. A novel approach of "tagging" a transmitted pulse with a unique code is proposed to allow for increased sensitivity in detecting this tagged signal. In general, the lower limit on the sensitivity in any measurement system is the thermal noise level in the
measurement bandwidth. The use of a coded signal and coherent integration allows
digital signal processing techniques to be used, with the added benefit of correlation gain.
Thus, signals that are below the noise floor are now detectable.

The system must be capable of supporting a fast-pulsed operation to allow for
narrow, time-gated measurement points. The proposed method takes samples of the
energy along the pulse profile to build a history of the actual power profile of the pulse.
These data points are combined to generate a full picture of the pulse over a very wide
dynamic range since additional correlation gain is available. A pictorial view of the pulse
power profile and sampled points is shown in Figure 2.1

2.2 Class E Amplifiers for Fast Switching, Pulse-Mode Operation

Class E amplifier designs have traditionally been restricted to lower frequencies
of operation due to the stringent device requirements in terms of switching characteristics
that are limited by device parasitics. The maximum frequency of operation for Class E is
different from the transition frequency ($f_T$) or maximum frequency of oscillation ($f_{\text{max}}$).
commonly associated with active devices. The maximum frequency of operation for an amplifier in *optimum* Class E mode [26] is

\[
f_{\text{max}(E)} = \frac{I_{\text{max}}}{56.5C_{\text{out}}V_{ds}}
\]

where \(I_{\text{max}}\) is the maximum current the device can safely handle, \(C_{\text{out}}\) is the output parasitic capacitance, and \(V_{ds}\) is the voltage across the device. The actual operation of an amplifier can extend beyond this maximum frequency with the tradeoff of reduced efficiency. It is clear that as the operating voltage increases, the maximum frequency of operation decreases. Therefore, this tradeoff must be carefully considered in choosing the supply voltage. In a Class E mode amplifier, the maximum voltage seen across the device can be as much as 3.56 times the supply voltage, approaching breakdown in devices optimized for low-power operation, such as in cellular telephones [81]. A high breakdown voltage process, such as GaN, allows for higher supply voltages with the advantage of reduced current draw for a higher efficiency amplifier.

Class E amplifiers should also offer the advantage of pulse-mode operation simply by pulsing the input RF signal, as discussed in the previous section. However, this mode has not been studied in the literature and it may not be suitable for high-dynamic range applications. A method of using gate and/or drain modulator circuits is considered for increasing the on/off ratio and pulse speeds of the amplifiers to improve performance for use in real systems.
3. HIGH-DYNAMIC RANGE PULSE PROFILE MEASUREMENT SYSTEM

3.1 Introduction

In high-dynamic range systems, the power amplifier pulse must turn off at a rate compatible with the system noise floor at the receive time. It is useful in high-dynamic range systems to characterize the output power of the amplifier pulse versus time, referred to as the pulse power profile. A pictorial view of an example pulse power profile is shown in Figure 2.1. A turn-off rate with two distinct regions is shown for generality. The real behavior of amplifiers may be a single linear region or include more regions depending on the pulse modulator used and on the base device characteristics.

Traditionally, pulse characterization is performed in the time domain using either a crystal/diode detector or a peak power meter. These techniques allow one to measure the rise and fall times of an RF pulse, but do not give insight into the pulse profile over the dynamic range required in highly sensitive systems. In the development of high-dynamic range systems, a technique has not previously existed to measure the pulse characteristics of an amplifier for compatibility with system level requirements. The problem then becomes that a power amplifier must be tested for compatibility in the final assembly, because only the final system is capable of making measurements over the dynamic range required. However, this testing sometimes involves a pass or fail style approach because the final assembly may only be exposed to a single point on the pulse profile. The power amplifier can be tested as a sub-assembly before the final system design is complete using the pulse profiling technique outlined in this work. Problems
can be detected earlier in the product development cycle and can be addressed when they are much easier to fix.

A high-dynamic range pulse characterization system must be capable of supporting a fast-pulsed operation to allow for narrow, time-gated measurement points over a dynamic range greater than 150 dB as shown in Figure 2.1. The method proposed and demonstrated in this work uses multiple samples of the pulse at a single time location in the pulse profile, along with a correlation technique to increase the measurement signal-to-noise ratio (SNR). Multiple time locations can be combined to generate a full picture of the pulse over a very wide dynamic range since processing gain allows for detecting signals below the thermal noise floor that limits traditional systems. Measurement results are shown on power amplifier devices in the S-band illustrating the utility of this technique to real-world amplifiers.

3.2 Measurement Concept

The basic concept of the system is to take samples from multiple pulses at a specific delay and then correlate these samples with a code impinged on the transmitted signal to obtain the power at that specific delay position. The measurement gate is then moved to the next location, and the process is repeated until the entire time region of interest is sampled. A simplified representation of the measurement sample combination concept is shown in Figure 3.1 for a single receiver delay position.

The applied code has two primary purposes. First, the code allows a correlation technique to be applied in the receiver to provide unambiguous detection of power at a specific delay. If the code is not applied, then sample energy could potentially originate
from a different pulse if the dissipation rate is slow enough [82]. Second, the code aids in the rejection of extraneous, uncoded signals that may lie in the measurement band. For example, without a coding technique, if the carrier frequency from the synthesizer leaks into the receiver, it appears as a signal and degrades the minimum sensitivity. However, with a coding technique, the correlation process spreads this leakage energy in the frequency domain and it is not detected as a signal.

The technique is similar to pulse integration used in radar systems [82]. In pulse radar systems, multiple returns from a target are combined either coherently or incoherently to increase the detectability of the target. If the combination of pulses is performed before the detection step, where the phase information from the returns is retained, then the process is called predetection integration or coherent integration.
If $N$ pulses with the same SNR are combined in a lossless coherent integrator, the integrated signal-to-noise ratio, $(SNR)_N$, is $N$ times the single pulse SNR, $(SNR)_1$, or

$$(SNR)_N = N(SNR)_1. \quad (3.2.1)$$

A processing or correlation gain $G_p$ is defined as

$$G_p = 10 \log_{10} \left( \frac{(SNR)_N}{(SNR)_1} \right) = 10 \log_{10} (N). \quad (3.2.2)$$

If the pulse integration is performed postdetection, where only the pulse envelopes are combined (i.e. magnitude only), then the processing gain is less than the value in (3.2.2), and follows a $\sqrt{N}$ relationship. It is clear that if a large number of samples are coherently processed, then signals can be measured that would otherwise be undetectable without pulse integration.

The following assumptions are made about the behavior of the amplifier response to allow a pulse integration technique to provide useful results:

1) The device under test (DUT) behavior must be consistent between pulse periods, i.e. each pulse response is identical. If the behavior of the amplifier changes from pulse to pulse, then the technique outlined in this work will provide unreliable results. However, in general, practical devices must meet this requirement or they would not be useful in real system designs.

2) The instantaneous bandwidth of the amplifier is sufficient to support the fast pulse operation as well as a phase code signal used to tag the pulses. If an amplifier is considered for use in fast, pulse-mode applications, then it must also meet this requirement. The technique proposed is equally applicable to lower speed methods, but they are not demonstrated here.
3) The response of the amplifier is consistent for the different phase states of the phase code modulation used. A phase code is impinged on the pulses applied to the DUT that allows for correlation processing in the receiver. If the response of the amplifier is different for the various phase states, then the calculated power will be inaccurate.

Several considerations in the measurement approach are made to address item 1) above. First, the position of the transmit position is kept fixed while the receive gate is moved. Therefore, the pulse conditions on the DUT are kept consistent for the duration of the test, reducing any potential variability. Second, the DUT is allowed to reach a thermal equilibrium point before measurements are performed. The devices measured in this work are allowed to operate for a minimum of two hours at full saturated output power before measurements are performed.

The limitation of other power profiling methodologies is two-fold. The first limitation is that a static input attenuation into the measuring receiver must be set according to the peak power to protect it from damage. In this technique, the input attenuation is set according to the power level at the measurement time. Therefore, as the receiver gate is moved to the leading or trailing edges of the pulse, the input attenuation is reduced. The second limitation is that the signal of interest falls below the thermal noise floor of the measurement aperture. It is difficult to extract signals from the noise without a correlation technique. This system employs coherent integration to increase the measurement SNR as well as a coding scheme to reject extraneous signals. A wise person once said that in the end, all dynamic range problems encountered when measuring power are thermal: destruction at the high end and noise at the low end.
3.3 System Block Diagram

The measurement technique demonstrated here involves four primary sections that follow the simplified block diagram shown in Figure 3.2. The first portion of the measurement system is the timing and control field-programmable gate array (FPGA) that is responsible for synchronizing the pulsing of the transmitter and receiver. This block also generates the necessary clock signals required in the digital signal processing section.

The second section is a transmitter that generates fast pulse-modulated signals. The transmitter section also impinges a code on the signal allowing digital signal processing to provide unambiguous detection of power from the DUT. The addition of the phase code also helps in the rejection of extraneous, uncoded signals that may lie in the measurement band that would adversely affect standard power measurement techniques.
The third portion of the measurement system is a receiver that is capable of providing measurement gates with the same fast transition times as the transmitter. Another requirement of the receiver is that it must provide very high on/off isolation to allow detection of very small signals, even when the input signal is very large outside of the measurement gate.

The fourth portion of the measurement system is the digital receiver section and the associated signal processing algorithms. This section includes a high-speed analog-to-digital converter (ADC) used to convert the received analog output signal to a digital representation. The digital signal is processed by a set of software algorithms developed in MATLAB that perform the signal correlation and subsequent power calculations and calibration.

3.4 FPGA Block Diagram

An FPGA is used to provide the synchronization between the timing/control signals as well as generating the code that is applied to the transmitted pulses. A Xilinx Virtex-II MB1000 development FPGA is used in conjunction with the Xilinx System Generator for DSP software for The Mathworks Simulink system simulation tool. The System Generator software adds a library of blocks to the Simulink environment that are used to create a functional model of the FPGA. The software also automatically generates the VHDL code required to program the FPGA.

The FPGA is responsible for providing the phase code, digitizer sample clock, and a trigger signal to synchronize the timing pulse generators that control the transmit and receive gates. The timing for the FPGA is controlled by a master clock signal, $CLK$, which is a 24 MHz square wave created by an Agilent 33250 function generator.
The overall system consists of 10 timing/control signals described in Table 3.1. The detailed timing diagram depicting the relationship between the various signals is shown in Figure 3.3. The delay of signals $SCLKD$ and $RXQ/N$ vary according to the sample point measured in the pulse power profile.

![System timing diagram](image)

**Figure 3.3. System timing diagram.**

<table>
<thead>
<tr>
<th>Name</th>
<th>Purpose</th>
<th>Stimulus</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>Master clock for FPGA</td>
<td>24 MHz, 3 V square wave</td>
</tr>
<tr>
<td>PSQ</td>
<td>BPSK phase code to phase modulator</td>
<td>0.5 MHz chip rate, 0-3 V</td>
</tr>
<tr>
<td>PSQS</td>
<td>BPSK phase code to digitizer</td>
<td>0.5 MHz chip rate, 0-3 V</td>
</tr>
<tr>
<td>RXQ*</td>
<td>Turn receiver on/off</td>
<td>0.5 MHz, 250 ns pulse width, 0-3 V</td>
</tr>
<tr>
<td>SCLK</td>
<td>Sample clock to delay generator</td>
<td>12 MHz, 3 V square wave</td>
</tr>
<tr>
<td>SCLKD</td>
<td>Delayed sample clock to digitizer</td>
<td>12 MHz, 3 V square wave</td>
</tr>
<tr>
<td>TRG</td>
<td>Trigger for pulse generators creating $TXQ/N$, $RXQ/N$, $TXQA$, $TXQB$</td>
<td>0.5 MHz, 3 V square wave</td>
</tr>
<tr>
<td>TXQ*</td>
<td>Turn transmitter pulse modulators on/off</td>
<td>0.5 MHz, 250 ns pulse width, 0-3 V</td>
</tr>
<tr>
<td>TXQA</td>
<td>Turn transmitter PA on/off</td>
<td>0.5 MHz, 250 ns pulse width, 0-3 V</td>
</tr>
<tr>
<td>TXQB</td>
<td>Turn DUT on/off</td>
<td>0.5 MHz, 250 ns pulse width, 0-3 V</td>
</tr>
</tbody>
</table>

*Denotes that a signal compliment exists
A maximal length pseudorandom noise (PN) code is used as the modulation code in this system. A PN code is attractive because very long code sequences can be generated without repetition, which is useful for gathering long data sequences. Additionally, the autocorrelation properties of the PN sequence are very good, resulting in low correlation values for any shift in code [83]. The normalized autocorrelation of the PN code used in this system for \( \sim 350 \text{ kSa} \) is shown in Figure 3.4.

The PN code is generated using a linear feedback shift register (LFSR) in the FPGA. The method in which the outputs of the registers are fed back to the input sets the behavior of the output code. A Fibonacci implementation is used where the outputs of specific registers are compared in an exclusive-OR gate and fed back to the input of the shift register. A shift register with length \( N = 28 \) and feedback taps set for a maximal length code is used. The code generated has a clock pulse repetition period of \( M = 2^{N-1} = 268,435,455 \). The chip period is 2 \( \mu \text{s} \), which translates to a maximum measurement time of \( \sim 536 \text{ s} \) before the code is repeated.

![Figure 3.4. PN code autocorrelation for \( \sim 350 \text{ kSa} \).](image-url)
The PN code is output on two pins of the FPGA, \( PSQ \) and \( PSQS \). The \( PSQ \) signal is used to control the binary phase-shift keying (BPSK) modulator in the transmitter section. The \( PSQS \) signal is sent to the digitizer and sampled for use when calculating the correlation of the received signal. These signals are identical, but separated to provide isolation between the transmitter and receiver sections and to reduce the signal integrity problems that arise from mismatched lines.

A trigger signal, \( TRG \), is generated by dividing the master clock signal by 48 to create a 0.5 MHz square wave. This signal is required to provide synchronization between the PN code and the timing signals \( RXQ/N \) and \( TXQ/N \). The \( TRG \) signal controls the first Agilent 81110 pulse generator that generates \( TXQ/N \). This generator is set as the master pulse generator in the system. The other pulse generators are set as slave to this pulse generator and are triggered when the master is triggered.

A square wave sample clock, \( SCLK \), is created by dividing the master clock signal by two, providing an IF sampling rate of 12 MHz. The \( SCLK \) signal is used to trigger an Agilent 8110 pulse generator that outputs a delayed version of the sample clock, \( SCLKD \). This additional pulse generator is used to provide fine resolution positioning of the sample clock to keep the relative sample position fixed within the receive gate as it is moved in time.

### 3.5 RF Block Diagram

The simplified block diagram of the RF section (transmitter and receiver) of the measurement setup is shown in Figure 3.5, and the detailed block diagram is shown in Figure 3.6. The components in the transmitter and receiver chain are chosen to operate within the S-band. However, a single frequency of operation is used when testing the
characteristics of the DUT. Bandpass filters are used to provide higher selectivity to the transmitter and receiver sections. The band of operation is then easily modified by changing the filters and performing a new calibration.

3.5.1 Receiver Design

The RF receiver design in the HDRPPM system is the most complicated section for multiple reasons. The minimum sensitivity of the system is set by the receiver, and it must be capable of detecting the very low-power signals on the leading and trailing edges of the DUT pulse. Therefore, the noise figure of the receiver must be suitably low to maintain an acceptable SNR at the output. Second, the receiver must be capable of providing high isolation in the off state so that the very small signals during the pulse transitions are not hidden by the high power of the DUT within the main pulse time. The receiver design progressed through several iterations, as described in the following sections.
Figure 3.6. Detailed RF block diagram.
3.5.1.1 Homodyne vs. Superheterodyne

The homodyne and superheterodyne topologies are both considered in the design phase of the receiver. A homodyne receiver includes a single downconversion stage that directly converts the input RF signal down to DC. A superheterodyne receiver includes at least one intermediate frequency stage before any further downconversion. The design of a receiver in a fast-pulsed system must include careful consideration of the spectra of the switching control voltages with respect to the output frequency.

The homodyne receiver is attractive because of its simpler implementation, and it does not require an additional oscillator. The superheterodyne receiver is capable of providing higher selectivity because higher $Q$ filters are available at the IF frequency as compared to filters at the RF frequency. The superheterodyne topology also has some other advantages in fast-pulsed systems with respect to rejection of noise generated by the switching control signals.

A homodyne receiver is first considered for the pulse characterization system and follows a block diagram similar to the superheterodyne system, with the exception that the LO frequency is equal to the transmitter frequency, $f_{LO} = f_{RF}$. The main problems with a homodyne receiver topology arise at the downconversion mixer in the form of voltage offsets at the output. It seems feasible that the offset voltage at the output of the mixer is a fixed value and could be compensated with a simple DC block that also passes the signal of interest. However, the fast pulsing in the receiver complicates this simplistic situation.

In any practical mixer, there is a finite isolation between the LO and RF ports. A portion of the signal applied at the LO port exits RF port of the mixer. The return loss of
real components is finite; therefore, some of the LO leakage signal reflects off the preceding component and enters the RF port of the mixer. The pulse characterization receiver requires that an RF switch immediately precede the downconversion mixer to blank the amplified noise from the RF amplifiers during the receiver off time. The output impedance of the switch is time varying, since the switch is toggling between the through path and its internal 50 ohm load. Therefore, the reflected LO signal that is entering the RF port takes the form of a pulsed signal with an on/off ratio equal to the difference in the output return loss of the two states of the RF switch. This modulated LO signal mixes with itself and forms a square wave at the IF port which is a replica of the switch control signals. This undesired signal is extremely large compared to the small signal of interest in this receiver design because a high IP3 mixer is used that requires the LO drive signal be greater than 17 dBm. A more complex active cancellation scheme must be used to compensate for these large transient signals.

A superheterodyne topology circumvents the voltage offset problems because the output signal is offset by the IF frequency. It is convenient to choose a low IF frequency because higher performance ADCs exist to directly digitize the downconverted signal. However, the switching transients must also be considered in the superheterodyne receiver. An investigation into the frequency content of the control signals must be performed to realize the requirements on the IF frequency.

3.5.1.2 Suppression of Switching Transients

The waveforms used to control the receiver are complimentary signals given the designation $RXQ$ and $RXQN$. These signals are 3 V, square waves with $RXQ$ taking a logic high value when the receiver gate is open and providing gain (see timing diagram in
If the signals are perfect square waves, then the envelope of the frequency spectrum follows a sinc function in the form of $\sin(\pi \tau f) / \pi \tau f$, where $\tau$ is the pulse width. In this case, the spectrum envelope rolls off with a slope of -20 dB/decade after the break frequency $1/\pi \tau$. However, the outputs are not ideal square waves and are modeled as a trapezoidal pulse with finite rise and fall times as shown in Figure 3.7.

The signals output by the pulse generator are set to have equal rise/fall times. In this case, with $\tau_r = \tau_f$, the envelope of the spectrum of the trapezoidal pulse [84] is

$$20 \log_{10} (\text{env.}) = 20 \log_{10} \left( \frac{2A \tau}{T} \right) + 20 \log_{10} \left[ \frac{\sin(\pi \tau f)}{\pi \tau f} \right] + 20 \log_{10} \left[ \frac{\sin(\pi \tau_r f)}{\pi \tau_r f} \right]. \quad (3.5.1)$$

The resultant envelope has three distinct regions as shown in Figure 3.8. The first region is dominated by the duty factor and has a 0 dB/decade slope. The second region is dominated by the pulse width and has a -20 dB/decade slope beginning at the break frequency $1/\pi \tau$. The third region is dominated by the rise/fall times of the pulse and has a -40 dB/decade slope beginning at the break frequency $1/\pi \tau_r$. This analysis assumes that the pulse width is greater than or equal to the pulse rise/fall time. Therefore, it is

![Figure 3.7. Ideal trapezoidal pulse waveform.](image-url)
clear that the high-frequency content of a trapezoidal waveform is dominated by the rise/fall times of the signal.

The low-frequency square wave signal used to control the switch leaks through the switch onto the RF output, commonly called video feedthru. The video signal is a replica of the control signals with a reduced power level. Therefore, it appears as a sinc function centered at DC in the frequency domain and follows the same envelope response as calculated in (3.5.1). The control signals have fast rise/fall times of 1.6 ns. Therefore, energy exists in the frequency spectrum extending to several hundred megahertz. This signal reaches the downconversion mixer that has a finite isolation between the RF port and IF port. The majority of the gain in the receiver is located in the IF chain so that higher selectivity is achieved. If an IF frequency is chosen where there is significant energy remaining in the video transient spectrum, then this leakage signal is amplified, and the overall receiver performance is degraded since this energy adds to the noise floor. A higher IF frequency beyond the frequency breakpoint for the rise time is desirable.
since the energy from the switching transients is greatly reduced, easing the requirements on the RF high pass filter.

An example of a 50 MHz IF output is shown in Figure 3.9 for the noise-only and signal input cases. The signal input case uses a -70 dBm signal at the RF input under the conditions $f_{RF} = 3$ GHz and $f_{LO} = 3.05$ GHz. A control signal with $\tau = 250$ ns, $\tau_r = \tau_f = 1.6$ ns, and $D = 33$ % is used to modulate the RF switches. It is shown that signal energy exists extending into several hundred megahertz for these pulse conditions. Therefore, signal components exist within the 50 MHz band and pass through the IF filters used. The signal that passes through the RF filters is then amplified and appears at the IF output, as seen by the ringing in the noise-only and signal input cases. A high pass filter with much greater rejection is required in the RF section to provide more isolation to the transient signals. A higher order filter provides increased rejection of these signals. However, it also adds additional loss and delay that is problematic in some receivers.

A higher IF frequency beyond the frequency breakpoint for the rise time is desirable since the energy from the switching transients is greatly reduced, easing the requirements on the RF high pass filter. An example of a 315.5 MHz IF output is shown in Figure 3.10 for the noise-only and signal input cases. The signal input case uses a -70 dBm signal at the RF input under the conditions $f_{RF} = 3$ GHz and $f_{LO} = 3.3155$ GHz. The control signal conditions are the same as the 50 MHz IF case. In this case, the noise-only output exhibits the clean "puff" of noise as the receiver gate turns on and provides the full gain to the thermal noise at the RF input. Similarly, the IF output signal is clean when viewed with a signal applied at the RF input.
3.5.1.3 Final Receiver Design

Ultimately, the superheterodyne receiver topology is chosen to provide rejection of the switching transients. The first element in the receiver front-end is a high-power RF switch that is capable of dissipating up to 10 W of input power with switching speeds similar to the other pulse modulators. Two additional pulse modulators follow the input high-power switch to provide over 130 dB isolation before the first low-noise amplifier (LNA). The high isolation before the first LNA is required to keep the signal power from
the transmitter extremely low during the receiver off time so there is no potential for saturation in the amplifier. The LNA in the system has a noise figure of ~1 dB at 3 GHz. The LNA sets the front-end noise figure and provides ~25 dB gain. Additional pulse modulators and another amplifier follow the input LNA in the RF front-end. The total receiver on/off isolation is greater than 200 dB, which is important for overall system sensitivity.

A high side LO signal is used, allowing the image frequency and noise to be eliminated with a simple low-pass filter. A high IP3 downconversion mixer is used to convert the carrier from $f_{RF}$ to $f_{IF}$. An IF frequency of 315.5 MHz is chosen due to the availability of IF filters and the ability to reject switching transients.

The input high-power switch is a key enabling element that allows the receiver to measure low-power signals on the trailing edge of the transmitted pulse. It can blank the high power of the transmitted pulse allowing the receiver to amplify the very small signals for processing. A standard GaAs RF switch can typically handle a 20 dBm input signal without distortion. The high-power switch allows an input signal of up to 40 dBm without distortion. Therefore, less attenuation can be used between the DUT and the receiver, increasing the sensitivity.

### 3.5.2 Transmitter Design

The transmitter section begins with a frequency synthesizer that generates a CW signal at frequency $f_{RF}$ in the S-band. A BPSK phase code is applied to the CW carrier through a mixer that acts as a biphase modulator. The input signal is amplified and pulse modulated to achieve a high on/off ratio. The pulse modulation is achieved by running the RF signal through a GaAs FET switch that toggles between the through path and a
50 ohm termination. The switches are capable of operating with fast rise/fall times and provide over 50 dB isolation per stage. Multiple switches are used in the system to provide a high on/off ratio to the signal applied to the DUT. A bandpass filter is used to reduce the overall system bandwidth to 200 MHz.

The power level at the input to the receiver changes drastically as the position of the receiver gate is moved to overlap with the transmit gate. An HP 8496H 110 dB programmable step attenuator is used to provide full coverage of attenuation levels required to prevent the receiver from saturating in gate overlap conditions. A static attenuator is used, as necessary, prior to the programmable attenuator to prevent damage to the device.

### 3.6 Digital Receiver Design

The choice of sampling frequency in a system depends on the characteristics of the signal, as well as other system considerations. If a signal is a lowpass signal, containing information from DC to some upper frequency $f_{max}$, the uniform sampling theorem dictates that the signal must be sampled at least twice as fast as the highest frequency component to be able to reconstruct the original signal. However, if the signal is categorized as a bandpass signal where the information bandwidth is centered at a non-zero carrier frequency, then alternative sampling schemes become available.

The theory of undersampling, sometimes referred to as subsampling, bandpass sampling, or direct RF/IF sampling, involves sampling a signal at a rate of at least twice the information bandwidth and using the effect of aliasing to downconvert the signal [85]. The carrier frequency of $f_{RF} = 3$ GHz is used to excite the DUT in the measurements reported in this work. The LO frequency is set to $f_{LO} = 3.3156$ GHz to provide an IF
output signal at 315.6 MHz. An effective sampling rate, resulting from the combination
of the digitizer sampling rate and decimation, is 0.5 MHz that aliases the signal band at
\(f_{IF}\) to be centered on DC. The LO signal offset is added so the final aliased signal appears
at a 100 kHz offset from DC. The 100 kHz offset is chosen to place the aliased signal
approximately in the center of the discrete Fourier transform (DFT) bandwidth after
digital signal processing, giving an oversampling ratio of 2.5.

The analog-to-digital converter used in an undersampling system must have an
analog bandwidth capable of supporting the full IF information band, even if a slow
sample rate is utilized. An Acqiris DP240 digitizer card is selected that has a front-end
analog bandwidth of 1 GHz and 8 bits of resolution on its two channels. The digitizer
also supports a large acquisition memory depth of greater than 8 million points per
channel. The large memory depth is important for sampling multiple consecutive pulses
to perform the coherent integration required to detect very low-level signals.

The choice of sampling at the IF significantly decreases the complexity of the RF
block diagram at the expense of increased requirements on the stability of the sampling
clock. An additional downconversion stage in the receiver is required if direct IF
sampling is not used. This downconversion stage requires an additional stable local
oscillator (STALO) at the IF frequency to downconvert the received signal to near DC
before passing to an ADC. However, the transmitter also requires that the STALO IF
signal be upconverted to \(f_{RF}\) in the transmitter to maintain full phase coherency between
the transmitted and received signals.

As the digital section of a system is moved closer towards the RF front-end, then
the requirements on oscillator phase noise and sample clock jitter become much more
stringent. Jitter is the time uncertainty of the zero crossings of a signal. Jitter can translate to AM noise on a digitized signal due to the fact that the sample position varies randomly from sample to sample, resulting in a different sampled amplitude value than the expected result, as shown in Figure 3.11. The signal is expected to be sampled at the time instant $t_n$. However, the actual sample time may vary from the expected sample time if jitter is present in the system. If the actual sample time is different by a value of $\tau_n$, then a random amplitude error of $\varepsilon_\tau(n)$ is generated.

The maximum available SNR is degraded due to the presence of random jitter on the sample clock. If the jitter term is much greater than the amplitude noise [86], then the maximum available SNR is described as

$$SNR_{max} = -20\log_{10}(2\pi f_tj_{r,m}) ,$$

(3.6.1)

where $f$ is the carrier frequency and $j_{r,m}$ is the RMS value of the sample clock jitter. The random jitter on the sample clock is measured as 54 ps in this work, which becomes a limiting factor in an 8 bit system.

Figure 3.11. Graphical representation of AM noise on a digitized signal due to jitter.
3.7 System Considerations

An important consideration in this system is maintaining the isolation between the transmitter and receiver sections as well as the on/off isolation in the respective chains. Each block of the transmitter and receiver is housed in an individual Faraday shielded enclosure to prevent stray signals from unintentionally leaking around elements. An example of one of the RF switch enclosures is shown in Figure 3.12.

The bias lines to the amplifiers and switches are routed with shielded cable, and significant RF bypassing is used in the individual circuits to prevent signals from coupling through the supply lines. Low pass filters are used on all of the control signal lines at each block to prevent RF signals from escaping the shielded enclosures through these ports.

A picture of the full RF section of the HDRPPM system is shown in Figure 3.13. System performance could be further improved if elements in the transmitter and receiver were integrated into a single assembly to reduce the interconnect losses. Higher performance components that achieve increased levels of integration, such as including the pulse modulator with an image reject downconversion mixer, would allow size

![Example RF shielded enclosure](image)

Figure 3.12. Example RF shielded enclosure.
reduction of the overall assembly [87]. Special attention would need to be made to ensure that adequate isolation is maintained between blocks in the same way to achieve the desired system performance.

### 3.8 Signal Processing and Correlation Algorithm

The algorithm used to correlate the received signal and calculate the power value is shown in block diagram form in Figure 3.14. The digitizer card has several different triggering methods available, such as internal clock, external reference, and external clock. The external clock mode is used since the undersampling technique requires that the sample clock be phase-locked to the RF and LO signals so that the sample is taken in the same location on the IF waveform each period. If the sample clock is not locked to the RF sources, then the sample position can vary over the course of the measurement.
window and the decimation process will fail. A stable 10 MHz reference is shared
between the RF, LO, and clock generation sources to maintain the necessary phase lock.

3.8.1 Determine Reference Position

The Acqiris DP240 card has two possible modes of operation when used with an
external clock: start/stop and continuous mode. In start/stop mode, the digitizer only
takes an acquisition when it receives a software trigger. In continuous external clocked
mode, the digitizer operates similar to the start/stop mode, but restarts the acquisition
after the memory buffer is filled. In either mode, it is not possible to provide a hardware
trigger input to tell the digitizer when to begin an acquisition. Therefore, it is necessary
to analyze the captured data to determine a reference position in the signal to know which
samples to decimate. The phase code signal $PSQ$ is a known signal and occasionally
transitions at the beginning or end of a chip. The first transition of the acquired $PSQ$
signal is detected and the samples are numbered from 1 to 24 from this point forward, as
shown in Figure 3.15.

Figure 3.15. Sample numbering scheme used in (a) normalized phase code and (b) IF
output sampled data.
3.8.2 Decimate Signal

The IF signal is sampled at a rate of 12 MHz. The PRF and phase code chip rate are 0.5 MHz (2 µs PRI) while the receiver pulse width is 250 ns, resulting in the possibility for three samples to fit within the output IF pulse. One sample is placed at the center of the output IF pulse and the other two samples are on the rising and falling edges of the pulse. The center sample is the only valid sample, and the other two samples are used for informational purposes only. The other 21 samples are digitizing noise and do not contain valid information. The sample rate is based on the limitations of the digitizer card, which has a minimum sample rate of 10 MHz. A lower sample rate ideally would be used which would reduce the required decimation rate, resulting in a larger number of valid pulse samples. However, it is difficult to find a digitizer that has a high analog bandwidth and allows very low sample rates.

The sample-numbering scheme is based on the location of the transitions in the phase code since a third channel of data is not available as a marker. The position of the transmitter gate (TXQ) and phase code signal is kept fixed so that the conditions on the DUT are kept consistent throughout the test sequence, which also allows for determining the reference position within the sampled data. The position of the receiver gate is varied to measure the power at different points in time, resulting in the valid sample number changing as a function of receiver delay. The appropriate sample number is determined for the receiver delay, and only this sample of the IF signal and phase code is retained.

The pulse-processing algorithm correlates one sample within each pulse with the phase code value during the pulse. Therefore, the signal must be decimated by a factor of \( D = 24 \) to retain a single sample. Let the original sampled voltage sequence of the phase
code and IF output be $v_{PSQ}$ and $v_{IF}$, respectively. Then the decimated signals are related to the original sequence through the decimation rate $D$ as

$$v_{PSQ,D}[n] = v_{PSQ}[nD + i_{ref}]$$
$$v_{IF,D}[n] = v_{IF}[nD + i_{ref}], \quad (3.8.1)$$

where $i_{ref}$ is the index to the first valid sample within the pulse.

### 3.8.3 Correlate

A BPSK phase code is applied to the transmitted signal, resulting in a signal that is either positive or negative at the receiver. The signal is demodulated by simply multiplying the received signal by an appropriate delayed version of the normalized phase code values. The phase code values must be normalized (1 or -1) to not alter the magnitude of the received signal, since the goal is to determine the power of the received signal. The correlator output is

$$v_{corr}[n] = v_{IF,D}[n]v_{PSQ,D}[n - R], \quad R = 0, 1, 2, \ldots \quad (3.8.2)$$

where $R$ is the phase code delay and takes on discrete values depending on where the sample position is made with respect to the phase code transition. If the sample is taken before the phase code transition, then $R = 0$ because the transmitted signal correlates with the current phase code value. If the sample is made after the phase code transition, then $R = 1$ because the transmitted signal correlates with the previous phase code value.

The output of the correlator is a sine wave at the offset frequency of 100 kHz, and the power of the correlated signal is proportional to the power at the output of the DUT. An example of a portion of the correlator output for a sample position within the transmitter gate is shown in Figure 3.16.
3.8.4 Power Spectral Density

The power spectral density (PSD) of the correlated signal is calculated, providing a means of calculating the power of the correlated signal in the presence of noise. Several different techniques are available for calculating the PSD of a signal and are efficiently coded in many software packages, such as MATLAB. The PSD in this system is calculated using Welch's method of overlapping periodograms [88]. The signal is divided into segments of length $0.5N$ with an overlap of $0.35N$ per segment, where $N$ is total number of points in the captured signal. A Hamming window is applied to each segment before processing. An example plot of the PSD for one sample position is shown in Figure 3.17.

The PSD covers the frequency range up to $f_s/2 = 250$ kHz. The power of the signal at 100 kHz is found by integrating the PSD over the effective correlation bandwidth, as shown by the shaded area in Figure 3.17(b). The PSD is integrated numerically using the trapezoidal integral approximation. The signal power is defined at the reference plane at the input to the digitizer card and must be calibrated to move the reference plane back to the output of the device under test.
Figure 3.17. Power spectral density example for one sample position depicting (a) the full PSD of the output signal and (b) zoomed view of the carrier signal and correlation bandwidth for integration.

The use of the code allows for separating signals at different delay values, i.e. previous output pulses. An example of the algorithm applied to all possible samples and delay values up to \( R = 2 \) at a single receiver delay position is shown in Figure 3.18. The three samples that lie within the receiver gate \((S = 21, 22, 23)\) correlate at \( R = 0 \). The center sample \((S = 22)\) is used for the power calculations and is noted by the letter \( S \) in the figure. There is no correlation for higher delay values since there is no detectable energy present at these ranges. The signal is still present at these sample positions, but the correlation algorithm spreads the energy from uncorrelated signals into the noise. However, the total power in the spectrum remains unchanged, as shown in Figure 3.19. The consequence is that the effective noise floor is raised at these higher delay values.
Figure 3.18. Correlation SNR versus delay for all samples (a) 3D bar chart and (b) top view intensity chart. $S$ denotes the active sample and $M$ denotes the sample with maximum correlation.

Figure 3.19. Total power versus delay for all samples (a) 3D bar chart and (b) top view intensity chart. $S$ denotes the active sample and $M$ denotes the sample with maximum correlation.

3.9 System Simulation

A simulation of the correlation algorithm is developed in MATLAB to validate the proposed technique. The simulation is performed beginning at the intermediate frequency in the receiver to conserve memory usage. A CW carrier signal is created as

$$v_{\text{carrier}}[n] = A \cos(2\pi f_{\text{ip}} nt_s),$$  \hspace{1cm} (3.9.1)
where $A$ is the amplitude of the voltage waveform, $f_{IF}$ is the frequency of the IF signal, and $t_s$ is the time step. The amplitude of the signal in the simulation is chosen to be $A = 1$ V, corresponding to a power of 10 dBm in a 50 ohm system. The carrier frequency is $f_{IF} = 315.6$ MHz to match the real system. The IF signal is sampled at 6 GHz, resulting in a time step of $t_s = 0.167$ ns. The system is simulated with a PRI = 2 $\mu$s and pulse width of 250 ns to match the real system specifications. The number of pulses that can be simulated is limited by the memory of the computer. A simulation with $N = 4001$ pulses is shown, which results in a memory usage of approximately 6 GB in MATLAB R2008a on a Windows XP x64 computer. The CW carrier signal is shown in Figure 3.20 for the full simulation time span and a zoomed portion at the beginning of the signal.

![Simulated carrier signal](image)

Figure 3.20. Simulated time domain carrier signal (a) full time interval and (b) zoomed time interval.
The signal is then pulse modulated by multiplying the CW carrier signal by a pulse train signal as

\[ v_{\text{pulse}}[n] = v_{\text{carrier}}[n] \cdot \left( \prod \left( \frac{nt}{\tau} \right) \ast \sum_{m=-\infty}^{\infty} \delta(nt - mT) \right), \] (3.9.2)

where \( \prod(t/\tau) \) is the rectangular pulse function with width \( \tau \), \( \delta(t) \) is the unit impulse function, \( T \) is the PRI, \( m \) takes on discrete values, and the symbol * denotes the convolution operator. The pulse modulated carrier is shown in Figure 3.21(a). A phase code signal is generated by creating a pseudorandom signal that is either +1 or -1 and has a chip rate equal to the PRI. An example of the phase code signal is shown in Figure 3.21(c). The phase code is applied to the pulse-modulated signal by multiplying

![Simulated signals](image)

Figure 3.21. Simulated signals: (a) pulse modulated carrier, (b) pulse modulated, phase coded carrier (c) applied phase code.
the two signals, expressed as

$$v_{\text{coded}}[n] = v_{\text{pulse}}[n] \cdot v_{\text{PSQ}}[n],$$  \hspace{1cm} (3.9.3)

where $v_{\text{PSQ}}$ is the normalized voltage values of the phase code signal. The phase coded signal is shown in Figure 3.21(b).

Two cases of signals are simulated. An ideal signal without noise is simulated to validate the accuracy of the power detection algorithm. A signal with additive white Gaussian noise (AWGN) is also simulated to validate the power detection algorithm in the presence of noise, such as is present in the real system. An AWGN noise signal is created as

$$v_{\text{noise}}[n] = A_\sigma \cdot \text{randn}[n],$$  \hspace{1cm} (3.9.4)

where \text{randn} creates a pseudorandom value drawn from a normal distribution with zero mean and a standard deviation of one, and $A_\sigma$ is the standard deviation of the noise signal. A noise signal with a standard deviation of 0.1 V is used in the simulation results shown. The noise is added to the coded IF signal as

$$v_{\text{coded,noise}}[n] = v_{\text{coded}}[n] + v_{\text{noise}}[n].$$  \hspace{1cm} (3.9.5)

The signal is then undersampled to simulate the output of the ADC. The original signal is sampled at 6 GHz and reduced to 12 MHz, resulting in an undersampling ratio of $R_U = 500$. The undersampling is performed by retaining only every $R_U$ sample of the original waveform

$$v_{\text{IF,U}}[n] = v_{\text{coded}}[R_un],$$

$$v_{\text{PSQ,U}}[n] = v_{\text{PSQ}}[R_un].$$  \hspace{1cm} (3.9.6)
The undersampled signals are shown in Figure 3.22 with red x’s for both the ideal and AWGN cases.

At this point, the signals are identical to the data that is output by the digitizer card. Therefore, the same algorithm that is described in Section 3.8 is applicable. The first transition in the applied phase code is detected and the samples are numbered as shown in Figure 3.23. The signal is then decimated and correlated with the phase code. A portion of the resultant output is shown in Figure 3.24. Finally, the power spectral density of the correlated signal is calculated. The result for the ideal and AWGN cases is shown in Figure 3.25. The detected power is approximately 10 dBm in both cases. This result compares favorably with the known power of the input carrier signal, which is 10 dBm.
Figure 3.23. Simulated sample numbering scheme used with (a) phase code (ideal), (b) IF output signal (ideal), (c) phase code (AWGN), and (d) IF output signal (AWGN).

Figure 3.24. Simulated correlator output for (a) ideal and (b) AWGN cases.

Figure 3.25. Simulated PSD of correlated signal (a) full range (ideal), (b) zoomed view (ideal), (c) full range (AWGN), and (d) zoomed view (AWGN).
3.10 Calibration

The power calculated from the algorithm in Section 3.8 is referenced to the input of the digitizer card. The desired result is the pulse profile at the output of the device under test. Therefore, the power measured must be compensated for the system gain and loss to move the reference plane back to the output of the amplifier (see Figure 3.5).

3.10.1 RF Gain Compensation

The gain (or loss) after the output of the DUT is divided into four main sections. The total gain of the system is defined as

\[ G_{RF} = G_{Static\,Atten} + G_{Prog\,Atten} + G_{Rx} + G_{IF\,Cable}, \]

where \( G_{Static\,Atten} \) is the gain of the static attenuator immediately following the DUT, \( G_{Prog\,Atten} \) is the gain of the programmable attenuator, \( G_{Rx} \) is the conversion gain of the receiver, and \( G_{IF\,Cable} \) is the gain of coaxial cable connecting the IF output to the digitizer input port. The values for \( G_{Static\,Atten} \), \( G_{Rx} \), and \( G_{IF\,Cable} \) remain fixed for all receiver delay values. The value of \( G_{Prog\,Atten} \) is varied depending on the available input power to the receiver to keep the receiver from saturating during full overlap conditions of the receiver and transmitter gates.

3.10.2 Jitter Loss Compensation

The sample clock jitter in the system has the effect of spreading the power of signals in the frequency domain. The total power of the signal is unaffected. Therefore, the peak of the signal is reduced in the PSD when processing a signal with no phase coding. The correlation process serves to despread the signal in the frequency domain.
However, the signal peak remains at the same value. The amount the signal power is reduced from the true value remains constant for any input signal level. Therefore, a static offset value is used to compensate for the jitter loss. A static value of $G_{\text{jitter}} = -0.7 \text{ dB}$ is used for all delay values based on calibration results for a known input signal level.

### 3.10.2.1 Overall Power Compensation

The power measured at the reference plane of the digitizer is referenced to the output of the DUT by subtracting the gain of the RF receiver and the jitter gain. Therefore, the power at the reference plane of the DUT is

$$ P_{\text{DUT}} = P_{\text{corr}} - G_{\text{RF}} - G_{\text{jitter}}, $$

(3.10.2)

where $P_{\text{corr}}$ is the calculated correlated power from the algorithm defined in Section 3.8, and the other terms have been defined previously.

### 3.11 Power Measurement Specifications

It is important to consider the accuracy and repeatability of the measurement results. The power measurement specifications are validated in this system by measuring an input signal with a known power level. The block diagram of the measurement specification test setup is shown in Figure 3.26. A signal generator is used to provide a stable input signal. The output of the signal generator is split and applied to a spectrum analyzer and the HDRPPM system. The spectrum analyzer measures the power of the signal ($P_{\text{real}}$) and provides the baseline level for calculating the power accuracy in comparing the power measured by the HDRPPM system ($P_{\text{meas}}$).
The power measurement accuracy and repeatability in any system is influenced by the SNR of the signal. The SNR of signals measured by the HDRPPM system vary from approximately -40 dB to 10 dB. Signals with a SNR below -40 dB are not reliably detected. The SNR of signals measured within the main pulse of a DUT typically have a high SNR. The SNR decreases as the samples move away from the center of the pulse.

A set of measurements is performed on a power range with a nominal SNR of -20 dB. The measured power versus real power response is shown in Figure 3.27. The linearity of the system is very good under nominal SNR conditions with a variation of less than 0.1 dB. The accuracy and repeatability of the measurements are shown in Figure 3.28. The accuracy of the technique is quite good, with a difference of less than 0.1 dB from the real power values. The repeatability is better than 0.4 dB under nominal SNR conditions. The repeatability of the overall measurement is primarily driven by the repeatability of the digitizer.
The power measurement specifications are given as a function of SNR with the minimum sample size of $N \approx 350$ kSa in Figure 3.29. The accuracy and repeatability of the system is considerably degraded in the low SNR regions below -30 dB. The situation is significantly improved if the sample size is increased in the low SNR regions. The
results for increasing the sample size by five times below -30 dB SNR are shown in Figure 3.30. In this case, the accuracy improves to better than 0.5 dB at a SNR level of -40 dB. The repeatability is also significantly improved in this region. All power measurements using the HDRPPM technique that are shown in this work utilize additional samples in the low SNR regions to improve the repeatability of the measurement results.

Figure 3.29. HDRPPM power measurement specifications versus SNR for minimum sample size \( (N \approx 350 \text{kSa}) \).

Figure 3.30. HDRPPM power measurement specifications versus SNR with sample size increased \( (N \approx 1.75 \text{MSa}) \) for SNR values less than -30 dB.
3.12 Measurement Control and Automation

The complete measurement system includes the hardware described in the previous sections, as well as a collection of power supplies, signal generators, and pulse generators that control the transmitter/receiver gates and sample clock position. The process of controlling the receiver delay position, setting the appropriate attenuator value, and acquiring data from the digitizer is completely automated in the MATLAB environment using an in-house test automation framework.

3.13 Experimental Results

The final power amplifier in the pulse profile measurement system is a 2–3 GHz, 12 W Microwave Power, Inc. (MPI) L0203-41 linear amplifier with an integrated pulse modulator capable of generating pulses with typical rise/fall times approximately 20-30 ns, as specified by the manufacturer. This amplifier is measured to provide the baseline of pulse behavior characteristics for the other amplifier measurement results presented in this work.

A TTL control pulse with a width of 250 ns and PRI of 2 µs (12.5% DF) is applied to the transmitter section to generate an output RF pulse width of approximately 240 ns as measured by a diode detector. The delay of the control signals to the pulse modulators in the transmitter ($TXQ/N$) is set to center the RF pulse in an optimum position for the Microwave Power PA to achieve the maximum output power and pulse width.

A static attenuator with value of 13 dB is used immediately following the amplifier to reduce the signal level into the programmable attenuator to prevent damage to the device. A large heat sink and fan are used to provide cooling for the amplifier. The
device is operated for a minimum of 2 hours at full saturated output power before the
measurements are taken to ensure a stable thermal operating point for the amplifier.

The pulse power profile for the MPI amplifier is shown in Figure 3.31. The pulse
is sampled in 5 ns steps within the pulse time and in 10 ns steps elsewhere. The total
measurement time is 5.5 hours using a 3.0 GHz Pentium 4 computer. The results using
the HDRPPM technique illustrate the pulse behavior over greater than 160 dB range.
The power profile is compared to the traditional measurement techniques using a diode
detector or a peak power meter. An HP 8472B crystal detector is used as the standard
detection method. An Agilent N1912A peak power meter is used as the industry
benchmark for comparing this work's results to peak power meter results.

The accuracy of the technique is demonstrated by comparing the peak power level
of the pulse for the three different measurement techniques. The maximum power of the
pulse is measured to be 42.5 dBm using the HDRPPM technique, compared to a result of
42.4 dBm and 42.3 dBm for the diode detector and peak power meter, respectively. In
particular, the power on the rising and falling edges of the pulse tracks well with all three
measurement techniques within their respective dynamic ranges.

The initial turn-off rate of the amplifier is dominated by the pulse modulators in
the transmitter. Two different rates of decay appear in the further out turn-off
characteristics of the amplifier. A fast decay rate appears in Region 1, defined as the time
range from 200-260 ns. A slower decay rate is seen in Region 2, defined from
260-550 ns. A linear least squares curve fit is performed for the two regions and is
shown in Figure 3.32. The rate of decay in Region 1 is 2.12 dB/ns compared to the
slower decay rate of 0.06 dB/ns observed in Region 2. The determination of the physical
Figure 3.31. MPI L0203-41 amplifier results at $f_{RF} = 3$ GHz.

Figure 3.32. MPI L0203-41 amplifier turn-off characteristics at $f_{RF} = 3$ GHz.

The phenomenon causing the behavior in these different regions is beyond the scope of this work, although drain lag in the FET is a likely culprit.
The knowledge of the turn-off power characteristics is important to the system designer. Consider an application where the pulse power must dissipate to a level 150 dB below the peak level, 250 ns after the falling edge of the pulse. In this example, the power difference is 146 dB for the MPI amplifier and does not meet the requirement. The other measurement techniques do not reveal this characteristic.

3.14 Summary

A high-dynamic range pulse profile measurement technique is demonstrated. The measurement technique outlined offers a significant advantage over traditional techniques by extending the dynamic range of the measurement as well as allowing for short pulsing conditions. The basis for the improvement stems from adding a pulse coding scheme and coherent integration of multiple pulses to allow for an improvement in measurement SNR. A full description of the system design is presented, with a detailed explanation of the main system elements, including the FPGA, correlation receiver, coding transmitter, and digital receiver.

Measurement results are presented on a typical pulsed power amplifier to prove the validity of this technique on an actual device under fast pulsing conditions. The system achieves a measurement dynamic range of greater than 160 dB. The measurement results are compared to the pulse profile results obtained using the standard methods of a diode detector or peak power meter. This technique offers a significant advantage to the system designer who must characterize the pulse profile of the output power amplifier for use in high-dynamic range systems since the alternative techniques do not sufficiently reveal the behavior of the amplifier.
The system could be further improved if the effects of jitter on the dynamic range could be reduced. A second downconversion stage increases the system complexity, but significantly reduces the effect of jitter in the digitization process due to the lower frequency of operation. Theoretically, even greater sensitivity could be achieved with this alteration. Alternatively, improved clock generation sources with less jitter would also increase the overall system sensitivity.
4. HIGH-EFFICIENCY AMPLIFIER DESIGN

The output power amplifier in a high-dynamic range pulsed system must be pulsed so that the output noise during the receive time does not affect the overall system performance. There are numerous techniques available to provide pulse modulation for an amplifier. Two popular techniques used in FET amplifier designs use a pulsed gate or drain voltage to control the gain of the device. In gate modulation, a constant drain voltage is applied and the gate voltage is transitioned from the saturation region to below pinch-off, effectively turning the device on and off. A similar process is used in drain modulation, except that a steady gate voltage is applied and the drain voltage is transitioned from zero volts to the desired operating voltage. In both cases, additional circuit elements and a control voltage for the modulation are required. These additional elements add to the complexity of the design.

The Class E amplifier provides gain only when an input RF signal is present. Therefore, it is possible to provide high-isolation pulse modulation simply by pulsing the RF input signal. The amplifier provides gain to the signal when the input power is high enough to force the FET into the switch mode. The device provides loss when the input is taken away because the device is statically biased off by the gate voltage. It is easier to generate a pulsed RF signal farther back in the transmitter chain because the power levels are lower and alternative pulse modulation techniques are available. For example, a simple RF switch can act as a pulse modulator. As an added bonus, the amplifier does not dissipate power during the dead time of the pulse. The linear amplifier requires the use of a modulator to provide this behavior. However, the modulator itself will likely dissipate some power and tend to reduce the overall efficiency.
The Class E amplifier is inherently a nonlinear mode of operation. Therefore, any linear modulation schemes that depend on varying the signal envelope, such as amplitude modulation (AM) or quadrature amplitude modulation (QAM) cannot be used directly. A linearization technique can be applied in these situations to restore the envelope of the signal, but with increased circuit complexity [43], [56]. However, constant envelope modulation schemes, such as frequency modulation (FM) or phase shift keying (PSK), can be used without any modifications to the amplifier design.

The design of a high-efficiency amplifier targeted for pulse-mode applications is explored in this section. A GaN HFET is used as the switching device in the amplifier. The design procedure for the input and output networks to achieve high-efficiency operation is illustrated. Simulation results on the amplifier are presented showing the device performance in the nonlinear operating mode. Finally, a drain modulator design is presented which can be used with a linear amplifier design to compare the pulsing behavior for different modes of operation.

4.1 Device Selection

The development of GaN devices is predominantly developed on two types of substrate materials: high-resistivity silicon and high-resistivity silicon carbide. Silicon carbide is very attractive because it has a much higher thermal conductivity, allowing for devices with a higher power density since the operating temperature is potentially lower. However, devices fabricated on high-resistivity silicon substrates have the advantage in material cost and manufacturability. Silicon processing techniques can be used, such as substrate vias, which are difficult and costly on a SiC substrate. Silicon manufacturing is much more mature, offering the possibility of processing on 150 mm wafers while
standard SiC devices are fabricated on a 75 mm or 100 mm wafer. The larger wafers allow a reduced per unit device cost in production quantities.

There are many manufacturers focusing on GaN device production, such as TriQuint Semiconductor, RF Micro Devices (RFMD), Cree, Eudyna, and Nitronex, just to name a few. RFMD and Eudyna are currently selling commercial packaged GaN devices. The packaged device approach is problematic in high-efficiency amplifier design because the devices are typically prematched inside the package to a more suitable impedance for a linear amplifier mode. This prematching eases the impedance transformation required at the fundamental frequency, but causes serious problems when attempting to provide a specific impedance at the harmonic frequencies.

A solution using just the device die is attractive because it allows ultimate freedom in terms of the matching network design. There are no prematching networks to account for and the design can be optimized for the target application. The disadvantage is increased difficulty in working with the devices, including die attach procedures, wirebonding, and stray fingers that tend to crush exposed devices.

A 2 mm GaN HFET device from Nitronex Corporation is selected as the transistor for the Class E amplifier. The device is fabricated in the NRF1 process that uses a silicon substrate. The relevant process characteristics are summarized in Table 4.1 [89]. The cross-section of the GaN HFET device is shown in Figure 4.1 [90]. A photograph of the NRF1-02A 2 mm die is shown in Figure 4.2. The device has a 0.5 μm gate length. The substrate is thinned to 6 mil to allow a substrate via connection from the topside source pads to the backside gold metallization. Therefore, the entire backside of the device can be used as a source connection.
Table 4.1. Nitronex NRF1 GaN process characteristics at room temperature [89].

<table>
<thead>
<tr>
<th>Description</th>
<th>Typical</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two Terminal Off-State Breakdown Voltage</td>
<td>160</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Extrinsic Transconductance</td>
<td>290</td>
<td>mS/mm</td>
</tr>
<tr>
<td>Drain Leakage at $V_{DS} = 100$ V, $V_{GS} = -8$ V</td>
<td>0.2</td>
<td>mA/mm</td>
</tr>
<tr>
<td>Maximum Open Channel Current</td>
<td>830</td>
<td>mA/mm</td>
</tr>
<tr>
<td>Isolation Leakage Current at 8 kV/mm</td>
<td>10</td>
<td>nA/mm</td>
</tr>
<tr>
<td>Ohmic Contact Resistance</td>
<td>0.38</td>
<td>Ohm mm</td>
</tr>
<tr>
<td>Open Channel On Resistance</td>
<td>3</td>
<td>Ohm mm</td>
</tr>
<tr>
<td>Epitaxial Layer Sheet Resistance</td>
<td>490</td>
<td>Ohm/sq</td>
</tr>
<tr>
<td>Pinch-off Voltage</td>
<td>-1.55</td>
<td>V</td>
</tr>
<tr>
<td>Saturated Output Power (28 V and 2.14 GHz)</td>
<td>3.9</td>
<td>W/mm</td>
</tr>
<tr>
<td>Maximum Drain Efficiency (28 V and 2.14 GHz)</td>
<td>62.5</td>
<td>%</td>
</tr>
<tr>
<td>Thin Film Sheet Resistance</td>
<td>20</td>
<td>Ohm/sq</td>
</tr>
<tr>
<td>MIM Capacitance</td>
<td>150</td>
<td>pF/mm$^2$</td>
</tr>
</tbody>
</table>

Figure 4.1. GaN HFET cross-section [90].
4.2 DC Characterization

The DC properties of an active device give the designer an insight into the expected behavior of the device in both DC and RF operating modes. A DC curve tracer is commonly used to measure the DC current-voltage (IV) curves, which are a family of drain current versus drain voltage curves for varying input voltages. In a FET device, the family of curves is for different gate voltages. An example family of IV curves is shown in Figure 4.3, where each trace represents the IV characteristics for a different gate voltage.
The measurement of DC IV curves is problematic for high-power devices due to thermal effects. The device will self-heat in the high power dissipation regions on the IV plane (high drain current and drain voltage). The IV curves appear to “droop” or “sag” because the drain current in a FET device decreases with temperature for a given gate bias.

It is shown that IV measurements made under short pulse conditions are useful for several reasons [91]-[94]. Pulsed IV measurements address the self-heating issue because the device is only operated for a very small percentage of time, reducing the average operating temperature. The duty factor can be held to less than 1 % in modern pulsed IV measurement systems. Pulsed IV measurements also allow measuring the high power dissipation regions of the IV curves where the device would typically self-destruct in a static measurement.

Pulsed IV measurements can also give insight into the deep level or trapping behavior of a device. These traps influence the microwave power performance of transistors through the formation of quasi-static charge distributions, commonly found on the wafer surface or in the buffer layers under the channel [74]. This parasitic charge serves to restrict the drain voltage and current excursions, ultimately limiting the high-frequency power output. It is also shown that the associated time constant of the electron transfer through these deep level traps is much slower than in regular microwave amplifier operation [94].

The pulsed IV measurements allow setting a quiescent bias that establishes a steady-state trap population, which generally cannot follow short pulses or high-frequency signals. Therefore, varying the quiescent bias point can provide insight into
the device trapping behavior. The measurement of pulsed IV curves can lead to a more accurate prediction of the high-frequency characteristics of the device [95].

The Auriga AU4550 pulsed IV measurement system is used to measure the pulsed IV curves of the Nitronex NRF1-02A 2 mm GaN HFET die. The die includes a ground-signal-ground (GSG) pad configuration on the gate side, but only a single drain pad. The device must be probeable by a GSG probe to allow simultaneous measurement of the IV curves in addition to calibrated S-parameters.

The solution is to use an adapter board that performs a coplanar waveguide to microstrip transition. The Jmicro Technology ProbePoint adapter is a thin film network (TFN) that has a GSG probable CPW to microstrip transition. An example representation of the ProbePoint adapter board is shown in Figure 4.4. Jmicro also supplies a calibration substrate that allows a network analyzer calibration to the reference plane at the end of the microstrip line.

The NRF1-02A die are attached to a copper tungsten (CuW) heat spreader with Diemat DM6030Hk epoxy. The Diemat material is a silver-loaded epoxy with a high electrical and thermal conductivity. The high thermal conductivity is important to

Figure 4.4. Jmicro Technology Probe Point adapter.
provide a low thermal resistance to the heat spreader to reduce the temperature of the device in testing. The ProbePoint 0503 adapters are 5 mil thick, which closely matches the 6 mil thickness of the die, reducing the height difference of the wire bond. The RF performance of the interface between the adapter boards and the die is important. Therefore, the die is connected to the adapters with a 3 mil wide ribbon with wedge bonds to reduce the effective inductance of the bond. A photograph of the assembled die test fixture is shown in Figure 4.5.

The pulsed IV measurement system allows choosing an arbitrary quiescent point (Q-point) for the measurements. The Q-point is the voltage condition where the device is maintained for the duration of the time interval. The Q-point should be selected in a region where there is minimal power dissipation in the device to keep an isothermal

![Figure 4.5. Assembled die test fixture (a) full view on CuW carrier and (b) zoomed view of single die.](image-url)
measurement. The device is pulsed to a non-quiescent point (NQ-point) to measure the particular location on the IV curve. An example of the aperture selection screen is given in Figure 4.6 that shows the location of the Q- and NQ-point.

Consider a pulsed IV curve measurement as shown in Figure 4.7. In one case, the drain quiescent point is at the origin, and the voltage pulses from the origin to the measurement point. Alternatively, a quiescent point other than the origin can be chosen. The other case uses a quiescent drain bias of 28 V and pulses from this point to the measurement points. These two different quiescent bias points may exhibit a different charge trapping behavior, which can affect the measured IV curves.
The Nitronex NRF1-02A devices are measured in a pulsed configuration with a pulse width of 5 μs and a duty factor of 0.1 %. These parameters translate to a PRI = 5 ms or PRF = 200 Hz. The gate and drain voltages are both pulsed simultaneously on the device. Measurements are taken using two different quiescent points for the device. The measurements for the device pulsed with a Q-point of $V_{gQ} = -1.5$ V and $V_{dQ} = 0$ V are shown in Figure 4.8. The measurements for the device pulsed with a Q-point of $V_{gQ} = -1.5$ V and $V_{dQ} = 28$ V are shown in Figure 4.9. A different behavior is observed in the shape of the IV curves near the knee region for the two cases. The small dip after the knee in the $V_{dQ} = 0$ V case is likely caused by trapping effects within the device. The accuracy of the gate current measured for the device is limited by the measurement system. A similar gate current is obtained even if a device is not present, which means that the actual gate current of the device is below the measurement limits for the pulsed IV system.
The devices exhibit a very soft knee region compared to GaAs devices. The knee voltage of a FET is the voltage at which the particular IV curve transitions from the linear to the saturation region. In the linear region, $I_{ds}$ depends on both $V_{gs}$ and $V_{ds}$. In the saturation region, $I_{ds}$ depends primarily on $V_{gs}$ and not on $V_{ds}$. A lower knee voltage allows a greater RF voltage swing for a given drain bias, resulting in a higher drain efficiency [96]. The Nitronex device is intended primarily for linear applications with a nominal drain bias of 28 V. In this case, the soft knee region does not have a large impact on efficiency. However, for lower bias voltages, the knee voltage is a larger percentage of the overall bias and has a greater effect on efficiency.

Figure 4.8. Pulsed IV measurements for $V_{gQ} = -1.5$ V and $V_{dQ} = 0$ V (a) IV curves and (b) gate current.

Figure 4.9. Pulsed IV measurements for $V_{gQ} = -1.5$ V and $V_{dQ} = 28$ V (a) IV curves and (b) gate current.
4.3 RF Characterization

The RF characteristics of the device are obtained by measuring the S-parameters. The measurement of S-parameters is typically only considered for continuous wave devices. However, measuring high-power amplifiers in a CW mode is difficult for the reasons already stated. Therefore, it is desirable to perform S-parameter measurements in a pulsed mode. An Agilent PNA-X N5242A network analyzer with the appropriate pulsing options is used to measure the pulsed S-parameters of the device. The pulsing options add pulse modulation to the RF stimulus on both ports as well as a pulsed receiver gate in the analyzer.

There are two pulsing modes available on the PNA-X: narrowband and wideband detection [69]. The narrowband detection technique requires very specific pulse repetition frequencies so that its spectral nulling technique is applicable. The dynamic range also degrades as the duty factor is reduced. These factors led to the decision to use the wideband detection technique. This technique is useful for pulses that are greater than 1 μs to allow the majority of the spectral energy to fit within the bandwidth of the receiver. A trigger signal is used to synchronize the pulse gates of the PNA-X with the DC pulsing of the Auriga 4550. The network analyzer samples the data when it receives a pulse trigger, and the length of the measurement gate must be less than the pulse width as shown in Figure 4.10.

The S-parameters of the device are measured at each of the locations measured on the IV curves. The network analyzer is configured with a frequency range of 10 MHz to 20 GHz and 201 measurement points. An example of the measured S-parameters for two different gate voltages is shown in Figure 4.11. Each curve represents the measurement
at a different drain voltage, ranging from 0 V to 40 V. The device exhibits a large amount of low frequency gain, as seen in the $S_{21}$ plot of Figure 4.11(b). The low frequency gain of HEMT devices can cause low frequency instability issues in a final amplifier design.

### 4.4 Bias Selection

The selection of appropriate DC bias voltages is important in any amplifier design. The gate bias voltage in a Class E amplifier is commonly set near the pinch-off
voltage so the device is on for 50% of the time. However, there are additional considerations when targeting the Class E amplifier for pulse-mode applications.

It is important that the device does not provide gain during the dead time of the input pulse so that the noise level is not affected during this time. The gain of the device ($S_{21}$) is plotted versus the DC gate voltage in Figure 4.12 for $V_d = 16$ V. It is also important that the amplifier shut off as quickly as possible when the input RF pulse is removed. These two conditions require that the gate voltage be set as negative as possible so the device is fully pinched off. However, setting the gate voltage below pinch-off reduces the overall efficiency of the amplifier. It is clear the pulse-mode requirements are in competition with the efficiency parameters of the device. The pinch-off voltage for the device is approximately -1.55 V. A gate bias voltage of $V_g = -1.7$ V is selected to ensure the device is pinched-off as well as to provide a minimal impact on achievable efficiency.

4.5 Load Pull

The pulsed IV and S-parameter measurements give a look into small signal performance of the device, but they do not provide the full story of the device
performance under large signal drive conditions. The technique of using source or load pull is commonly used to determine the optimum termination impedance to present to the device [4]. A load pull involves using a tuner to vary the impedance at the device and measuring the performance at each impedance point to generate a set of contours. The output power, gain, and efficiency are common parameters measured while performing a load pull. An example of an automated load pull tuner is shown in Figure 4.13.

Traditional load pull systems provide tuning for a fundamental frequency of operation. The impedance presented to the harmonics is not controlled and may vary wildly over the fundamental impedance range measured. The device performance could be affected by the harmonic termination. A change in performance may be incorrectly attributed to the fundamental tuning, when it is the harmonic impedance variation that causes the change in performance.

A traditional harmonic load pull system is costly, and calibration of the system is complex because a separate tuner is required for each harmonic. Focus Microwaves has invented an automated tuner that uses three separate carriages in one tuner assembly, allowing independent tuning of the fundamental frequency and the second and third harmonics. The Focus Microwaves MPT-1818-TC 2-18 GHz multiharmonic tuner is used on the load side to provide harmonic load pull measurements of the device.

Figure 4.13. Example automated load pull tuner.

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The load pull setup requires the use of an input (source) and output (load) tuner as well as other blocks to couple the RF power into the measurement equipment. The block diagram of the measurement setup as seen in the Focus Microwaves Load Pull Explorer software is shown in Figure 4.14. A picture of the measurement setup is shown in Figure 4.15.

The device is biased in pinch-off at $V_{gs} = -1.7$ V and the drain is biased at $V_{ds} = 15$ V for the load pull measurements. A coarse source pull is performed to determine the approximate location of maximum gain. A denser source pull is then
performed to locate a more exact location. The source pull results are shown in Figure 4.16 and Figure 4.17. The coarse source pull results in Figure 4.16 show that the contours for gain and maximum output power are very similar. An optimum search is performed in a smaller region of the Smith chart as seen in Figure 4.17. The colored contours for gain and output power are shown. A source reflection coefficient of $\Gamma_s = 0.85 \angle 160^\circ$ is used for the remaining load pull measurements.

![Figure 4.16. Source pull measurement results: (a) gain and output power contours and (b) gain color contours.](image1)

![Figure 4.17. Source pull optimum search results: (a) gain and (b) output power.](image2)
A course fundamental load pull is then performed on the device, keeping the second and third harmonic fixed at $\Gamma = 0.5\angle 0$. The contours of the fundamental load pull are given in Figure 4.18. A denser load pull is performed on a smaller region of the Smith chart as shown in Figure 4.19. The contours for output power and PAE are shown. The optimum fundamental reflection coefficient for PAE is determined to be $\Gamma_1 = 0.55\angle 133^\circ$.

A second harmonic load pull is performed by keeping the fundamental reflection coefficient fixed at $\Gamma_1$ and the third harmonic at $\Gamma_3 = 0.5\angle 0$, then varying the second harmonic around the Smith chart. The results from the second harmonic load pull are shown in Figure 4.20. The optimum second harmonic termination is on the open circuit side of the Smith chart. The optimum termination is measured as $\Gamma_2 = 0.8\angle 0$, but the PAE is consistent for a broad range of impedances on the open circuit side of the Smith chart. The magnitude of the reflection coefficient is limited by the loss in the test setup and may not be the global optimum for the device. Finally, a load pull is performed at

![Figure 4.18. Fundamental coarse load pull measurement results for PAE.](image)
the third harmonic by fixing the fundamental and second harmonic at their optimum locations while the third harmonic impedance is varied. The results from the third harmonic load pull are given in Figure 4.21. The optimum reflection coefficient is determined to be $\Gamma_3 = 0.75\angle75^\circ$. The magnitude of the reflection coefficient is again limited by loss in the test configuration. The optimum fundamental impedances remain relatively unchanged after varying the harmonic terminations.

Figure 4.19. Fundamental load pull optimum search: (a) PAE and output power contours, (b) output power color contours, and (c) PAE color contours.
4.6 Modeling Effort

An initial attempt is made at modeling the HFET device using the Transistor Parameter Scalable (TOPAS) model by IMST [97]. The model requires measuring the device IV curves and S-parameters on a rectangular sampling grid of bias points. The model extraction software uses these data to extract a bias dependent intrinsic device representation and the extrinsic parasitics, realizing a fully functional nonlinear model.
The pulsed IV and S-parameter measurements for 1216 bias locations are fed into the TOPAS extraction software. The extraction and optimization process is followed to generate a .SIM model file. The small signal fit is quite good for all bias conditions, and the results for a single bias location are shown in Figure 4.22. However, there are significant problems when using the model in a nonlinear harmonic balance simulator. The harmonic balance simulator in ADS is used to simulate the device in a nonlinear power sweep. Unfortunately, a nonlinear simulation is not achievable with the extracted TOPAS model. The simulator could not achieve DC convergence for any of the bias points used. Ultimately, the TOPAS model is abandoned in favor of the model provided by Nitronex.

The Nitronex model is based on an Angelov model with the equivalent circuit given in Figure 4.23 [98], [99]. The model is extracted on a device similar to the one used in this work, except that it included a direct CPW probable structure for the gate and

Figure 4.22. Example TOPAS extraction at a single bias point.
drain. The model extraction process is detailed in [99] and follows a procedure similar to the TOPAS model extraction. The Nitronex team also performed measurements at elevated temperatures to include self-heating effects in the model.

The self-heating in the model is seen in the simulated device IV curves. A standard CW IV curve measurement is performed by sweeping the drain voltage for a set of gate voltages. The pulsed IV curves are created by using a pulsed gate and drain voltage similar to the pulsed IV measurement, with an example given in Figure 4.24. A PRI of 4 μs with a 2 % duty factor is used. The quiescent operating point is $V_{gQ} = -1.5 \, \text{V}$ and $V_{dQ} = 0 \, \text{V}$. The reported current is an average over 25 % of the current pulse since ringing is present due to the Gibbs phenomenon. The CW and pulsed IV curves are shown in Figure 4.25. The CW curves experience considerable droop as the device heats while the pulsed curves do not.
4.7 Amplifier Design Considerations

The first stage in the amplifier design involves several considerations. The first detail is the selection of a suitable matching network strategy using either lumped elements or a distributed matching network topology. The available $Q$ of lumped element components in the S-band limits the efficiency of the amplifier. Therefore, a
distributed matching network topology is selected. Microstrip lines are used due to their ease of construction and integration with the active device.

The next step is to select a suitable substrate for fabricating the amplifier. It is convenient to connect the die directly to the microstrip matching networks with a minimum length wirebond, since this configuration results in the least amount of connection inductance and loss. The surface of the die should be at the same height as the top of the substrate to minimize the wirebond length. It is possible to mill out an area in the substrate to insert the die so it is recessed. The backside of the die must make contact with the ground plane to provide the grounded source connection. Therefore, the substrate height must be similar to the thickness of the die. Alternatively, a conductive slug could be used, but a manufacturer could not be located for the dimensions required.

A Rogers Corporation Duroid 5880 substrate with a substrate height of 5 mil is selected. The Duroid 5880 material is chosen since the relative dielectric constant of \( \varepsilon_r = 2.2 \) results in a 50 ohm transmission line that has a manufacturable trace width of 15 mil. A higher dielectric constant material, such as Duroid 6010 (\( \varepsilon_r = 10.2 \)), requires a trace width of approximately 4 mil for a 50 ohm line. The manufacturing process used requires a minimum line width of 8 mil for producible products.

### 4.8 Stability Network Design

The stability of a linear, two-port device can be assessed using the familiar Rollet stability factor \( K \) and the auxiliary condition \( \Delta \) defined as

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}. \tag{4.8.1}
\]

\[
\Delta = S_{11}S_{22} - S_{12}S_{21}
\]
The device is said to be unconditionally stable if $K > 1$ and $|\Delta| < 1$ [100]. It is cumbersome to validate two separate conditions to check stability.

An alternative metric, termed the geometric stability factor, is used which computes the distance from the center of the Smith chart to the nearest unstable point [101]. The geometric stability factor ($\mu$), referenced to the source or load, is defined as

$$
\begin{align*}
\mu_1 &= \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{21} S_{12}|} \quad (\text{load}) \\
\mu_2 &= \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \Delta| + |S_{21} S_{12}|} \quad (\text{source})
\end{align*}
$$

where $\Delta = S_{11} S_{22} - S_{12} S_{21}$ and the operator $^*$ indicates the complex conjugate. The necessary condition for unconditional stability of the two-port network is $\mu > 1$.

It must be noted that both of these stability calculations are applicable to linear, two-port devices only. The Class E mode is inherently a nonlinear mode of operation. It is unclear if a classical stability factor approach has any meaning to the true stability of the device as it operates in the highly nonlinear switch mode [102].

The base device is extremely unstable, which is noted by low-frequency oscillations detected during the source pull for some regions of the Smith chart. In particular, the gain of the device is high at low frequencies, adding to the problem. It is clear that some stability network must be applied to the device to prevent the low frequency oscillation without providing too much loss to degrade the amplifier performance.
A linear stability analysis is performed on the device in Microwave Office using the Angelov model. A stability network targeted at the low-frequency behavior is attractive because it does not affect the higher frequency operation of the device as much. A network consisting of a series gate resistor with a shunt resistor in series with an inductor is selected, as shown in Figure 4.26. This network provides loss at low frequencies to help stabilize the device, as well as a series gate resistor to increase the stability over all frequencies. The geometric stability factor and stability circles are shown in Figure 4.27 for the raw device and the device with stabilization network. The device is not unconditionally stable in the classical sense, but the network does keep the device from experiencing any detectable oscillations during testing.

![Figure 4.26. Amplifier stability network.](image-url)
4.9 Output Matching Network Design

The design of the Class E amplifier begins by examining the classical design equations, then using the harmonic balance simulator to optimize the results. It is shown in [2] that the approximate load resistance $R$ to optimize Class E behavior is

$$R = 0.58 \left( \frac{V_{dd} - V_{ds, sat}}{P_E} \right)^2,$$

where $V_{dd}$ is the drain voltage, $V_{ds, sat}$ is the saturated drain to source voltage, and $P_E$ is the output power of the device. The conditions $V_{dd} = 15$ V, $V_{ds, sat} = 2.5$ V, and $P_E = 32.5$ dBm yield an ideal load resistance of approximately 40 ohm for the Nitronex NRF1-02A device. The classical Class E design equations also provide a relationship between the load impedance $Z_L$ and the output reactance $X_{out}$ of the device, given by
The output reactance of the device is set primarily by the parasitic capacitance from the drain to the source, \( C_{ds} \). The value of the parasitic output capacitance is obtained from the admittance parameters (Y-parameters) of the intrinsic transistor simulated using the Angelov2 device model [103]. The parasitic drain to source capacitance is calculated as

\[
C_{ds} = \frac{\text{Im}\{Y_{22}\} + \text{Im}\{Y_{12}\}}{\omega},
\]

where \( Y_{12} \) and \( Y_{22} \) are the intrinsic device Y-parameters and \( \omega \) is the frequency of the Y-parameter. The value of the drain-source capacitance calculated using the ADS model is \( C_{ds} = 0.57 \) pF. The load impedance is calculated at 3 GHz using \( \text{C}_{\text{out}} = C_{ds} \) and (4.9.2), yielding

\[
Z_L = \left(0.183 + j0.211\right) |X_{\text{out}}| = \left(0.183 + j0.211\right) \left| \frac{1}{j2\pi fC_{\text{out}}} \right| = 17 + j19.6 \Omega
\]

This load impedance is converted to a reflection coefficient in a \( Z_o = 50 \) ohm system as

\[
\Gamma = \left( \frac{Z_L - Z_o}{Z_L + Z_o} \right),
\]

\[
= 0.55 \angle 133^\circ
\]
and compares favorably with the optimum fundamental frequency reflection coefficient determined from load pull results described in Section 4.5.

A distributed matching network topology using microstrip lines is considered since the available $Q$ of lumped elements at this frequency limits the performance of the amplifier. The Class E design requires setting the fundamental impedance of the device and controlling the impedance presented to the harmonics. A basic topology, as shown in Figure 4.28, uses a high-impedance, quarter-wavelength stub at the second and third harmonics to control the phase of the harmonic frequencies. The high-impedance stub provides minimal interaction with the fundamental match. The distance of the stub to the input plane controls the phase of the harmonic impedance. The fundamental impedance is set using the length $l_4$ of the fundamental stub and the combination of the series lengths $l_1-l_3$.

Figure 4.28. Amplifier multiharmonic matching network topology.
Two separate amplifier designs are considered in this work. One amplifier design attempts to set the source and load impedances to values obtained from load pull. This amplifier is given the designation JTB0007A. The second amplifier uses the nonlinear model and the harmonic balance simulator and optimizer to obtain the optimal matching networks for the input and output. This amplifier is given the designation JTB0008A.

The network that approximates the load pull results is defined in the Rev. A output matching network design. The matching network topology shown in Figure 4.28 is created using microstrip elements in Microwave Office (MWO). The fundamental stub is RF grounded with bypass capacitors so that it can be used to supply the drain bias to the device. The widths of the fundamental lines are set to 15 mil, which translates to an approximate 50 \( \Omega \) characteristic impedance. A schematic of the matching network is shown in Figure 4.29. The series and shunt line lengths are set as variables and optimized to achieve the desired reflection coefficient at the DUT port. The values used in the matching network are summarized in Table 4.2, and a pictorial representation of the layout is given in Figure 4.30. The simulation results of the matching network for a fundamental frequency of 3 GHz are shown in Figure 4.31. The reflection coefficient at the fundamental frequency closely matches the load pull results, while the harmonics are terminated in an approximate open circuit.

A second output network is designed by simultaneously optimizing the input and output matching networks for the amplifier parameters of output power and PAE. The optimization is performed on the full amplifier schematic so that all of the parameters in the matching networks are varied to achieve an optimal design. The values obtained
from the global optimization are used in output matching network Rev. C design and are summarized in Table 4.2. A pictorial representation of the layout is shown in Figure 4.32.

The simulation results are given in Figure 4.33. In this case, the fundamental frequency termination remains approximately the same, but the phase of the harmonic terminations is vastly different. The position of the second and the third harmonic terminations cause a sharpening of the voltage and current waveforms seen at the drain terminal of the HFET, thereby causing an increase in overall simulated efficiency.

![Amplifier output matching network schematic.](image)

**Figure 4.29.** Amplifier output matching network schematic.

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<th>Parameter</th>
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<th>Rev C</th>
<th>Unit</th>
</tr>
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<td>mil</td>
</tr>
<tr>
<td>LSeries2</td>
<td>35.5</td>
<td>306.0</td>
<td>mil</td>
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<td>mil</td>
</tr>
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<td>mil</td>
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<td>mil</td>
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<td>WStubF1</td>
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<td>15.0</td>
<td>mil</td>
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</table>
Figure 4.30. Amplifier output network Rev. A layout.

Figure 4.31. Amplifier output matching network Rev. A simulation results with a fundamental frequency of 3 GHz.
Figure 4.32. Amplifier output network Rev. C.

Figure 4.33. Amplifier output matching network Rev. C simulation results with a fundamental frequency of 3 GHz.
4.10 Input Matching Network Design

The input matching network design follows a similar procedure as the design of the output matching network. There are two additional considerations in the design of the input network. The input matching network must include the stability network described in Section 4.8. The reflection coefficient required by active device results in a very low impedance compared to 50 Ω. This difference increases the difficulty of the matching network. The input matching network is designed to provide the impedance matching in a 30 Ω environment, and then the input is transformed to a 50 Ω environment for testing purposes. A microstrip line width of approximately 30 mil results in a 30 Ω transmission line on the 5 mil Duroid 5880 material.

The harmonic matching network topology shown in Figure 4.28 is also used for the input network. The series resistor required by the stability network is included next to the series DC blocking capacitor. The shunt resistor is included in series with the fundamental matching stub. RF bypass capacitors are included on the end of the fundamental stub to create a short-circuited line, similar to the output matching network. The DC gate bias is also fed through the fundamental stub. The GaN HFET draws negligible gate current, so the inclusion of the 110 Ω in series with the DC bias does not affect the gate voltage seen at the device. The schematic of the input matching network is shown in Figure 4.34.

Two designs of the input matching network are considered. The first matching network is optimized in a harmonic balance simulation with the Rev. A output matching network that simulates the optimum load pull results. In this case, parameters of the input network are varied and the geometry of the output network is fixed during the
optimization. The resultant parameters are used in the input matching network Rev. B design. The final design parameters are summarized in Table 4.3. The simulation results for this design are given in Figure 4.35.

A second matching network design is considered by simultaneously optimizing the input and output matching networks as described in Section 4.9. The results of this optimization are incorporated into the input matching network Rev. C design. The

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>Rev C</th>
<th>Unit</th>
</tr>
</thead>
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<td>mil</td>
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<tr>
<td>L.Series5</td>
<td>66.5</td>
<td>41.5</td>
<td>mil</td>
</tr>
<tr>
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<td>mil</td>
</tr>
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<td>L.StubF3</td>
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<td>236.5</td>
<td>mil</td>
</tr>
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<td>mil</td>
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<td>mil</td>
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<td>10.0</td>
<td>mil</td>
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<td>W.StubF1</td>
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<td>mil</td>
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</table>
parameters for this design are summarized in Table 4.3. The parameters for this matching network are very similar to the previous design. A pictorial representation of the matching network is shown in Figure 4.36. The simulation results for the Rev. C network are given in Figure 4.37.

![Figure 4.35. Amplifier input matching network Rev. B simulation results with a fundamental frequency of 3 GHz.](image)

![Figure 4.36. Amplifier input matching network Rev. C.](image)
4.11 Simulation Results

The input and output matching networks are combined with the device model to create a circuit representation of the amplifier. The amplifier is initially designed in MWO at a fixed frequency of 3 GHz. The device is statically biased at $V_{gs} = -1.7$ V and $V_{ds} = 15$ V. The performance of the fabricated amplifier differed considerably from the simulation results in MWO, as described in the next section.

A similar simulation setup is constructed in ADS, as shown in Figure 4.38. The harmonic balance simulator is used to compute the large-signal power and PAE performance of the device. A large-signal S-parameter (LSSP) simulation is used to compute the gain and return loss of the device in a nonlinear operating mode. A small amount of attenuation is added at the input and output of the amplifier to simulate the loss of the SMA connectors on the amplifier test board.
The amplifier is simulated using a swept input power over the range 0-30 dBm. The frequency of the input is swept over the range from 2.5-3.1 GHz to show the performance of the device over a broader range of frequencies. The simulation results for gain, output power, PAE, and input reflection coefficient are given in Figures 4.39-4.42, respectively. The maximum power and PAE for the device versus frequency is plotted in Figure 4.43.

The initial design created in MWO shows a much better PAE performance at 3 GHz. Additionally, the peak PAE occurs at a reduced input power level of 21 dBm. The design is ported to ADS to perform the same simulations to validate the performance after a discrepancy was discovered between the MWO simulation and measurement results.
Figure 4.39. JTB0008A gain simulation results.

Figure 4.40. JTB0008A output power simulation results.
Figure 4.41. JTB0008A PAE simulation results.

Figure 4.42. JTB0008A input reflection coefficient simulation results.
The ADS simulations show a different behavior than the MWO simulations for the amplifier designs. The maximum output power occurs near 2.8 GHz. The PAE performance is consistent across the 2.8-2.9 GHz frequency range. However, the PAE performance drops off considerably at 3 GHz, the target design frequency. The large discrepancy between the two different simulations is observed in the input match behavior of the amplifier. It appears that both MWO and ADS do not accurately predict
the input matching conditions for the nonlinear operating mode. However, the ADS Angelov2 model is much closer to reality because it more accurately predicts the swept power behavior of the device, shown in Figure 4.44. The peak in PAE occurs at a higher input power level of approximately 25 dBm in the ADS simulation results. This result more closely matches the measured amplifier performance. Unfortunately, the ADS simulations were not performed until after the designs were fabricated. Therefore, it was not possible to incorporate any design changes onto the boards to tune the amplifiers to a higher frequency.

The amplifiers perform reasonably well at the lower frequency of operation and provide useful results for applications in high-dynamic range, pulse-mode systems. The HDRPPM system is capable of measuring devices within the S-band, so there are no issues with characterizing the devices at the slightly lower frequency of operation. The full suite of measurement results for the amplifiers and a comparison to the simulated results is treated in Section 5.

4.12 Amplifier Fabrication

The two amplifier designs are fabricated on Duroid 5880 material with a milled hole for the die. The physical dimensions of the test boards are 3.3 in x 2.0 in. A photograph of the fabricated test boards before assembly is shown in Figure 4.45. The amplifier circuit requires an assortment of discrete parts, such as blocking and bypass capacitors and the resistors in the input stability network. SMA connectors are used to provide the RF and DC interface to the test board. The assembled amplifier test boards are shown in Figure 4.46. The GaN die is attached using the high thermal conductivity DM6030Hk epoxy. A zoomed view of the die attach area is shown in Figure 4.47.
Figure 4.45. Amplifier boards before assembly: (a) JTB0007A and (b) JTB0008A.

Figure 4.46. Assembled amplifier test boards: (a) JTB0007A and (b) JTB0008A.
4.13 Drain Modulator Design

The Class E amplifiers designed in this work are also compared to a linear operating mode utilizing the same base GaN device. An amplifier biased at a Class A operating point provides linear gain to input signals with a power level below its input compression point. Therefore, for a pulsed RF input signal, the thermal noise is amplified during the dead time of the input pulse. Additionally, the amplifier is dissipating power during this time. The power dissipation in the amplifier creates a thermal management problem.

The solution to these two problems is to introduce a drain modulator onto the linear amplifier. The drain modulator pulses the drain voltage from 0 V to 15 V, matching the bias voltage used for the Class E amplifier. The amplifier does not have gain when the drain voltage is zero. Additionally, the amplifier does not dissipate any power when the drain voltage is off, reducing the average temperature of the device.
A fast drain modulator that supports the required voltage range is not a simple design. A single MOSFET configured as a switch in the drain path (high side) of the amplifier is not sufficient. In the high-side configuration, there is no element to pull charge out of the device as it is turning off. Therefore, the turn-off characteristics of the pulse are significantly degraded.

A totem-pole configuration allows the drain voltage to be switched on quickly and provides a low-side device to pull charge out of the amplifier HFET. The International Rectifier IRF7343 provides an n- and p-channel MOSFET in a single package. The input gate capacitance is relatively low for this device (~700 pF), which allows for a faster operation when compared to other MOSFETs with similar breakdown voltages. A simulation of the input gate voltages required to create a suitable output voltage pulse is shown in Figure 4.48.

![Figure 4.48. Drain modulator simulation results.](image)
A laboratory pulse generator, such as the Agilent 81110, can generate a pulse with a voltage compatible with the requirements, but the outputs cannot source enough current to overcome the input capacitance of the MOSFETs. A suitable voltage driver is required to interface the MOSFETs with a standard pulse generator. The International Rectifier IR2110 is a high-power, high- and low-side MOSFET driver. It is intended for very high-voltage MOSFET switching applications. However, it can also serve as a suitable driver for translating a CMOS 3 V input logic signal to the voltages required by the MOSFETs. The schematic of the full drain modulator is shown in Figure 4.49. The design is fabricated on a standard FR4 material as shown in Figure 4.50. The output pulse from the drain modulator that is provided to the amplifier test board is shown in Figure 4.51.

Figure 4.49. Drain modulator schematic.
Figure 4.50. Assembled drain modulator board.

Figure 4.51. Drain modulator test results.
5. AMPLIFIER MEASUREMENT RESULTS

The proof-of-concept Class E amplifier designs are presented in the previous section. The performance of the amplifier designs is validated in this section. The Class E amplifiers are first tested in a CW operation mode to verify the correct performance. Next, the devices are tested in a pulsed mode to verify that the Class E mode creates a high on/off isolation pulse. The drain modulator is added to the Class E amplifier design to improve the Class E amplifier pulse performance. Finally, the designs are tested in a linear operating mode to compare with the pulsed Class E performance. The amplifiers are tested using the high-dynamic range pulse profile measurement system to examine the pulse profile of the amplifiers over different bias and operating frequency conditions.

5.1 Continuous Wave Class E Amplifier Results

The fabricated proof-of-concept Class E amplifiers are tested in a continuous-wave mode to verify that the devices are functional. The important amplifier characteristics measured are gain, output power, PAE, and return loss. The block diagram of the test setup used in the CW amplifier testing is shown in Figure 5.1. A photograph of the actual test setup is shown in Figure 5.2.

![Figure 5.1. CW class E amplifier testing block diagram.](image-url)
A pair of directional couplers is used on the input side of the DUT to separate the forward and reverse power. An Agilent N1912A power meter is used to measure the power at the coupled ports of the directional couplers. The actual power at the DUT reference plane is calculated by compensating for the directional coupler losses. The reflection coefficient is calculated as the ratio of the reverse power to the forward power. The output power of the DUT is measured by another Agilent N1912A power meter on the through path of a direction coupler. The coupled port is connected to a spectrum analyzer to measure the power at the harmonics and to detect any spurious oscillations. The gate and drain bias to the DUT is supplied by an Agilent N6705A power supply. The sense lines of the power supply are attached at the SMA connector interface so that the applied voltages are referenced to the DUT test fixture. The gate and drain DC current is measured using the internal capabilities of the power supply that has an accuracy specified at 0.1% + 4 mA.
A swept input power measurement is performed across a range of frequencies to accurately characterize the device performance. The input network includes a power amplifier to increase the power from the signal generator. A first pass power sweep is performed to characterize the power setting of the signal generator versus the input power delivered to the DUT to account for the return loss variation of the DUT. This calibration step allows the input power to the DUT to be within 0.1 dB of the desired setting.

5.1.1 JTB0007A

The initial test results on JTB0007A are less than spectacular at 3 GHz. The plot of the measured maximum output power and PAE is shown in Figure 5.3. The output power drops considerably with increasing frequencies, and the PAE follows a similar pattern. It is clear that the amplifier is tuned incorrectly due to the incorrect simulation results obtained using the Angelov model in MWO.

The incorrect amplifier results primarily stem from an incorrect input match. The input reflection coefficient is plotted in Figure 5.4. The input match near 3 GHz is quite good for low power conditions. The input match at 3 GHz becomes steadily worse as input power is increased, while the match becomes better at the frequency range near 2.6 GHz. It appears that the MWO model is correctly predicting the small signal performance of the device, evidenced by the accurate match for low input power levels. However, the MWO model degrades as the power level is increased and the device enters a nonlinear operating mode. The MWO simulation predicts a performance similar to the 2.6 GHz case, but at a frequency of 3 GHz.
5.1.2 JTB0007A Mod 11

The initial parameter values of the input and output networks used in the JTB0007A design missed the target frequency of operation. The base design is resimulated in ADS to discover the necessary changes to increase the performance at higher frequencies. The capability to make changes to the existing board is limited. The only changes that are achievable are shortening or lengthening the stubs. The series line lengths cannot be easily modified without fabricating a new board.

The parameters for the stub lengths are optimized in the harmonic balance simulation and a suitable tradeoff is implemented. The changes to design are implemented in stages to validate the performance, and the final values are given in Table 5.1. The final implementation of the design changes is dubbed JTB0007A Mod 11.
Table 5.1. JTB0007A Mod 11 modified parameters.

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<td>mil</td>
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<tr>
<td>Input</td>
<td>LStubF1</td>
<td>239.5</td>
<td>mil</td>
</tr>
<tr>
<td>Input</td>
<td>LStubMatch</td>
<td>50.0</td>
<td>mil</td>
</tr>
<tr>
<td>Output</td>
<td>LStubF3</td>
<td>200.0</td>
<td>mil</td>
</tr>
<tr>
<td>Output</td>
<td>LStubF2</td>
<td>310.0</td>
<td>mil</td>
</tr>
</tbody>
</table>

This updated design is tested using the setup detailed in Figure 5.1. The gain, output power, PAE, and input reflection coefficient are shown in Figures 5.5-5.8, respectively. The output power and gain are increased at the higher frequencies. The maximum PAE is also shifted higher in frequency. The return loss characteristic is significantly improved in the higher frequency region. The original design showed that the return loss was best near 2.6 GHz at high drive levels. The updated design is more optimal at 2.95 GHz. The tuning using only the open-circuit stubs provides some improvement in performance. Additional improvement is achievable if the series lengths are also tuned.

The maximum power and PAE is plotted in Figure 5.9. This representation of the data also shows that the frequency range is shifted higher, and even better results could be achieved with a new layout to optimize the series line lengths. A summary of the swept input power device performance at a specific frequency is shown in Figure 5.10. These plots show a slice of the data represented in the surface plots. The power at the second and third harmonics are reflected back into the device quite well, exhibited by the low harmonic power levels seen at the output.
Figure 5.5. JTB0007A Mod 11 CW class E mode gain.

Figure 5.6. JTB0007A Mod 11 CW class E mode output power.
Figure 5.7. JTB0007A Mod 11 CW class E mode PAE.

Figure 5.8. JTB0007A Mod 11 CW class E mode input reflection coefficient.
Figure 5.9. JTB0007A Mod 11 CW class E mode maximum output power and PAE versus frequency

Figure 5.10. JTB0007A Mod 11 CW class E mode swept input power response at (a) $f_1 = 2.8$ GHz, (b) $f_1 = 2.9$ GHz, (c) $f_1 = 2.95$ GHz, and (d) $f_1 = 3.0$ GHz. The variables $f_2$ and $f_3$ denote the second and third harmonics.
5.1.3 JTB0008A

The JTB0008A is initially designed using MWO. Therefore, the performance of the amplifier is also maximized at a lower frequency of operation. This design is left unmodified so that a comparison between the measured and the simulated performance in ADS is possible. The design also serves the purpose of allowing high-dynamic range testing at a different frequency range to study the effects of RF frequency on the pulse characteristics.

The JTB0008A design is tested in the same way as the other amplifier. The gain, output power, PAE, and input reflection coefficient are shown in Figures 5.11-5.14, respectively. The maximum output power and PAE is plotted in Figure 5.15. The output power and PAE is optimized at a carrier frequency of 2.6-2.7 GHz, similar to the original, unmodified JTB0007A design. The same characteristic in the return loss is visible in this design. The performance is limited when the return loss is high because the input drive to the amplifier is reduced. Therefore, the gain is reduced and the efficiency suffers. The swept power performance at a fixed frequency is shown in Figure 5.16. The performance is very similar to the other amplifier design. The harmonic power levels are low compared to the fundamental power due to the output matching network. The efficiency in this design is higher due the different harmonic matching network used.
Figure 5.11. JTB0008A CW class E mode gain.

Figure 5.12. JTB0008A CW class E mode output power.
Figure 5.13. JTB0008A CW class E mode PAE.

Figure 5.14. JTB0008A CW class E mode input reflection coefficient.
Figure 5.15. JTB0008A CW class E mode maximum output power and PAE versus frequency.

Figure 5.16. JTB0008A CW class E mode swept input power response at (a) $f_1 = 2.6$ GHz, (b) $f_1 = 2.7$ GHz, (c) $f_1 = 2.8$ GHz, and (d) $f_1 = 2.9$ GHz. The variables $f_2$ and $f_3$ denote the second and third harmonics.
5.1.3.1 Measured Versus Simulated Results

A test structure for the matching networks is created that allows measuring the S-parameters of the input and output matching networks. The networks are fabricated on a separate test board, and the Jmicro Technology Probe Point adapters are used to connect to the RF ports of the networks. The DC feed at the fundamental matching stub is connected to ground with a 0 Ω resistor to simulate the power supply connection. A photograph of the test board is shown in Figure 5.17.

![Figure 5.17. Matching network test structures (a) full test board view and (b) zoomed view of probe adapter board.](image)
The S-parameters of the test structures are measured using a vector network analyzer. A TRL calibration is performed to the end of the Jmicro Technology adapter boards using the supplied calibration structure and the Focus Microwaves TRL calibration software.

The results for the input matching network Rev. C design are shown in Figure 5.18. This design is used in the JTB0008A amplifier. The simulated and measured results for the fundamental frequency of 3 GHz and second and third harmonic are shown in Figure 5.18 on a Smith chart. The measured and simulated magnitude and phase response of the reflection coefficient presented to the DUT over the frequency range 1-12 GHz is also plotted in Figure 5.18. The network is optimized at the single frequency of 3 GHz. There is some phase error in the expected harmonic response and the magnitude response is slightly different, although the same general shape is present.

There are two main sources of errors in the matching networks. The first is the probe adapter test connection. The TRL calibration moves the reference plane of the measurement to the end of the adapter board. However, the wirebond is not attached to the exact end of the board, as seen in Figure 5.17. The simulated S-parameters use the reference plane at the end of the microstrip transmission lines. The wirebond is also not attached directly to the end of the transmission line. Therefore, this difference in line lengths causes a phase error in the measurement. It is expected that the phase error increases with frequency since the electrical length of the offset section becomes longer with increasing frequency. This effect is seen in the S-parameter comparison on the Smith chart in Figure 5.18(a). The phase error is increasingly worse for the second and third harmonic responses. The second source of error is the modeling of the discrete
passive elements used in the matching network. The input matching network includes a DC blocking capacitor and additional resistors in the stability network. The soldering process may add additional unaccounted parasitics that can affect the network response.

The results for the output matching network Rev. C design are shown in Figure 5.19. This design is used in the JTB0008A amplifier. The simulated and measured results for the fundamental frequency of 3 GHz and second and third harmonic are shown in Figure 5.19(a) on a Smith chart. The measured and simulated magnitude

![Smith chart diagram](image)

(a)

![Magnitude and Phase graphs](image)

(b) (c)

Figure 5.18. Input matching network Rev. C comparison to measured results (a) fundamental frequency \( f = 3 \text{ GHz} \), (b) magnitude, and (c) phase.
and phase response of the reflection coefficient presented to the DUT over the frequency range 1-12 GHz is also plotted in Figure 5.19. The network is optimized at the single frequency of 3 GHz. There is some phase error in the expected harmonic response and the magnitude response is slightly different, although the same general shape is present.

The input and output networks approximate the modeled response, but there are some magnitude and phase differences present. The measured S-parameters of the input and output networks are used in the harmonic balance simulation of the amplifier to

Figure 5.19. Output matching network Rev. C comparison to measured results (a) fundamental frequency $f = 3$ GHz, (b) magnitude, and (c) phase.
observe the effect of the shifted response. The maximum output power and PAE simulated response using the measured matching networks is shown in Figure 5.20.

The simulated results using the measured matching networks show that the output power drops off more rapidly with increasing frequency. The PAE is also slightly lower due to the matching network response. The updated simulation more closely matches the measured device performance.

A comparison of the measured and simulated swept input power response at a fixed frequency is shown in Figure 5.21. The nonlinear output power response is not accurately predicted in the simulated response. The gain of the real amplifier drops considerably at low drive levels, which is desired to achieve a high on/off isolation in a pulsed mode. However, the simulation shows that the output power follows a linear slope. The shape of the simulated PAE response compares well with the measured results. There is a difference in actual PAE values which appears considerable at first
Figure 5.21. JTB0008A class E mode measured and simulated results for swept input power at (a) $f_1 = 2.7$ GHz, (b) $f_1 = 2.8$ GHz, (c) $f_1 = 2.9$ GHz, (d) $f_1 = 2.95$ GHz. The variables $f_2$ and $f_3$ denote the second and third harmonics.

glance. However, the PAE is highly sensitive to the output power of the device. The PAE can be decreased by a factor of 10 points for a reduction in as little as 0.5 dB in output power. Therefore, the PAE difference is accounted for in the slightly lower simulated output power.

5.2 Pulsed RF Input Class E Amplifier Results

The proof-of-concept amplifiers are shown to be functional in the previous section. The CW performance is detailed, but it is the pulsed response that is of interest.
in this work. The Class E amplifiers are tested with a pulsed RF input using a test configuration similar to the CW test setup. In the pulsed test setup, a pulse modulator is added to the input RF signal as shown in Figure 5.22. The pulse modulator provides approximately 30 dB isolation over the measurement frequency range. It is placed after the input power amplifier so the noise is also pulse modulated.

The same directional coupler is used on the input to the DUT to measure the forward and reverse power. However, in this setup, the Agilent N1912A power meters are configured to a peak power mode. The output power meter is configured similarly. The spectrum analyzer is not able to measure pulsed signals; therefore, it is not possible to measure the harmonic power levels. The spectrum analyzer is used to view the output spectrum of the DUT to verify there are no spurious oscillations during testing.

The amplifiers do indeed generate a pulsed output, as theorized based on the sharp gain characteristic of the device versus input power, originally shown in Figure 4.12. However, the equipment used to validate the pulse behavior is limited in dynamic range and the high-dynamic range response can be hidden, as seen in the comparison of the MPI amplifier in Figure 3.31. The standard measurement results on the Class E amplifiers are taken. The measurements shown in this section are all based on the peak power level.

![Figure 5.22. Pulsed class E amplifier testing block diagram.](image-url)
results. The peak power, as measured by the N1912A power meters, is used for all power calculations. The DC supply current is reduced since the amplifier is off when there is no input drive. A peak value of the DC current is calculated by accounting for the duty factor of the input signal. This peak DC current is used in the PAE calculations.

The reduction of supply current is an important feature of the Class E amplifier operation in pulse mode. A similar Class A amplifier provides gain regardless of the input drive level. Therefore, the amplifier is dissipating power even during the dead time of the pulse. Conversely, the Class E amplifier only provides gain when the input pulse is present. Therefore, the amplifier dissipates minimal power during the dead time of the pulse. The Class A amplifier requires the addition of a suitable drain modulator to achieve this same effect. However, the drain modulator adds complexity to the amplifier and can dissipate a considerable amount of power itself.

5.2.1 JTB0007A Mod 11

The JTB007A Mod 11 design is tested in the pulsed test setup shown in Figure 5.22. The standard amplifier parameters of gain, output power, PAE, and input reflection coefficient are measured and the results are shown in Figures 5.23-5.26, respectively. The maximum output power and PAE versus frequency is plotted in Figure 5.27. The response of the amplifier in the pulsed mode follows the same trend as the CW performance. The output power and PAE is slightly better in the pulsed mode as compared to the CW input case. This result is not uncommon in power amplifiers, usually because of a reduced operating temperature due to the duty factor.
Figure 5.23. JTB0007A Mod 11 pulsed class E mode gain.

Figure 5.24. JTB0007A Mod 11 pulsed class E mode output power.
Figure 5.25. JTB0007A Mod 11 pulsed class E mode PAE.

Figure 5.26. JTB0007A Mod 11 pulsed class E mode input reflection coefficient.
5.2.2 JTB0008A

The JTB0008A design is tested similarly to the JTB0007A Mod 11 design. As expected, it follows a similar performance trend. The gain, output power, PAE, and input reflection coefficient results are shown in Figures 5.28-5.31, respectively. The maximum power and PAE versus frequency are plotted in Figure 5.32. The amplifier performance is also improved in the pulsed mode as compared to the CW mode. The output power is increased by nearly 1 dB at some frequencies with a corresponding increase in PAE of nearly 10 points.
Figure 5.28. JTB0008A pulsed class E mode gain.

Figure 5.29. JTB0008A pulsed class E mode output power.
Figure 5.30. JTB0008A pulsed class E mode PAE.

Figure 5.31. JTB0008A pulsed class E mode input reflection coefficient.
5.3 Pulsed RF Input Class E with Drain Modulator Amplifier Results

The Class E amplifier operates with a high on/off isolation in a pulse mode; however, the performance over a wide dynamic range cannot be verified using the standard measurement techniques. The amplifiers are tested using the HDRPPM technique and the results are presented later in this section.

The drain modulator is added to the Class E amplifier as another test configuration to provide assistance in generating a well-behaved pulse. The drain modulator is used to pulse the drain voltage from 0 to 15 V during the pulse time. The input RF signal is also pulsed. The block diagram of the test setup is shown in Figure 5.33. The drain modulator adds a considerable amount of low-frequency switching noise to the amplifier output. Therefore, a high pass filter is included in the output path to increase the accuracy of the output power measurements. The filter is

![Figure 5.32. JTB0008A pulsed class E mode maximum power and PAE versus frequency.](image-url)
reflective outside of the pass band. It is placed between attenuators to maintain a broadband 50 Ω impedance at the DUT reference plane.

The JTB0007A Mod 11 design is tested in a pulsed Class E mode with the addition of the drain modulator. The measurement results for gain, output power, and input reflection coefficient are shown in Figures 5.34-5.36. The maximum output power versus frequency is shown in Figure 5.37. The amplifier performance is quite similar to the standard pulsed Class E mode, as expected. The output power tracks well with the standard pulsed mode across frequency and input drive. A small difference of less than 0.5 dB is observed.

The device PAE is not easily measured due to the addition of the drain modulator. The drain modulator draws a considerable amount of current to generate the 15 V pulse and reduces the overall PAE of the amplifier/modulator combination. However, this test mode is primarily intended to examine alternative ways to increase the pulse profile performance and PAE is not a primary consideration.
Figure 5.34. JTB0007A Mod 11 pulsed class E mode with drain modulator gain.

Figure 5.35. JTB0007A Mod 11 pulsed class E mode with drain modulator output power.
Figure 5.36. JTB0007A Mod 11 pulsed class E mode with drain modulator input reflection coefficient.

Figure 5.37. JTB0007A Mod 11 pulsed class E mode with drain modulator maximum output power versus frequency.
5.4 Pulsed RF Input Class A Amplifier Results

It is instructive to have a comparison for the Class E amplifier results, in particular since the pulsed behavior of Class E amplifiers is previously unstudied. A linear Class A amplifier mode is typically well behaved in pulse behavior. The Class E amplifier design is biased at a linear operating point for comparison testing. The use of the same amplifier design with a different bias point helps to eliminate the effects of the matching network as a variable in the behavior of the pulse response. It also eliminates any possible device variability since the same device is used, just in a different operating mode. A separate optimized Class A amplifier design is not created so a direct comparison can be made. Better amplifier performance could be achieved if the matching networks are optimized, but the comparison is useful for the reasons stated.

The Nitronex HFET is biased using a static gate bias of $V_{gs} = -0.65$ V to achieve a linear operating mode. The drain modulator is used with the linear amplifier for pulsed testing. The drain is pulsed from 0 to 15 V to match the Class E drain bias. The Class A bias point causes a large drain current to be drawn continuously, which results in significant self heating for the amplifier. The amplifier bias is pulsed to reduce the self-heating effects and to protect the amplifier from thermal destruction. The test setup for the Class A amplifier is identical to the Class E amplifier testing with the drain modulator, shown in Figure 5.33.

The measurement results for gain, output power, and input reflection coefficient are shown in Figures 5.38-5.40. The maximum output power versus frequency is shown in Figure 5.41. The PAE is not measured for the same reasons given in the previous section.
The first noticeable difference is the gain performance shown in Figure 5.38. The gain remains flat versus input power until the amplifier compression point is reached. This behavior is expected for a linear amplifier. The input match is also consistent versus input power, as shown in Figure 5.40. The match is quite good even though the matching network is optimized for a different mode of operation. The maximum output power is achieved at a frequency of ~2.7 GHz, which is different from the Class E amplifier optimum performance point. The output power is higher in the Class A mode, as expected. The output power is over 1 dB higher when comparing the maximum values of each amplifier mode.

Figure 5.38. JTB0007A Mod 11 pulsed class A mode gain.
Figure 5.39. JTB0007A Mod 11 pulsed class A mode output power.

Figure 5.40. JTB0007A Mod 11 pulsed class A mode input reflection coefficient.
5.5 Pulsed RF Input Class E Amplifier HDRPPM Results

The amplifier measurements given in the previous sections provide a baseline performance evaluation metric for evaluating the high-dynamic range pulse profile behavior of the amplifiers. The standard amplifier power measurement techniques provide a course look at the power profile, but not over the dynamic range required for highly sensitive systems. The standard Class E amplifier mode with a pulsed RF input is evaluated for the two amplifier designs.

The JTB0007A Mod 11 amplifier is tested at 2.9 and 3.0 GHz using the HDRPPM system. The HDRPPM results are plotted against the standard peak power measurement using an Agilent N1912A power meter. The results at $f = 2.9$ GHz are shown in Figure 5.42 and the results at $f = 3.0$ GHz are shown in Figure 5.43.

The results for the Class E amplifier are significantly different from the initial results for the Microwave Power amplifier presented in Section 3.13. The JTB0007A Mod 11 Class E amplifier shows a very slow turn-off characteristic for both test frequencies. In both cases, the power of the pulse does not reach the noise floor of
Figure 5.42. JTB0007A Mod 11 class E HDRPPM results at $f = 2.90 \text{ GHz}$. 

Figure 5.43. JTB0007A Mod 11 class E HDRPPM results at $f = 3.00 \text{ GHz}$. 

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the measurement before the next pulse occurs. The power meter results do not reveal this behavior.

The JTB0008A amplifier is also tested to investigate the effect of an alternate matching network and lower measurement frequency. The JTB0008A amplifier is optimally tuned near 2.6 GHz. The amplifier is tested using the HDRPPM system at 2.6 GHz, 2.65 GHz, and 2.7 GHz with the results shown in Figures 5.44-5.46, respectively. A similar slow time-constant characteristic is seen in the pulse profile of the JTB0008A amplifier.

Figure 5.44. JTB0008A class E HDRPPM results at $f = 2.60$ GHz.
Figure 5.45. JTB0008A class E HDRPPM results at $f = 2.65$ GHz.

Figure 5.46. JTB0008A class E HDRPPM results at $f = 2.70$ GHz.
In both amplifiers, the pulse initially turns off with a fast decay rate. Then the pulse decay rate changes at approximately 100 ns after the half-power point on the falling edge of the pulse. This poor turn-off characteristic is problematic for high-dynamic range systems because the correlated energy level at the amplifier output remains detectable during a potential receive gate time.

5.6 Pulsed RF Input Class E Amplifier with Drain Modulator HDRPPM Results

The base Class E amplifier pulse profile results show a very slow turn-off characteristic. This result is not altogether unexpected, however, since there is no help from a pulse modulator to turn the device off. In a Class A amplifier with a drain modulator, the modulator serves two purposes. The modulator supplies current when the amplifier is initially turning on and also during the pulse time. The modulator then sinks current when the amplifier is shutting off. For example, when a totem-pole modulator is used, the bottom device helps to pull charge out of the active device, improving the fall time of the amplifier pulse. There is no mechanism in the Class E amplifier to actively pull charge out of the amplifier.

The drain modulator described in Section 4.13 is used to supply a drain pulse as used during the standard amplifier testing. The JTB0007A Mod 11 Class E amplifier with drain modulator is tested using the HDRPPM system to examine the impact the drain modulator has on the pulse profile. The amplifier results at 2.90 GHz and 3.00 GHz are shown in Figures 5.47 and 5.48, respectively. The measurement results are quite surprising.
The addition of the drain modulator does not improve the pulse profile characteristics of the Class E amplifier. There is little to no impact on the actual power measured in the pulse profile. The voltage applied to the drain of the amplifier is effectively 0 V, as seen in the drain modulator pulse in Figure 4.51. However, the HDRPPM results show that the dissipation rate at the output of the amplifier is unaffected by the drain bias. This result seems to indicate that the pulse behavior is affected only by the static gate DC bias on the amplifier during the pulse time. This result correlates with the effect that the charge trapping behavior in a FET device varies depending on the static bias [74]. The behavior of the Class E amplifier reflects a deep level trapping behavior that has a long time constant.

Figure 5.47. JTB0007A Mod 11 class E with drain modulator HDRPPM results at \( f = 2.90 \) GHz.
The initial MPI amplifier results showed that the linear amplifier pulse profile is well behaved during the falling edge of the pulse. The power on the falling edge of the pulse decreased below the detectable power level of the HDRPPM system approximately 700 ns after the half-power point on the falling edge. However, the Class E amplifier results have shown that energy still exists even as the next pulse is generated.

The bias on the JTB0007A amplifier is changed to operate the amplifier in a linear Class A mode to examine the effect on the pulse profile. The gate bias on the amplifier is set at -0.65 V and the drain voltage is pulsed using the drain modulator. The HDRPPM results for the JTB0007A Mod 11 amplifier at 2.9 GHz and 3.0 GHz are shown in Figures 5.49 and 5.50, respectively.
Figure 5.49. JTB0007A Mod 11 class A HDRPPM results at $f = 2.90$ GHz.

Figure 5.50. JTB0007A Mod 11 class A HDRPPM results at $f = 3.00$ GHz.
The pulse profile of the JTB0007A Mod 11 amplifier operating in a Class A mode is markedly different. In this case, the amplifier turn-off characteristics more closely resemble the MPI amplifier results. The power at the amplifier output goes below the minimum measurement sensitivity at approximately 700 ns after the half-power point on the falling edge of the pulse.

5.8 Amplifier Mode Comparison

The amplifier pulse profile behavior is different when operating in either a Class E or Class A mode. A summary of the pulse profile results for each of the amplifier modes is plotted in Figures 5.51 and 5.52 for the measurement frequencies of 2.9 GHz and 3.0 GHz, respectively. The pulse profile of the MPI L0203-41 driver amplifier is also included as a reference for the pulse behavior. The results are normalized to allow a direct comparison of the decay rates for the different amplifier modes.

The two cases for the Class E amplifier are nearly identical. The addition of the drain modulator does not affect the pulse profile of the amplifier. It appears that there are multiple rates of decay in the amplifier response for this operating mode. A linear least-squares curve fit is applied over three regions. Region 1 is defined as the time range from 215-280 ns, Region 2 is defined from 280-530 ns, and Region 3 is defined from 685-1500 ns. The Class E amplifier curve fits for 2.9 GHz and 3.0 GHz are plotted in Figure 5.53.

Region 1 has a fast time constant and decays at a rate of 0.89 dB/ns. A longer time constant effect takes over in Region 2 and shows a decay rate of only 0.07 dB/ns.
Figure 5.51. JTB0007A Mod 11 amplifier normalized pulse profile results for different operating modes in comparison to MPI amplifier driver at $f = 2.90$ GHz.

Figure 5.52. JTB0007A Mod 11 amplifier normalized pulse profile results for different operating modes in comparison to MPI amplifier driver at $f = 3.00$ GHz.
Finally, a very long time constant behavior is observed in Region 3 that has a decay rate of only 0.02 dB/ns. A similar curve fit is applied to the pulse profile at 3.0 GHz. A fast decay rate of 0.9 dB/ns is observed in Region 1. The power in Region 2 is nearly flat and only decays at a rate of 0.01 dB/ns. Then, in Region 3, the slow time constant effect takes over with a decay rate of 0.03 dB/ns.

The pulse profile of the Class A amplifier has a much faster decay characteristic as compared to the Class E amplifier. A linear least-squares curve fit is performed for two different regions. Region 1 is defined as the time range from 215-260 ns and Region 2 is defined from 345-800 ns. The frequencies of 2.9 GHz and 3.0 GHz are analyzed in Figure 5.54. The decay rate in Region 1 is fast at both frequencies. The decay rate at 3.0 GHz is 2.54 dB/ns compared to 2.35 dB/ns at 2.9 GHz. The response in Region 2 exhibits a much slower decay rate, similar to the decay rate of the Class E amplifier for the same time range.
It is shown that the different sources of traps in a FET have different associated time constants. It is demonstrated that slow traps are associated with the channel, intermediate time constant traps are related to the deep levels in the buffer layer, and fast traps are attributed to the surface states [104]. The channel is modified by the change in bias on the amplifier and can account for the drastic difference in decay rate in the initial turn-off region. Electrons can be trapped in the vicinity of the channel for large negative gate bias voltages [104]. This condition corresponds to the Class E amplifier bias and the behavior that is observed. The intermediate time constant effects could account for the similar decay rate in the final region of the pulse profiles for the various amplifier modes since the state of the buffer layer remains relatively unchanged for changes in gate bias. It is shown that the traps in the buffer layer vary little with changes in drain bias [104]. Further work is required to validate the exact nature of the trapping behavior in the device.
5.9 Summary

The detailed measurement results on the proof-of-concept Class E amplifiers are presented. The amplifiers are first tested in a CW Class E mode to validate that the test boards are functional. The realized performance of the amplifiers is offset in frequency due to an issue in the Microwave Office implementation of the Angelov2 model. The JTB0007A amplifier design is modified by trimming the microstrip stubs to tune the response higher in frequency.

The Class E amplifiers are tested with a pulsed RF input to validate that the devices operate with a high on/off isolation that follows the input pulse. The Class E amplifiers do indeed generate a clean pulse as measured by a peak power meter. The amplifiers are characterized in the pulsed mode to ensure there are no issues. The full suite of measurement results are given for the two amplifier designs created in this work.

The standard peak power meter is limited in dynamic range and does not reveal the characteristics of the pulse profile of the Class E amplifier. The two amplifier designs are tested in a pulsed Class E mode using the HDRPPM system. The measurement results reveal a very long time constant behavior in the turn-off characteristics of the amplifier. The decay rate is so slow that energy is still detectable by the time the next pulse is generated. This behavior is not observable using the standard power meter measurement technique. The slow decay rate is observed for the two Class E amplifier designs at all of the measurement frequencies. Therefore, the effect is not fundamentally frequency dependent, although the power does vary somewhat with frequency.

A drain modulator is added to the Class E amplifier design to aid in removing charge from the drain as the amplifier is pulsing. The drain modulator uses a totem-pole
driver output that allows current sourcing and sinking capabilities. However, the addition of the drain modulator has no impact on the measured pulse profile. This effect is interesting and leads to the belief that deep charge traps within the device are responsible for the slow energy decay rate. The trapping in an active device is dependent on the DC bias applied.

The JTB0007A Mod 11 amplifier is tested in a Class A mode to provide a direct comparison for the impact of bias on the amplifier turn-off characteristics. The gate is biased at a higher voltage to change the operating mode of the amplifier. The same drain modulator is used to provide the pulse modulation of the amplifier. The pulse profile for the linear operating mode is much better behaved than the Class E mode. The initial decay rate of the amplifier pulse is nearly two and a half times faster, resulting in a much lower final power level. The energy decays below the measurement threshold by approximately 700 ns after the falling edge of the pulse.

The baseline Class E design does provide an attractive amplifier for standard pulse-mode applications. The amplifier is effectively off when an input signal is not present. Therefore, the amplifier is not drawing supply current and it is not dissipating any power. This fact is important in comparison to the Class A amplifier that burns power even when an input signal is not present. However, the Class E amplifiers tested in this work have a very slow turn-off characteristic. The situation is not improved with the addition of a drain modulator. It is likely that the only solution for improving the turn-off rate is to eliminate the sources of trapping in the GaN HFET device.

GaN is a relatively immature technology compared to GaAs or other semiconductors, and it is going through the same growing pains. The trapping behavior
of GaN is widely studied, although there is not a consensus on what are the direct causes of the trapping behavior [74], [105]. The pulse performance might be improved if the impurities in the GaN buffer layer could be reduced. The surface states are also shown to have an effect on drain lag, even though it is commonly associated with substrate traps [74]. The surface state charge trapping effects have been reduced in GaAs devices through improved silicon nitride passivation processes. The Nitronex devices do have a passivation layer, but impurities in the layer can lead to charge trapping. The pulsed Class E amplifiers examined in this work may not provide suitable performance for use in a fast pulsed, high-dynamic range application due to the slow time constant behavior observed in the turn-off characteristics of the pulse.
6. GENERAL CONCLUSIONS

A high-dynamic range pulse profile measurement system is developed for fast, pulse-mode applications, advancing the state of the art in pulse profile measurement techniques. The current techniques available in the marketplace today do not support measuring the characteristics of a device over the full dynamic range required with a suitable time resolution in fast pulsing configurations.

A technique of tagging pulses along with a correlation technique using multiple pulses is presented to increase the measurement SNR, allowing for detecting very low signal levels. A full system is developed that includes a transmitter for stimulating a DUT, a pulsed measurement receiver, and the associated signal processing algorithms for measuring power accurately in the presence of noise. The system achieves a full measurement range of over 160 dB for measuring devices in the S-band with a pulse width of 250 ns. The technique developed is applicable to multiple domains, including long-range communication and radar systems.

The introduction of wide bandgap semiconductors stands to revolutionize the wireless industry. Semiconductor technologies such as GaN and SiC offer the promise of higher power densities and higher frequencies of operation. Gallium nitride is attractive due to its higher transition frequency and high breakdown voltages. These characteristics make GaN an excellent choice for high-efficiency amplifier design.

It is theorized that the Class E amplifier mode allows the generation of a high-isolation pulsed output signal simply by pulsing the input RF signal. This particular mode of operation has not been studied in the literature. A set of proof-of-concept
Class E amplifiers targeted for fast, pulse-mode applications are designed to operate within the S-band. The full design procedure is outlined. Measurement results are compared to the simulated results for the standard, CW operating mode.

The amplifiers are then characterized in a pulsed mode. The amplifiers perform reasonably well using standard characterization techniques. The Class E amplifier does work as expected, generating a clean output pulse that follows the input pulse. This design is attractive because there is no gain during the dead time of the input pulse; therefore, there is no power dissipation during this time. The supply current is reduced by the duty factor of the device, which reduces the average operating temperature. An external pulse modulator is not required as in linear amplifier designs, reducing the overall system complexity. This capability is useful for miniaturizing low-power systems that can operate with a constant envelope modulation scheme.

The output pulse of the Class E amplifier appears well-behaved using standard measurement techniques, such as a peak power meter. However, the amplifier’s pulse profile is significantly degraded when measured with the HDRPPM technique. The Class E amplifiers developed in this work demonstrate a very long time constant behavior during the falling edge of the output pulse. This energy is still detectable even when the next pulse in the system is generated. Clearly, energy would be present at the receive time if this amplifier were used in a real system. This behavior cannot be detected using the standard measurement techniques and could potentially cause undesired results, or even failure, of the final system.

A drain modulator is added to the Class E design to improve the capability of the amplifier to generate a pulsed signal. However, it is discovered that the addition of the
drain modulator does little to improve the long time constant effect of the amplifier. This behavior seems to originate as deep level traps within the device and is not affected by changes at the output.

The trapping behavior of a device is typically dependent on the static bias voltages applied. The same amplifiers are measured in a Class A operating mode by raising the gate voltage appropriately. The drain modulator is required for this bias condition because the amplifier provides gain even when no input signal is present. The amplifiers are characterized using the standard techniques to ensure that a suitable pulse is generated. Next, the amplifiers are characterized using the HDRPPM technique. An interesting result is obtained.

The amplifier turn-off characteristics are significantly improved in the Class A operating mode. This result seems to suggest that the behavior is not driven by the matching networks, since it is the same amplifier that is measured, only with a different gate bias. The second rate of decay of the energy is consistent for both bias points used. However, the Class A amplifiers show a much steeper initial rate of decay. Therefore, the total power measured on the falling edge of the pulse is much less in this situation.

It is clear that the Class E amplifier mode does indeed generate a high-isolation output pulse by pulse modulating the RF input signal. This mode is useful for simplifying the system design since a pulse modulator is not required. However, the turn-off characteristics of the pulse in this mode for the GaN device used are significantly degraded. These results could preclude the use of this amplifier in a high-dynamic range application that uses fast pulsing.
The results are particularly interesting in that the addition of a drain modulator
does not improve the Class E pulse characteristics. There is room for additional work in
this area. The gate bias could be varied over a wider range to observe the effect of
trapping on the resultant pulse characteristics. New amplifier designs could be fabricated
using alternative GaN or GaAs devices to determine if the effect is inherent in GaN or
only a result of the traps found in the device used in this work.
REFERENCES


