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Contributions towards a coherent chaotic oscillator at 100MHz and 70 GHz antennas for automotive radar applications.

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CONTRIBUTIONS TOWARDS A COHERENT CHAOTIC OSCILLATOR AT 100MHZ AND 70GHZ ANTENNAS FOR AUTOMOTIVE RADAR SYSTEMS.

by

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THESIS

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DEDICATION

To my father Nazem who influenced my career path.
May he live a long healthy life.

To my mother Safiya who sacrificed a lot to raise us up.

To my sister and best friend Amal.

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Contributions towards a Coherent Chaotic Oscillator at 100MHz and 70GHz Antennas for Automotive Radar Systems.

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Firas Ayoub

BE Electrical & Computer Engineering, American University of Beirut, June 2011

Master of Science in Electrical Engineering, July 2013

ABSTRACT

This Master's thesis focuses on the design of a coherent chaotic oscillator working at a base frequency of 100MHz, and the design of an array of patches operating in the frequency range of 71-76 GHz. The array will be used to transmit the chaotic signal after it is up-converted. The requirements of the coherent chaotic oscillator in terms of delays and linearity are investigated using two simulation software: MATLAB and Advanced Design System (ADS). A general relation between the allowed propagation delay and frequency is devised and the problems in the design and implementation of such an oscillator are discussed. Regarding the antenna, an array of patches is designed to operate at a frequency of 73GHz using both Computer Simulation Technology (CST-MWS) and High Frequency Structure Simulator (HFSS), in addition, two feeding techniques are realized. The first one uses a grounded CPW line, which allows the antenna to be tested using infinity probes and the second one uses a WR-12 rectangular waveguide to feed and test the operability of the antennas. The array is fabricated and tested in the lab to verify the simulated results.

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Chapter 1. Introduction

This thesis presents the work done on the design of a coherent chaotic transmitter used for radar applications. The transmitter up-converts a coherent chaotic signal with a base frequency of 100MHz and transmits at the frequency band 71-76GHz.

1.1 Chaos and Its Characteristics

According to Nagashima *et al.* in their book, Introduction to Chaos [1], chaos is defined as a totally disorganized state. In electrical engineering, chaos refers to a phenomenon that is moderately disordered and shows a temporarily irregular behavior: "an irregular oscillation governed by a relatively simple rule".

Chaotic signals are non-periodic, noise-like, broadband and extremely sensitive to the initial conditions of the system that generates them. As a consequence of being extremely sensitive to the initial conditions, the signal is unique and hence very hard to reproduce. In addition, the broadband characteristic of the signal gives it good interference avoidance properties. All of the properties mentioned, make the chaotic signal very hard to intercept.

For the system being designed, the idea is to design a coherent chaotic signal at a base frequency of 100 MHz. The design is based on the chaotic signal discovered by Corron *et al.* [2] that was proved to be achievable at low frequencies.

The main application of the chaotic signal is in an automotive radar system where it is going to be up-converted to the E-band (71-76GHz) since it is an unassigned band. Moreover, the E-band achieves high resolution for a radar system.

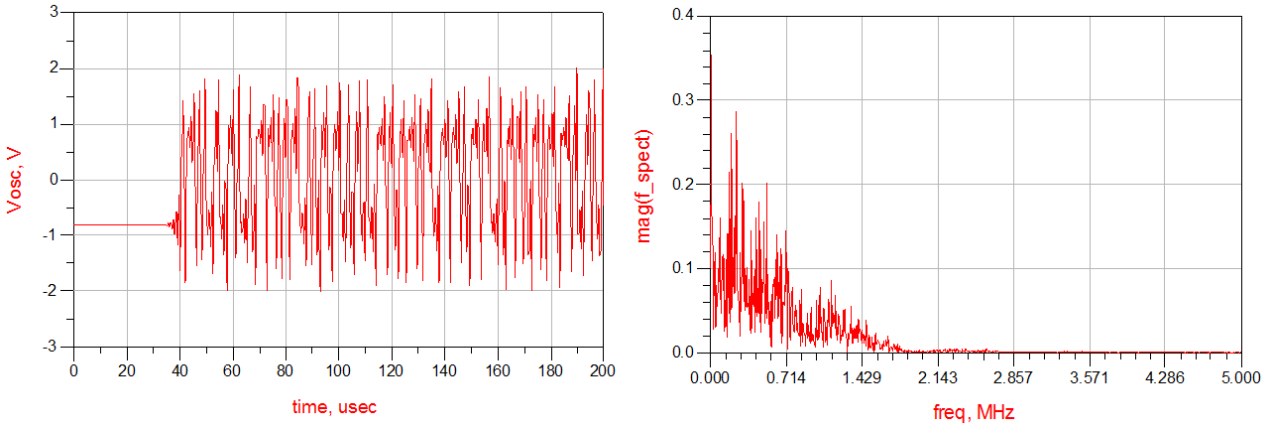

Figure 1: Chaotic signal with its frequency spectrum.

1.2 System Under Design

The proposed system is a coherent chaotic transmitter. The coherent chaotic signal is generated at a base frequency of 100MHz, in order to achieve a high data transmission rate. The chaotic signal is up-converted following these steps:

- Step 1: to 3 GHz.
- Step 2: to 18 GHz.
- Step 3: to 71-76 GHz.

The final up-converted signal is then amplified in order to be transmitted through the antenna. The proposed antenna design is an 8x8 printed array. The overall layout of the proposed system is detailed in Figure 2.

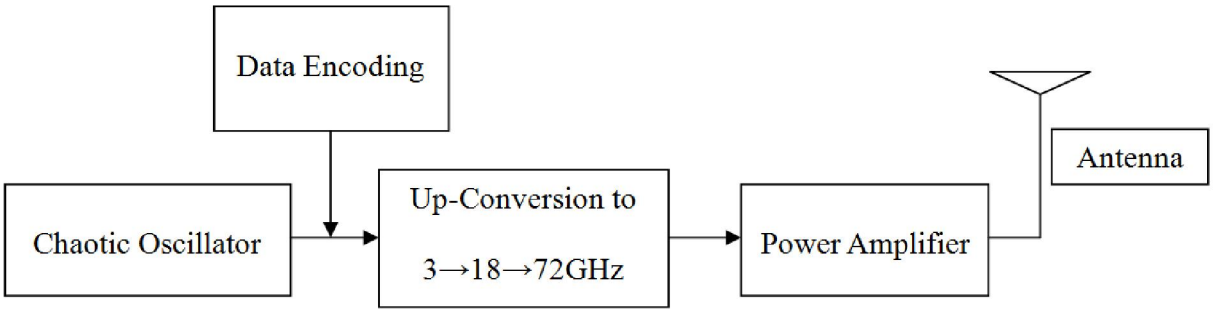

Figure 2: Block diagram for the proposed system.

This transmitter can be used in a collision avoidance system that employs automotive radar. The system is designed for the purpose of detecting surrounding cars and identifying the possibility of collision with these cars. In Figure 3, the scenario where nearby cars are detected by the radar is shown in green and the scenario where two interfering signals from two different cars is shown in yellow.. The up-conversion of the chaotic signal to E-band insures a better resolution for the radar and the chaotic signal insures no interference with other chaotic signals used by other systems deployed in other cars.

The proposed transmitter can also be used in military applications such as surveillance systems, altimetry and ground penetrating profiling.

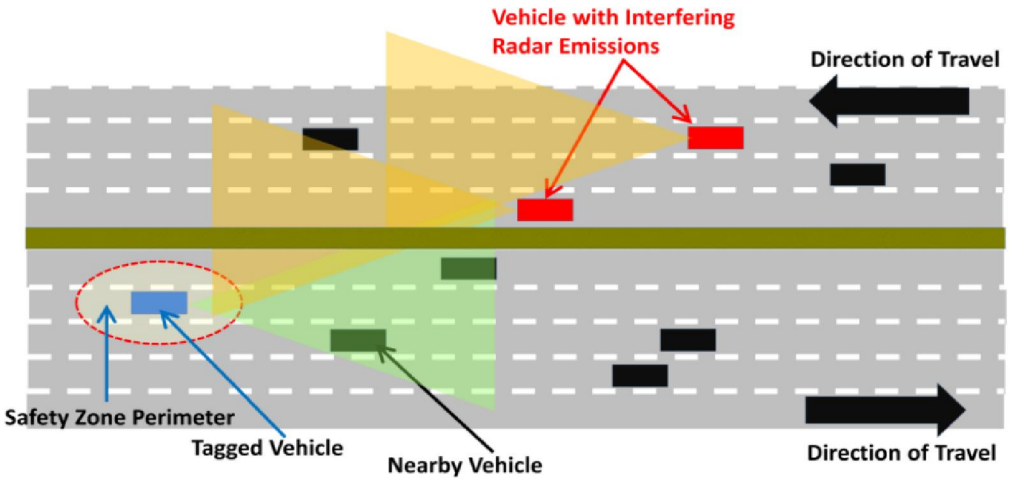

Figure 3: Illustration of the environment in which the chaotic transmitter could be put into use.

1.3 Thesis Organization

This thesis is divided into the following chapters. In chapter 2, a literature review of the work done on chaotic oscillators used in radar applications is presented. An overview of the different types of antennas designed to operate at 77GHz is also presented.

The study of the requirements of the coherent chaotic signal at high frequencies is described in Chapter 3. The design of the coherent chaotic oscillator at 100MHz is discussed in Chapter 4.

Moreover, in Chapter 5 the design of the antenna array operating at 73GHz is shown. Two different feeding techniques are also investigated. The fabrication and the measurement results of the antenna are presented in Chapter 6. The comparison between simulated and measured data is also provided. The thesis ends with a conclusion and the future work.

Chapter 2. Literature Review

In this chapter, a literature review on the different types of chaotic oscillators is presented. The different types of antennas, available in the literature, operating at frequencies as high as 77 GHz are also presented. The feeding techniques used to feed the antenna patches at E-band is discussed as well.

2.1 Chaotic Oscillator:

In 1993, it has been shown theoretically by Hayes *et al.* [3] that it is possible to communicate with chaotic signals by controlling them with small perturbations. Any symbol can be encoded within the dynamics of the chaotic signal by assigning 0 or 1 to the positive peaks and the negative peaks of the chaotic signal. By the use of small perturbations, the oscillations will follow the binary sequence to be encoded. Several methods were formulated to encode data in chaotic signals. The one proposed by Hayes et al. [4] uses a computer assisted algorithm (a controller) to determine the signal dynamics by taking samples rapidly and determining the time instances a current pulse should be given to the oscillator in order to control its oscillations.

This discovery concerning the encoding of data in the dynamics of chaotic signals had the potential to change the chaos radar systems and the high bandwidth data communication systems. However, the lack of a coherent receiver that can receive the controlled chaotic signal, created a problem in using the chaotic signal to encode data and transmit it.

Several research groups were working on techniques to be implemented in receivers to enable receiving chaotic signals. These research groups used either noise reduction techniques which were computationally intensive or synchronization techniques that necessitated low noise channels which is impossible in radar systems [5,6,7].

Coherent reception of a chaotic signal was proven difficult because of the lack of a fixed chaotic basis function and the irregular timing characteristics of the signal [8].

In 2010, Corron *et al.* discovered a new class of chaotic oscillators described by a hybrid dynamical system comprising both a continuous-time differential equation and a discrete switching condition, for which an analytical solution can be written as a linear convolution of a fixed basis function and discrete symbols. This signal was proven chaotic by the folding action in the state space representation that was due to switching events. The authors were able to generate this chaotic signal at a frequency of 84Hz along with its matched filter [2]. In this research, this class of oscillators is studied at RF frequencies, the implementation difficulties and the problems faced in the design of such chaotic oscillator at 100 MHz are determined.

2.2 77 GHz Antennas

With the rise of automotive radar, Intelligent Cruise Control systems (ICC) and collision avoidance systems, antennas operating at frequencies close to 77GHz gained more research interest, especially that, the frequency band 76-78GHz was allocated to

such applications [9,10,11]. However, the frequency band 71-76GHz is still not allocated and is open to collision avoidance research application. Depending on the application, these antennas must have certain characteristics. For instance, in the previously stated applications, these antennas should have high directivity and low side-lobe levels, plus, they can allow more than one main lobe [2]. The antennas used in these types of applications should have a small size to facilitate their integration in vehicles.

Several types of antennas were studied at these frequencies. The Laminated Resonator antenna [12], for example, showed a large bandwidth that can be controlled by varying the height and the length of each element. The folded optical lens antenna had an advantage in the feeding system with low losses [9]. Its disadvantage is the high level of side-lobes caused by the feeding technique. The Vivaldi antenna, in [13], produced a broadband beam and a narrow bandwidth but it experienced huge radiation losses because of the feeding system. The quasi Yagi-Uda antenna produced a directive high gain signal when the number of its elements was greater than three [10]. The dual bow-tie antenna, in [14], showed high total efficiency and a wide bandwidth. The ground plane influenced the impedance and the bandwidth of the antenna. The Micromachining technology (MEM) is used for integrated antennas because it offers efficient packaging, high radiation efficiency wide impedance bandwidth and less mutual coupling between antenna elements [15].

One last type of antenna which was studied previously in the E-band is the microstrip patch antenna. According to the authors in [9], this type of antennas experiences problems in the feeding network since the latter plays a role in its total

efficiency. They suggest the use of a slotted waveguide which reduces the radiation losses of the array when coupled to the microstrip feeding lines of each patch in an array.

In [6,10], the bandwidth of the patch was studied by considering different patch configurations. The authors in [16] compared the differences between several configurations of the patch antenna: suspended, partially-suspended and conventional patch antennas. In this paper, the antennas were fed using an RF probe. The partially-suspended antenna showed the highest radiation bandwidth, followed by the suspended and finally the conventional patch antenna.

In [17], the authors compared two different rectangular patch feeding line as shown in Figure 4. The conventional microstrip line which is connected to the width (W) of a patch and the differential microstrip line which is connected to the length (L) of the patch. The differential feeding technique proved to have a wider bandwidth than the microstrip line method.

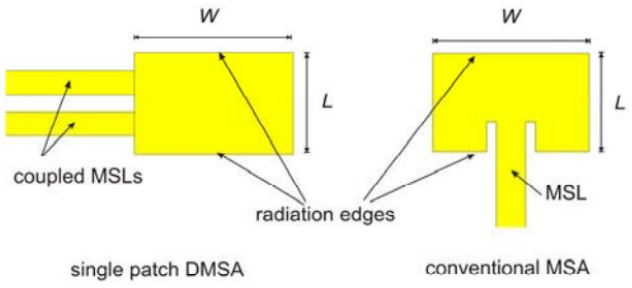

Figure 4: Differential Microstrip Antenna (on the left) and Conventional Microstrip Antenna (on the right) [10]

Furthermore, the authors in [11] suggest a beam steering technique based on a movable dielectric slab under the feeding lines of the patch antennas. The movement of the dielectric slab changes the permittivity of the dielectric material and causes the patch beam to change its angular position, as shown in Figure 5.

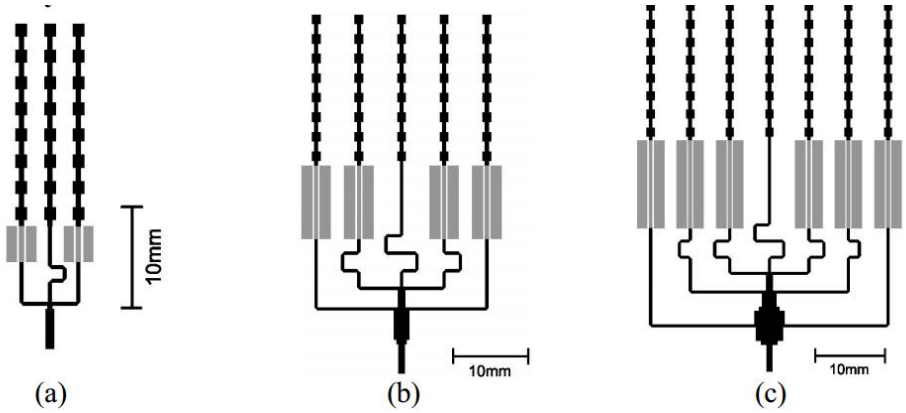

Figure 5: Layout of the antenna array with the dielectric slabs [5]

In all of the designs of the patch antennas, the patches were fed via either an RF probe mounted on a GCPW or a slotted WR10. Most of the designed patches were not tested. The implementation of an array of patches where all the elements are fed in phase was not done and the comparison between the effect of different feeding techniques on the array was not carried so far. These two issues are discussed in this thesis and detailed in Chapter 5.

Chapter 3. Chaotic Oscillator Requirements

3.1 Chaotic Oscillator Architecture

The chaotic signal generated is described by the following differential equation:

$$\frac{d^2u}{dt^2} = 2 \times \beta \times \frac{du}{dt} + (\omega^2 + \beta^2) \times (s - u) \ldots\ldots\ldots\ldots\ldots\ldots (3.1)$$

where 'u' is the chaotic oscillator output (continuous signal) and 's' is the switching condition [2].

The behavior of the signal can be described as follows:

The signal starts from a negative voltage level (-V). It starts oscillating with an increasing magnitude. The derivative of the signal is always monitored because it governs switching between the +V and –V DC offsets. The moment the signal reaches a positive value, with its derivative equals to zero (red dot indicator), the signal continues oscillating around +V. On the other hand, the DC offset level of the oscillating signal has to be switched to –V whenever the amplitude of the signal, with its derivative equals to zero, reaches a negative value. Figure 6 below illustrates the signal being generated.

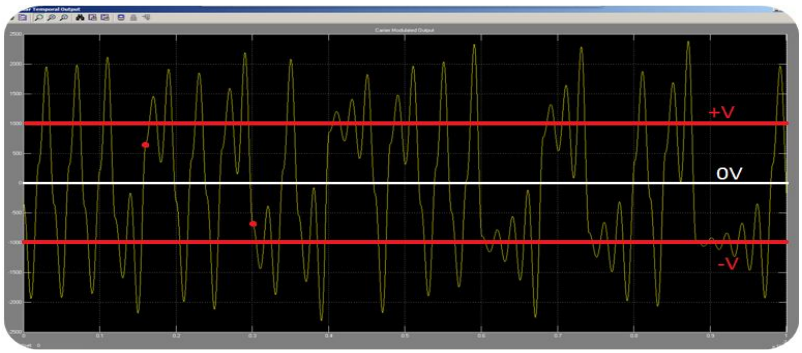

Figure 6: Coherent Chaotic Signal. (The red dots mark the time when the DC level is changed)

When sampling the chaotic signal at a certain time interval "T", which represents the times where the signal has a derivative equal to zero and an amplitude less than $|V|_s$ gives a series of points V_n that has the following return map shown in Figure 7. This return map is obtained because the relation among the elements of the series is described in equation 3.2 [2]:

$$u_{n+1} = e^{\beta}u_n - (e^{\beta} - 1)\mathrm{sgn}(u_n) \ldots\ldots\ldots\ldots\ldots\ldots (3.2)$$

This equation when plotted, gives the same plot as in Figure 7. Another explanation for the return map is the fact that the signal is deterministic. This means that the sampled points will be following a certain trajectory when the switching event occurs.

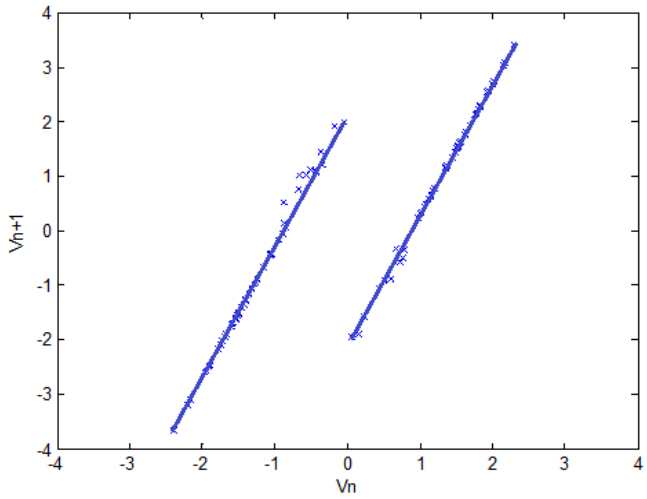

Figure 7: Return map of the chaotic signal being generated

In order to generate this chaotic signal, the circuit architecture, which was proposed by Corron et al. [2], should be used:

First a -RLC oscillator is used, its signal output is fed to the chaos control unit. The chaos control unit is divided into two paths, the first path consists of a differentiator followed by a comparator (cp1). The second path consists of another comparator (cp2). The comparator "cp1" checks whether the derivative of the oscillator signal is less than zero and the comparator "cp2" checks whether the oscillator signal is greater than zero. The outputs of the two comparators are fed to a logic control unit, which is the unit that controls the DC level of the chaotic signal being generated. The output of the logic control unit controls a switch which has its output fed to the inductor of the oscillator. Figure 8 below shows the different parts of the chaotic oscillator.

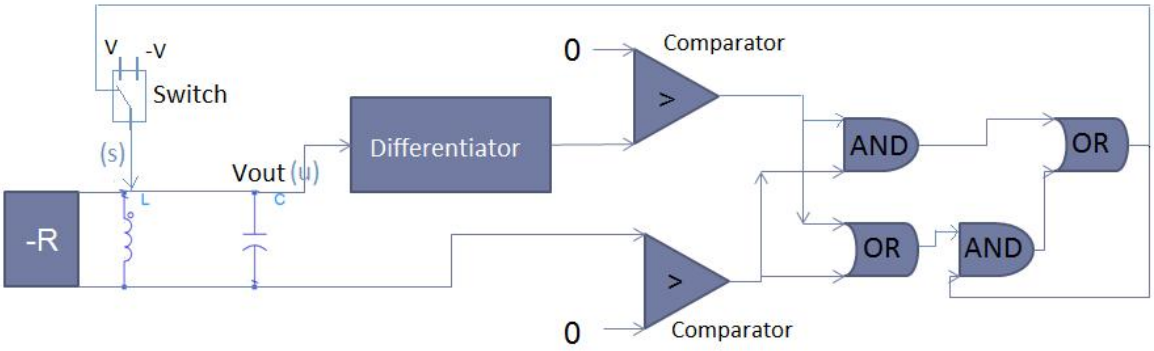

Figure 8: Chaotic oscillator blocks

3.2 Chaotic Oscillator Testing

The operation of the circuit shown in Figure 8 is tested at low frequencies. A propagation delay is then added in order to check the operation of the circuit at high frequencies. This is important because at high frequencies the propagation delay plays a

significant role in the generation of the signal. Equation 3.3 shows the role played by the propagation delay when its value is increased.

$$\frac{d^2u(t+T_1)}{dt^2} = 2 \times \beta \times \frac{du(t+T_1)}{dt} + (\omega^2 + \beta^2) \times (s - u(t+T_1)) \ldots\ldots\ldots\ldots (3.3)$$

Where T_1 represents the propagation delay.

The chaotic oscillator is simulated and tested using ADS as shown in Figure 9. The operation of the circuit is first studied at low frequencies (10Hz and 1KHz). Then, the effect of delays is investigated at higher frequencies (1MHz and 100MHz).

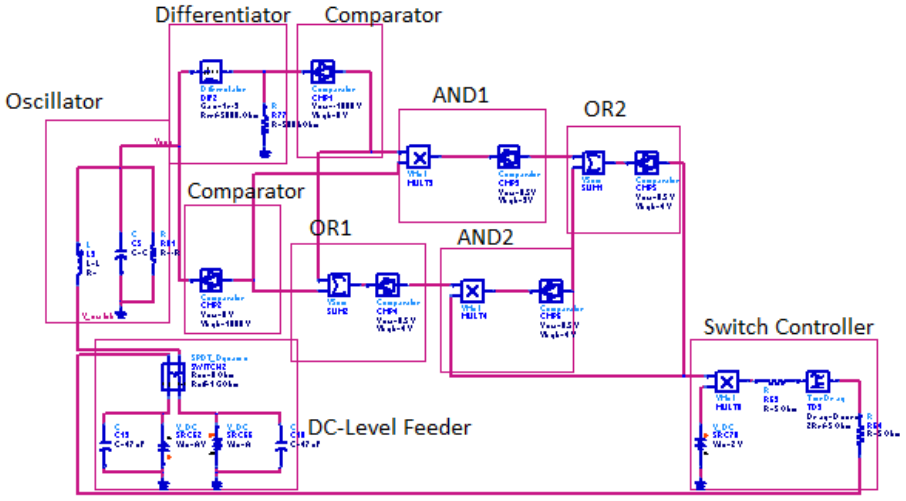

Figure 9: Ideal circuit used to study the chaotic signals at different frequencies

3.2.1 Study at Low Frequencies

I. For a base frequency of 10 Hz, the results are summarized in Figure 10:

The chaotic signal generated at 10Hz is shown in Figure 10 (a). The phase space representation which is shown in Figure 10 (b), represents the test for chaotic behavior. In this case, the shape of the phase space representation proves that the signal is chaotic. Figure 10 (c) shows the frequency spectrum analysis of the generated signal. The frequency spectrum shows a broadband signal which is one of the characteristics of the chaotic signal. The return map of the generated signal in Figure 10 (d), which is obtained from plotting V_n vs V_{n+1}, shows two parallel lines, as expected, with scattered points due to sampling errors.

The following values were used: -R = -5 Ω, L = 22mH and C = 11.5mF.

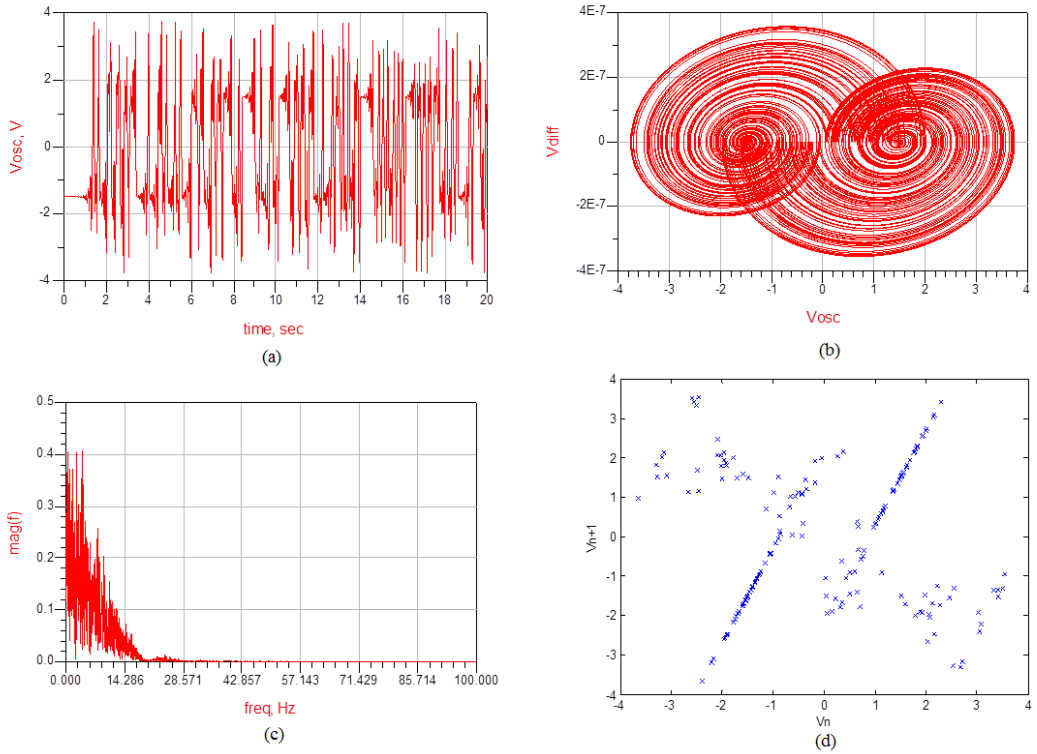

Figure 10: Chaotic output at 10 Hz where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

II. For a base frequency of 1 kHz, the following results were obtained:

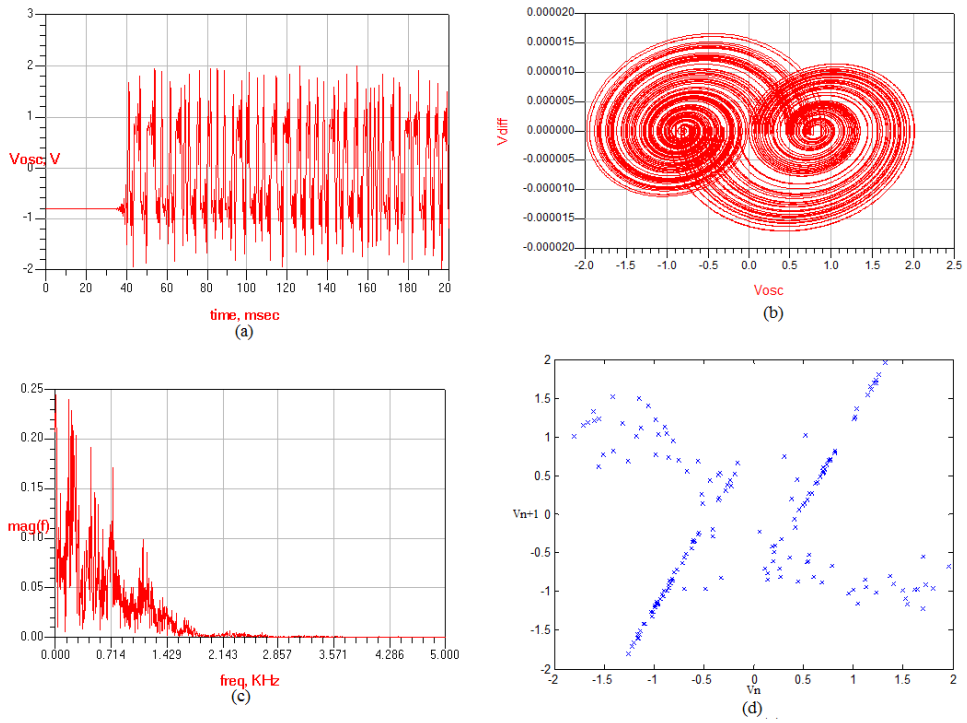

Figure 11: Chaotic output at 1 kHz where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

As we can see in Figure 11 the same results obtained for the 10 Hz frequency were obtained for the 1 kHz. The circuit showed to be working for these two frequencies. The same results were obtained for 100 kHz.

The following values were used: -R = -50 Ω, L = 2mH and C = 12.66uF.

3.2.2 Study at High Frequencies

I. For a base frequency of 1 MHz, the following results were obtained:

The following values were used: -R = -50 Ω, L = 2uH and C = 12.66nF.

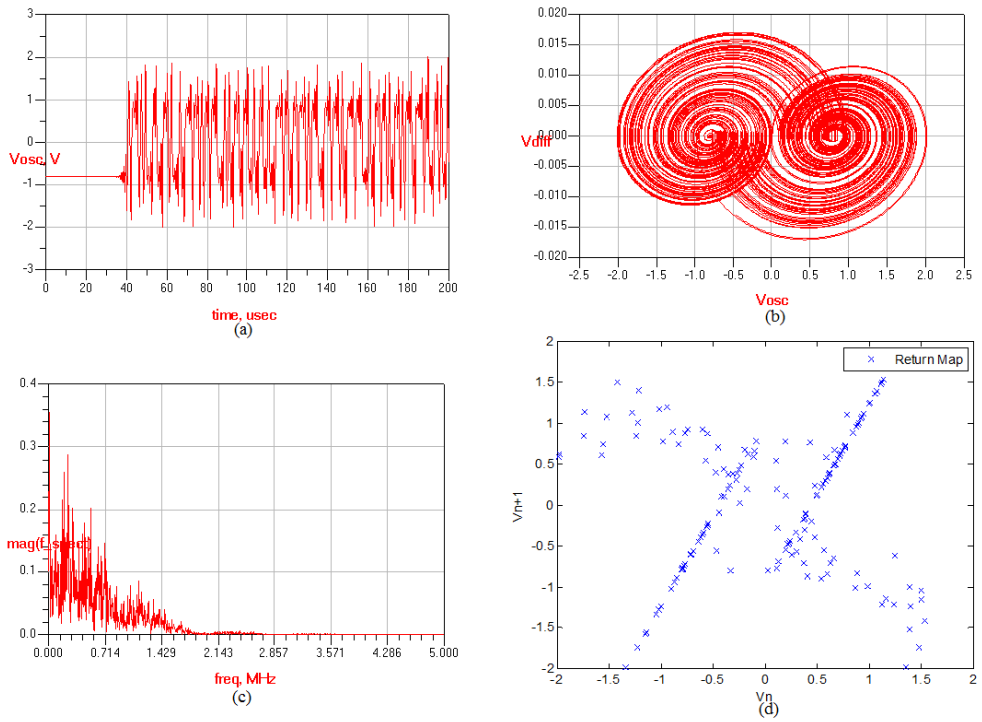

Figure 12: Chaotic output at 1 MHz where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

Figure 12 shows that the circuit is also functional at 1MHz. At this frequency and higher, the delay starts to play a role. The effect of the delays wasn't studied for lower frequencies since the most recent technology can achieve propagation delays less than 1 ns.

The effect of the delay was tested for different values (10, 20 and 30 nsec). The block "switch controller" in Figure 9 controls the amount of delay added to the chaotic circuit. The following results were obtained:

1. For 10 ns of propagation delays:

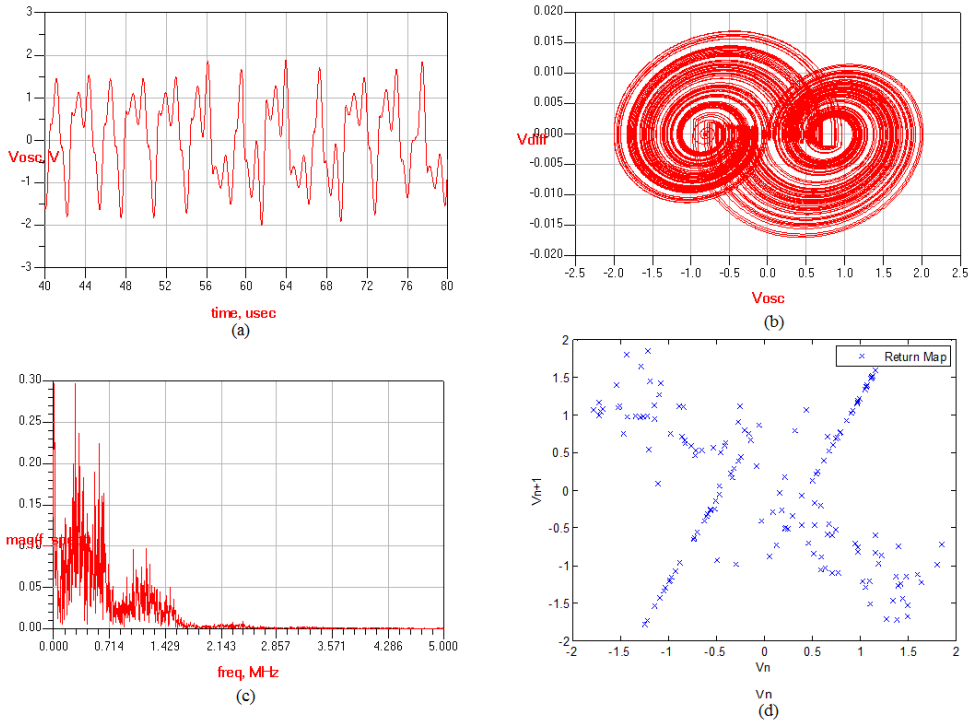

Figure 13: Chaotic output at 1 MHz with 10 ns delays where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

As shown in Figure 13 above, a delay of 10 ns does not affect the chaotic nature of the signal. The signal continues to be chaotic as can be inferred from the return map.

2. For 20 ns of propagation delays:

As can be seen from the return map in Figure 14, the chaotic behavior of the circuit is still apparent, but more non-linearities were introduced by the higher propagation delay.

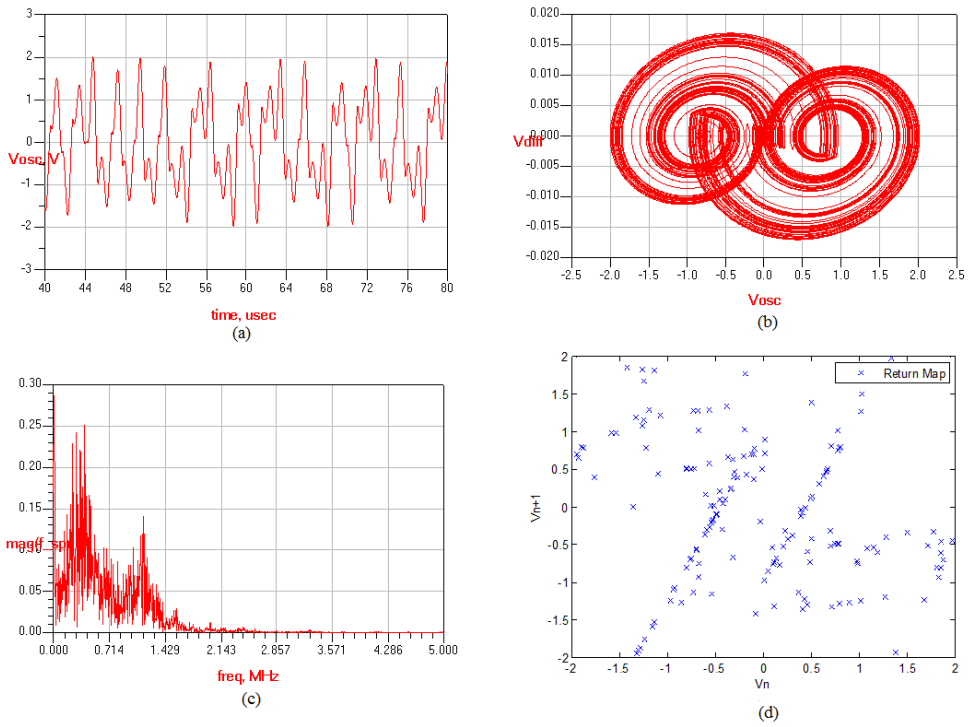

Figure 14: Chaotic output at 1 MHz with 20 ns delays where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

3. For 30 ns of propagation delays:

At this point, the delays became very high, the circuit stopped generating any chaotic signals. The form of the output signal is closer to a normal sinusoidal signal with some noise, and the return map showed that no chaotic behavior is present in the signal. The frequency spectrum of the signal shows that the signal is no longer a

broadband signal, instead a sinusoidal wave at a frequency of 420kHz is generated with its harmonics as summarized in Figure 15.

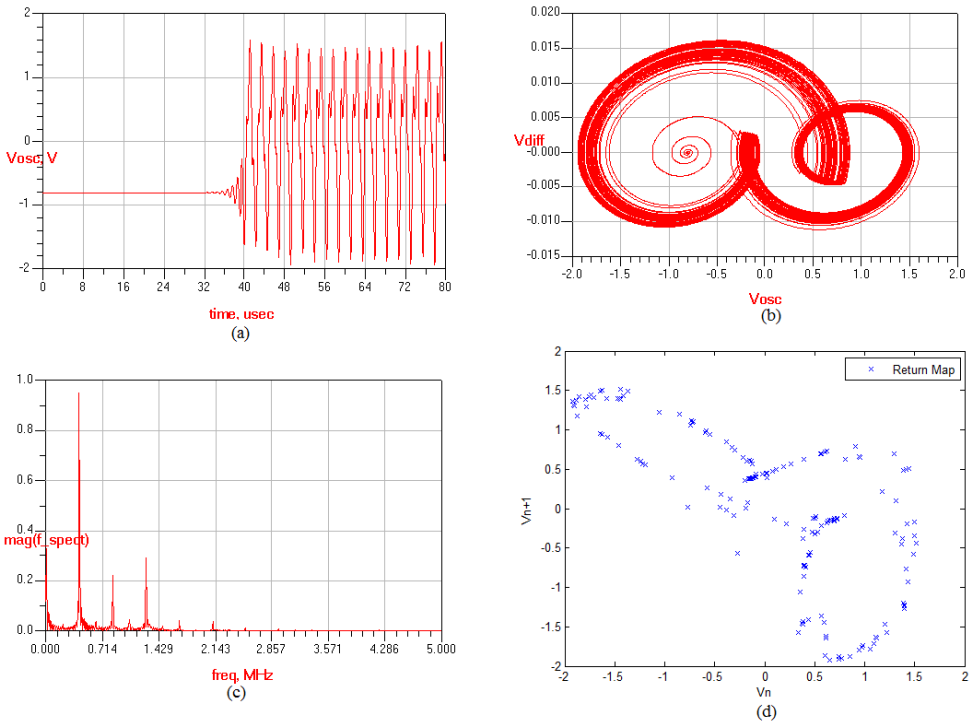

Figure 15: Chaotic output at 1 MHz with 30 ns delays where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

At this frequency, for a delay value equals to 30 ns, the chaotic signal can't be generated. The delay forms approximately 0.03 of the fundamental period of the chaotic signal being generated.

II. For a base frequency of 100 MHz, which is the targeted frequency for this thesis, the following results were obtained:

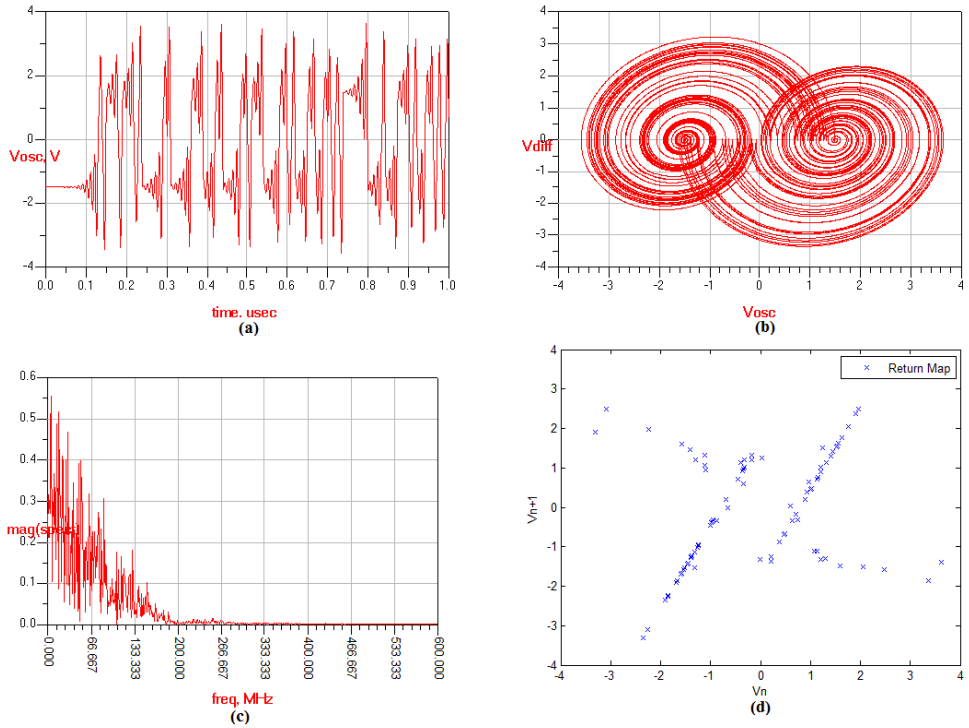

Figure 16: Chaotic output at 100 MHz where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

Figure 16 shows that the circuit works at 100 MHz. A chaotic signal has been generated as the return map shows.

The following values were used: -R = -400 Ω, L = 160 nH and C = 15 pF.

When the propagation delays were introduced to the circuit (0.1, 0.2 and 0.3 nsec), the following results were obtained:

1. For 0.1ns delays, the following results were obtained:

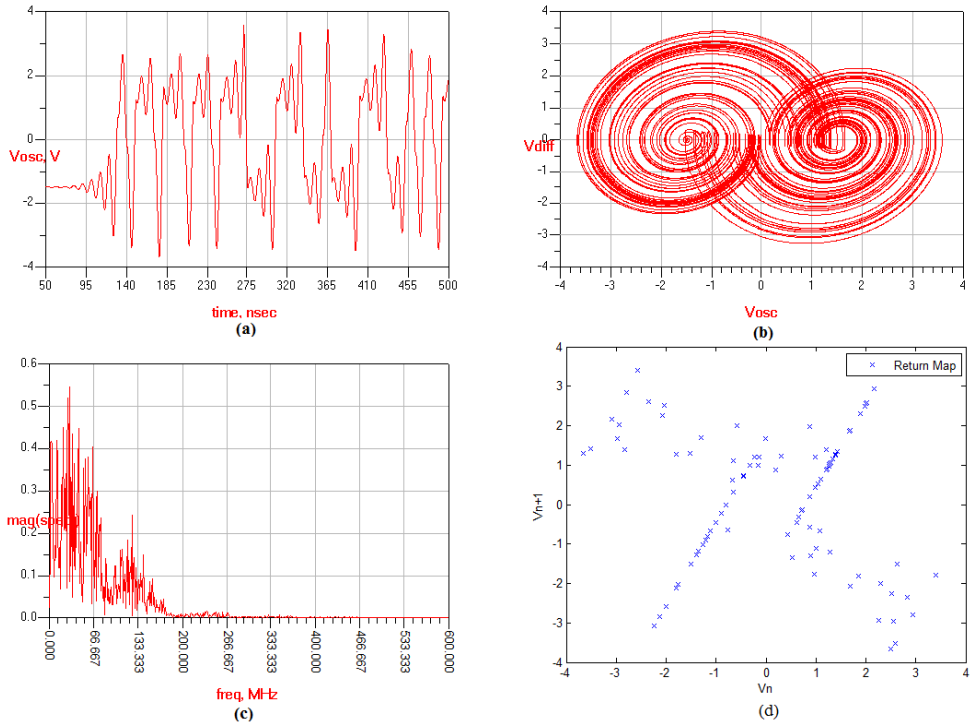

Figure 17: Chaotic output at 100 MHz with 0.1ns delays where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

As we can see from Figure 17, the 0.1 ns didn't affect the generation of a chaotic signal. The chaotic behavior of the signal is clearly apparent.

2. For 0.2 ns delays, the following results were obtained:

In Figure 18, and similarly to lower frequencies, the circuit is still generating a chaotic signal, but nonlinearities in the signal are more apparent. The results in the return map, and the "dV vs V" plot show that a chaotic behavior is still existent in the signal, but extra nonlinearities are added. Any slight additional delays will cause the circuit to not generate any chaotic signals.

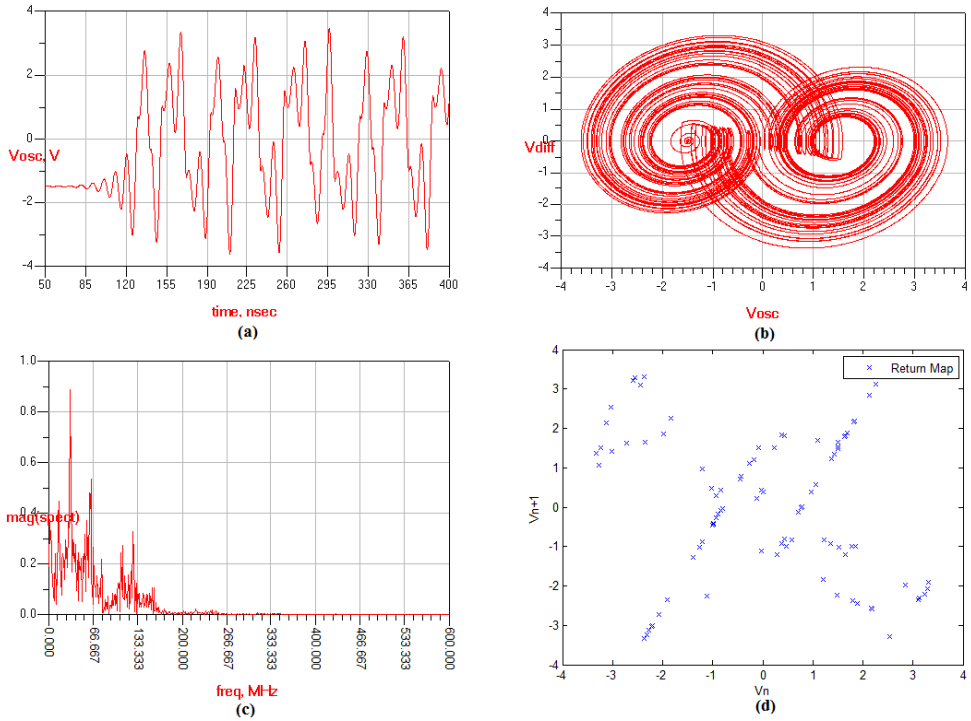

Figure 18: Chaotic output at 100 MHz with 0.2ns delays where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

3. For 0.3ns delays, the following results were obtained:

The plot of the voltage versus time in Figure 18 shows that no chaotic oscillations exist. The generated signal can be described as parasitic oscillations around zero. The return map shows that no chaotic behavior is present in the generated signal, and that all the elements of the "Vn" series are close to zero. At this delay values, the circuit is unable to generate any chaotic signals.

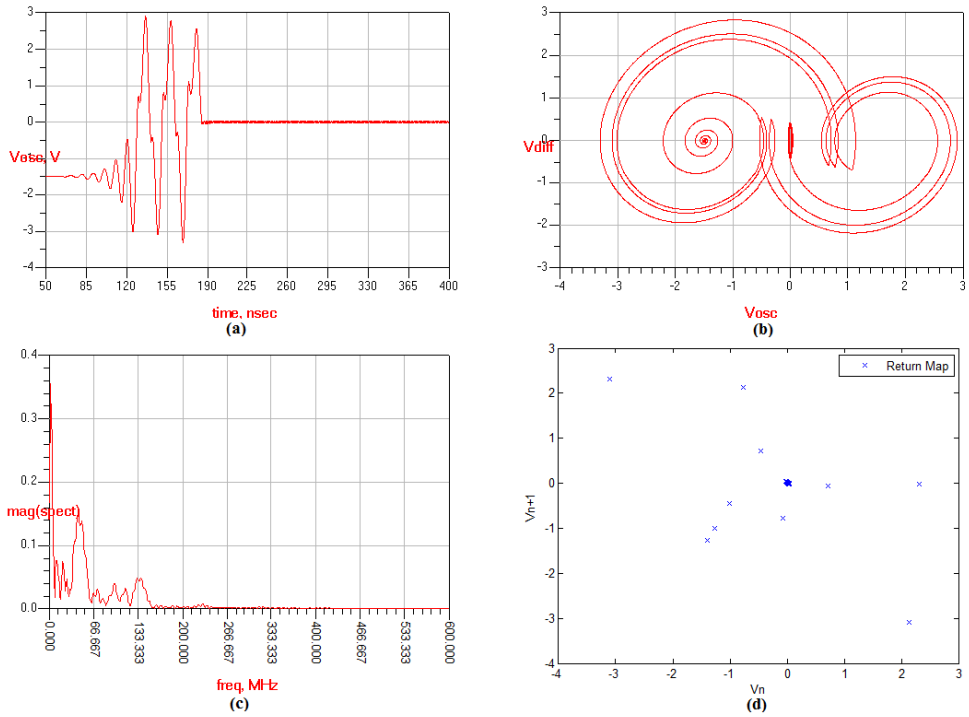

Figure 19: Chaotic output at 100 MHz with 0.3ns delays where, (a) shows Vout vs time, (b) shows dVout vs Vout, (c) shows the frequency spectrum of the signal and (d) shows the return map.

At this frequency, the value of the delay that suppressed the generation of chaotic signals was 0.3ns. This values is a 0.03 fraction of the base frequency period (10 ns in this case).

This same study was performed on other frequencies in order to come up with a general rule on how much delays can be tolerated for the generation of coherent chaotic signals. The following was concluded:

- For a delay value of 0.02*(Period of the base frequency), the circuit can generate chaotic signals.

- For a delay value of 0.025*(Period of the base frequency), the circuit is no longer able to generate any chaotic signals.
- For a delay value between 0.02*(Period of the base frequency) and 0.025*(Period of the base frequency), at some frequencies the chaotic signal was still generated and at some other frequencies it was supressed.

3.3 Summary

In this chapter, the architecture of the chaotic oscillator is illustrated, the requirements of the chaotic oscillator using an analog implementation is studied, and a rule concerning the maximum allowed delay is devised.

Chapter 4. Chaotic Oscillator Design Difficulties

From the previous chapter, it was determined that a 0.25ns delay value is acceptable for the generation of the coherent chaotic signal using the circuit architecture proposed by Corron *et al.* In this chapter, the design of the different parts of the circuit is presented, and the difficulties faced in the design of a chaotic oscillator are explained.

4.1 Oscillator design

The transistor used for the design of the oscillator is AT-41486 from Avago technologies. The transistor (BJT) has an 8GHz gain bandwidth, which is recommended for low noise RF circuit designs. The oscillator should be oscillating at 100 MHz.

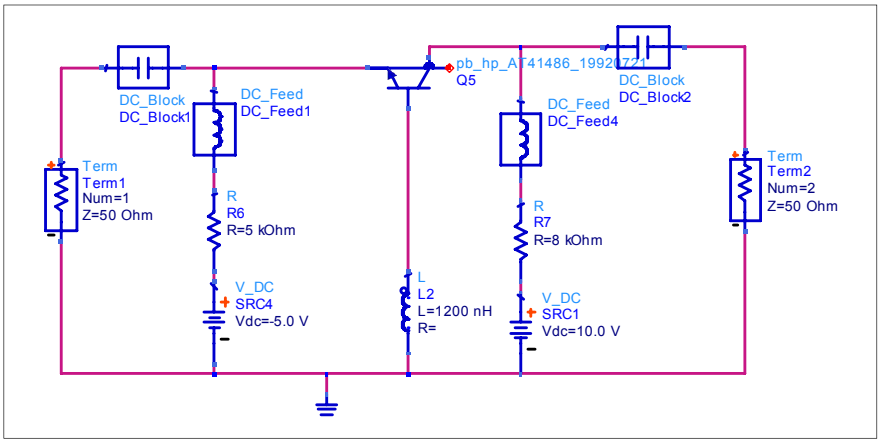

Figure 20: Biasing Circuit.

1. Biasing Circuit:

The transistor biasing circuit is shown in Figure 20. The aim of the biasing circuit is to make the transistor work in the unstable region, for it to create increasing oscillations with the appropriate matching networks. In other words, the biasing circuit

should change the $|S_{11}|$ and $|S_{22}|$ of the biased transistor to a value greater than 1 to achieve instability inside smith chart.

In order to create instability, an inductor (1200nH) was incorporated between the base of the BJT and the ground. The S-parameters of the resulting network is shown in Table 1 below:

S-Parameters	S_{11}	S_{12}	S_{21}	S_{22}
Value	$1.926\angle 156.33$	$0.366\angle 163.76$	$2.84\angle -19.195$	$1.35\angle -6.15$

Table 1: Oscillator Biasing network S-parameters

The resulting stability circles are shown in Figure 21:

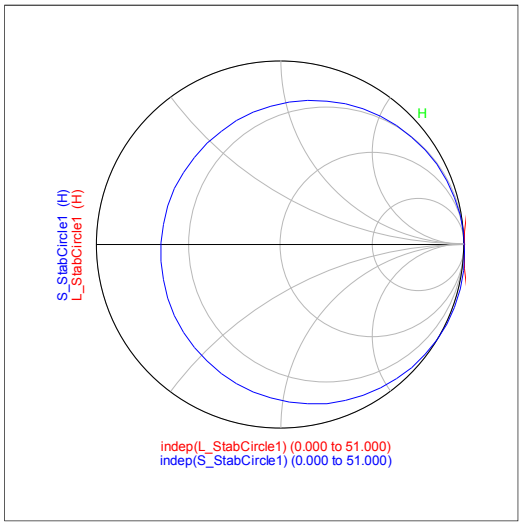

Figure 21: Oscillator stability circles

2. Matching Networks

The oscillator stability circles show that any value of Γ_T can be chosen on the smith chart will result in a $\Gamma_{in} > 1$, hence, an unstable biased transistor.

By choosing $\Gamma_T = 0.5i$, we get $\Gamma_{in} = \frac{S_{11}-\Delta\times\Gamma_T}{1-S_{22}\times\Gamma_T} = -1.7561 + j0.3297$

hence, Z_{in} =-14.228 +j4.2788. For maximum power transfer, we use X_L = -X_{in} and R_L = |R_{in}|/3. Which means that Z_L = 4.74 - j4.2788 and $\Gamma_L = 0.8279\angle -170.127$.

The load matching circuit is shown in Figure 22:

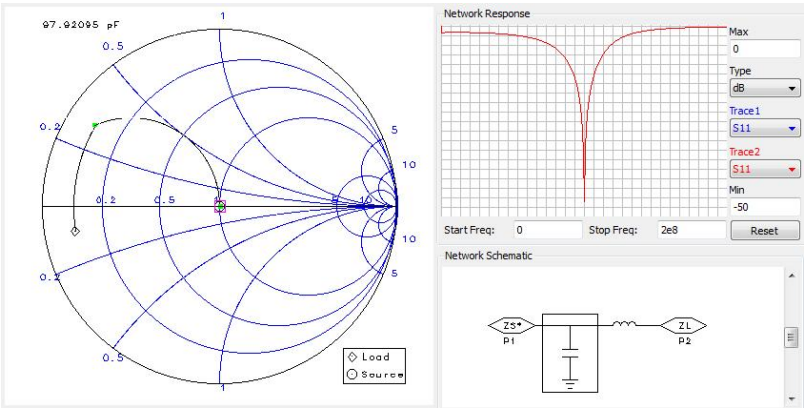

Figure 22: Load matching circuit and smith chart.

The chosen capacitor and inductor values are: C = 98 pF, L = 30nH.

The termination matching circuit is presented in Figure 23:

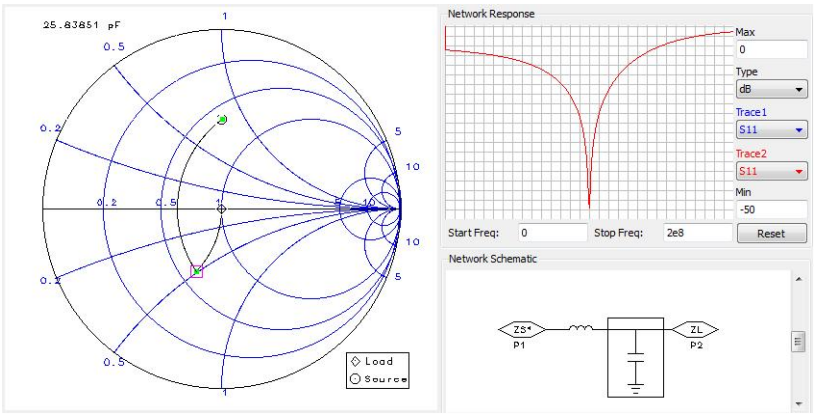

Figure 23: Termination matching circuit and smith chart.

The termination matching circuit determines the oscillating frequency of the oscillator, thus, it can be replaced by a capacitor and an inductor in parallel, with the values consistent with the following equation:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

For this matter we chose: L = 160nH and C = 15 pF.

3. Tweaking of Circuit Parameters

By tweaking some parameters at the load side, the output voltage of the oscillator was increased and the noise level was decreased after performing the following modification:

- The 50Ω termination was removed.

- The inductor was shortened.

- The capacitor value was changed to 30pF instead of 98pF.

Figure 24 shows the final oscillator design and its output:

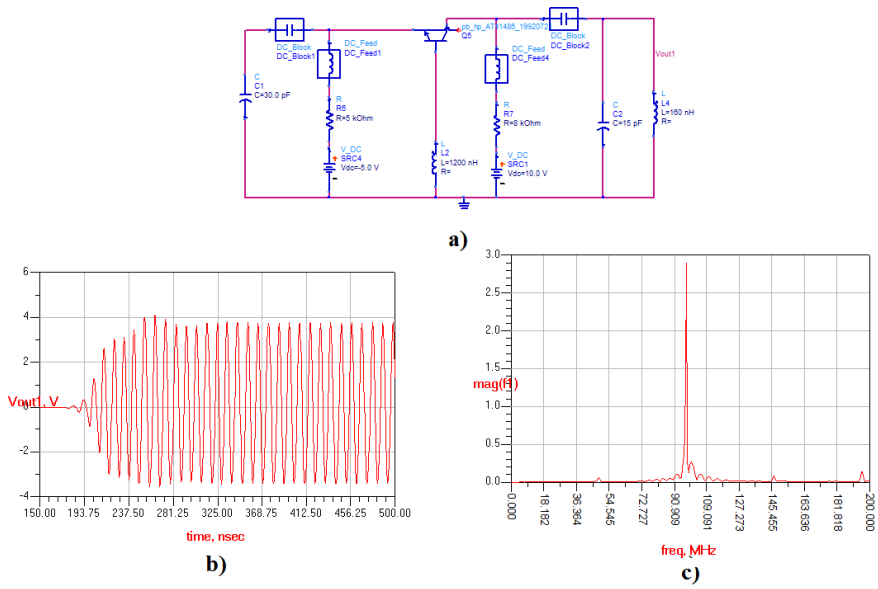

Figure 24: a) Oscillator circuit at 100MHz, b) Oscillator output signal and c) Frequency spectrum of the output signal showing oscillations at 100 Mhz

4.2 Differentiator design

In order to compute the derivative of the generated oscillator signal, a differentiator was designed using coupled microstrip lines technique. The differentiator works with both single ended or differential circuits. At the input port, the differentiator is matched to 50 Ω using a microsrip line. Then two other sections of microstrip lines with different widths, connect the input port to the coupled microstrip lines. The coupled lines are connected to the output port, as shown in Figure 25. The variation in the width of the microstrip lines along with the coupled lines secures the derivative functionality. The different sections of the differentiator have the following dimensions as shown in Table 2:

Table 2: Differentiator Dimensions.

Differentiator Section	Width (mm)	Length (mm)
Input port line	1.766	12.36
First Section	1.6	10
Second Section	1.43	7.5
Coupled Lines	0.523	10.5

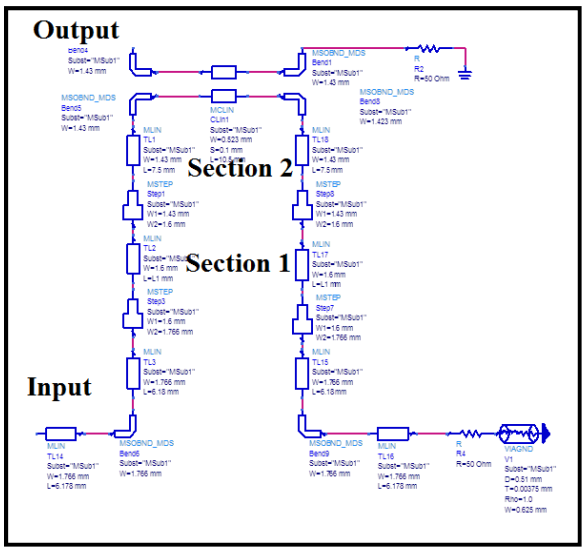

Figure 25: Differentiator Schematic

The separation between the coupled lines controls the output signal magnitude. Since the minimum separation that could be achieved in the antennas lab at UNM is 0.1mm, the separation used in the differentiator is s = 0.1mm. The output signal of the differentiator is shown in Figure 26.

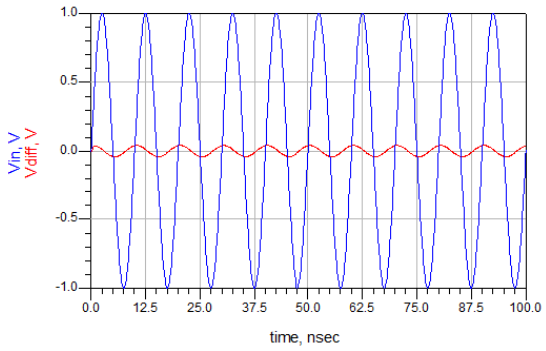

Figure 26: Differentiator input signal (in blue), differentiator output signal (in red).

Since the output signal of the differentiator has a very low voltage amplitude, it attenuates the magnitude of the input by 20 times, a low noise amplifier (LNA) was needed to amplify the signal. A capacitor acting as a filter was added to remove the higher frequencies created by the noise. The designed LNA with the filter, has a 15.3 dB gain and a 1.08 dB noise figure. The output of the amplifier is shown in Figure 27: Input voltage to the differentiator (in red), Output voltage of the differentiator (blue) and output voltage of the LNA (pink).Figure 27.

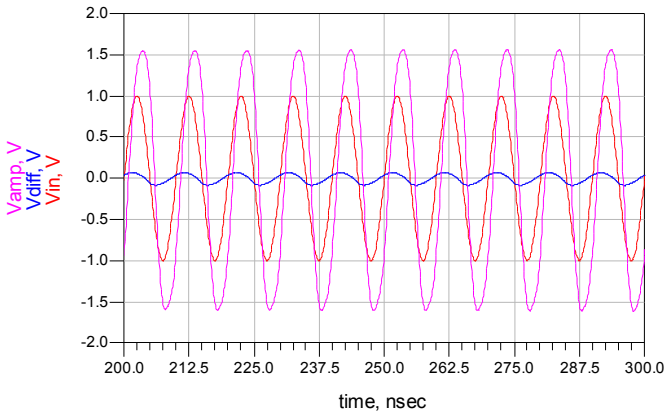

Figure 27: Input voltage to the differentiator (in red), Output voltage of the differentiator (blue) and output voltage of the LNA (pink).

4.3 Comparator, Logic Gates and Multiplexer

In the oscillator control unit shown in **Figure** 3, is implemented using voltage comparators, 2:1 multiplexer and logic gates (AND gate and an OR gate). The following components are the fastest components that can be used in the oscillator implementation. These components are manufactured by Hittite Microwave Corporation. Table 3 shows their characteristics:

Table 3: Digital components characteristics.

Component Name	Functionality	Rise/Fall Time	Propagation Delay
HMC674LC3C	Comparator	24/15ps	85ps
HMC843LC4B	AND/OR	10ps	10ps
HMC954LC4B	Multiplexer	15ps	113ps

The search for digital components focused on having the least propagation delays as a first criterion, then the consistency between the input and output voltage ranges among all digital chips as a second criterion.

4.4 Design Problems

Several problems were faced during the design of the chaotic oscillator. Some of them are related to non-linearity in the system, others are related to excessive delays and noise. The different design problems are detailed below:.

1. **Non-linearity caused by the BJT used in the oscillator design:**

By checking the response of the designed oscillator in the system, with ideal components, the output chaotic signal showed non-linearity.

The phase space projection of the output signal shown in Figure 28. It no longer shows two elliptical trajectories. This is due to the non linear behaviour of the BJT used in the design of the oscillator.

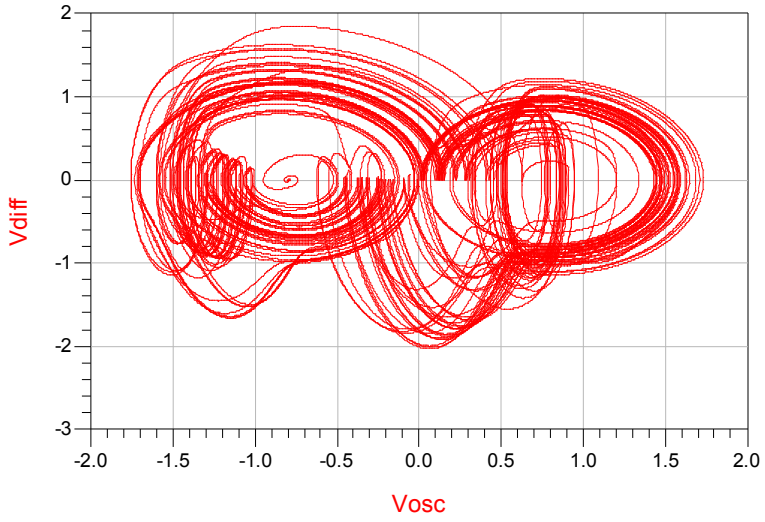

Figure 28: Phase space projection of the output signal while using the designed oscillator with ideal components

2. **The differentiator and LNA propagation delay is higher than the maximum allowable delay:**

   The differentiator introduced a 0.6 ns delay to the system. An LNA is added since the output of the differentiator has low amplitude, to avoid errors in the comparator's result. Consequently, the LNA introduced by itself a 1 ns delay. The total delay introduced by differentiating the signal is 1.6 ns.

   The delay is related to the length of the microstrip lines used in the system. In order to reduce these delays, the length of the microstrip lines in both differentiator and LNA are tweaked. When the length of the coupled microstrip

lines in the differentiator is changed, a change in the amplitude of the output signal is also noticed. This means, by increasing the length of the coupled lines, the amplitude of the differentiator output signal is increased. This has the advantage of removing the LNA from the system and reducing the delay by 1 nsec. However, additional delays are added due to the increase in the length of the coupled lines. After choosing the necessary length of the coupled lines which is 17 cm for the coupled lines, the total delay of the differentiator is 1.1ns, which is still very high.

3. **The total delay in the rest of the components is very close to the maximum allowable delay.**

   The total delay of the rest of the chaotic oscillator components is 228 ps. This leaves 22 ps worth of delays for the differentiator and the buffers used to remove the loading effects from the circuit.

4. **The un-even delays in the different parallel sections of the oscillator sections:** After the oscillator, the system is divided into two sections working in parallel. As mentioned in Chapter 3, the first section starts with a differentiator and the second starts with a comparator. Therefore, nonlinearities have been added since the signal needs more time in the first section than the second one. Hence adding a delay line in the second section is necessary to remove this non-linearity.

As a conclusion, due to the lack of very fast components, this chaos oscillator is non- realizable. The maximum frequency that could be implemented using the same architecture and the same components is 17 MHz.

4.5 Summary

In this chapter, the design of the chaotic oscillator according to the architecture proposed in the previous chapter is discussed. The problems faced are the high delays, the nonlinearities introduced by the BJT and the uneven delays in the different sections of the oscillator.

Chapter 5. Antenna Design

After the generation of the chaotic signal, it should be up-converted to the frequency range 71-76GHz, and then transmitted using an antenna operating at this frequency range. The antenna is used in a collision avoidance system, which means that it should have a directional beam. The antenna under study is an array of patch antennas. At this frequency range, it is hard to feed this antenna, because it can't be fed through an SMA connector. They only operate at the frequency range 0 - 26.5GHz. In this Chapter, the array of patch antennas is presented. The two feeding techniques that can be used are discussed. The first uses an RF Probe and the second uses a rectangular waveguide WR-12.

5.1 Single Patch Design

The substrate that is used to design and fabricate the antenna is Rogers 3003. This substrate is recommended for applications up to 77GHz. The board has a 0.13mm thickness, 3.02 dielectric constant and 0.0013 tan(δ) at 10 GHz. The narrow thickness is chosen to minimize the dielectric material losses which affects the efficiency of the antenna, and the characteristic impedances of the feeding lines. Among the substrates recommended to be used for applications in the E-band, the ones with a lower dielectric constant, create a problem in the matching between the rectangular waveguide and the feeding lines of the array. The ones with a higher dielectric constant are not intended for antenna design, because they negatively affect the radiation efficiency of the antenna.

As a first step after choosing the substrate, a single patch is designed with a microstrip line as the feeding line as shown in Figure 29. This step is done to find the

preliminary dimensions of the patch antenna. The following equations are used to find the dimensions of the patch [20]:

$$W = \frac{c}{2f_r}\sqrt{\frac{2}{1+\varepsilon_r}}$$

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1+12\frac{h}{W}}}$$

$$\Delta L = 0.412h\frac{(\varepsilon_{reff} + 0.3)\left(\frac{W}{h} + 0.264\right)}{(\varepsilon_{reff} - 0.258)\left(\frac{W}{h} + 0.8\right)}$$

$$L = \frac{c}{2f_r\sqrt{\varepsilon_{reff}}} - \Delta L$$

where "L" is the patch length, "W" is the patch width and "c" the speed of light in free space.

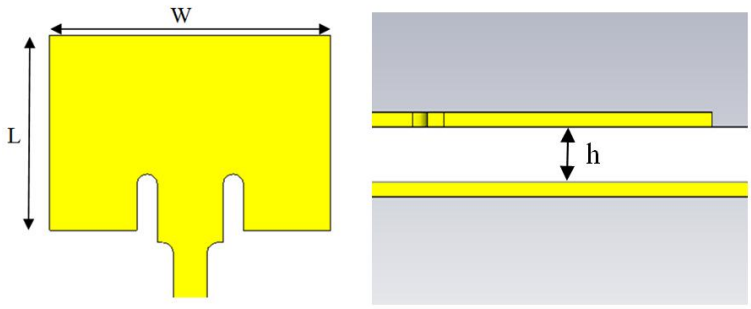

Figure 29: Patch Antenna

The primary results give a patch width W = 1.4 mm and a patch length L = 1.2 mm.

For feeding the patch, an inset feed technique is used, since using a quarter wave transformer between R_{in} = 360 Ω and Z_0 = 50 Ω requires a characteristic impedance of $Z_0 = \sqrt{50 \times 360} = 134.16\,\Omega$. This characteristic impedance corresponds to a microstrip line of 34μm which creates a fabrication problem.

By using the inset feed technique, the resulting inset needed is 0.35mm to match the patch to a feeding line of 50Ω characteristic impedance. This value is found by using the following formula [20]:

$$\text{inset} = \frac{L}{\pi} \times \arccos\left(\sqrt{\frac{R_{in_{wanted}}}{R_{in}}}\right)$$

The gap in the inset feed is 0.11mm because the smallest milling head has a diameter of 0.1 mm.

The previously calculated dimensions give a preliminary estimate of the dimensions that make the patch radiate in the frequency range needed. By simulating the patch with the above mentioned dimensions, no resonant frequency is found in the frequency range of interest. A tweaking in the length and width of the patch showed a resonance between 71-76 GHz. The length is close to 1.04mm and the width is close to 1.5 mm.

The feeding of the patch is challenging since the SMA connector cannot be used to feed the patch since it only operates at frequencies up to 26.5 GHz. Therefore, two different feeding techniques are investigated to feed the array of patches either through an RF probe or through a WR12 rectangular waveguide.

5.2 Feeding Techniques

1. RF Probe technique:

RF probes can support E-band operable signals and can be used to feed the array of patch. RF probes have different configurations. The one used for the feeding of the array has a Ground Source Ground (GSG) configuration. This necessitates a transition from Grounded CPW (GCPW) to microstrip line. The probe should be touching the GCPW and will be injecting its signal to the antenna.

The design of the transition from GCPW to microstrip line is presented. The transition is designed based on the model suggested by Papapolymerou in [18]. The transition consists of GCPW with a slowly increasing gap. The coupling between the center line and the upper ground plane decreases gradually until it vanishes and becomes a microstrip line. The width of the center line increases gradually until it matches the width of the microstrip line. Figure 30 shows the RF probe along with the different transition designs. Figure 31 show the transition design and its different sections.

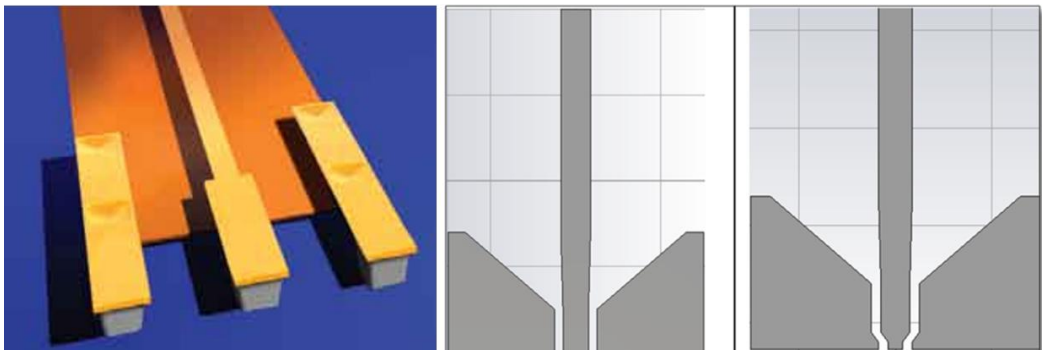

Figure 30: RF Probe layout (left), Proposed GCPW to Microstrip-line (middle), Modified to Microstrip-line (right).

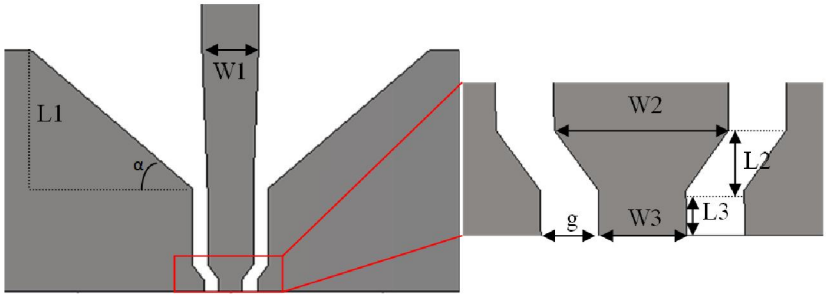

Figure 31: The design of the GCPW to Microstrip line transition

In order for the RF probe to fit on the GCPW, the design is slightly changed and a narrower center line width section is added to the input of the transition (since the RF probe has a pad width of 25x35 μm and a pitch of 0.25mm) as shown in Figure 30. The narrower center line section's length is optimized in order to prevent a mismatch between the feeding line and the transition. Figure 31 shows the different parameters of the modified GCPW to Microstrip line transistion and Table 4 shows the different dimensions of the transition. Figure 32 shows the S-Parameters corresponding to the designed transition.

Table 4: The dimensions of the different sections of the GCPW to Microstrip line transition.

Section	Dimension	Description
L1	0.9 mm	Transition length
L2	0.5 mm	Probe Pads to GCPW transition length
L3	0.075 mm	Pad length
W1	0.35 mm	Microstrip line width
W2	0.3 mm	GCPW line width
W3	0.15 mm	Pad width
g	0.11 mm	GCPW gap width
α	40.6^{o}	The angle in which the upper ground gap increases

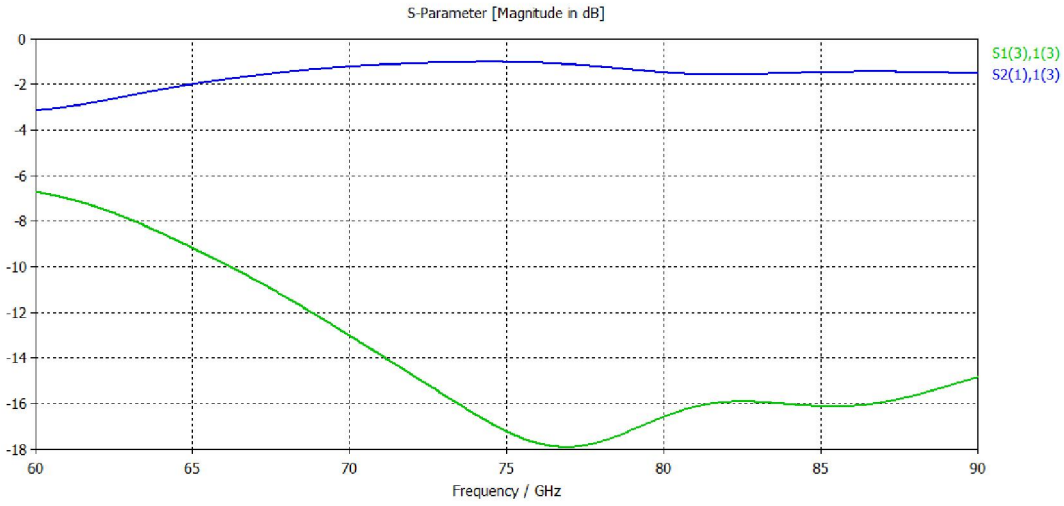

Figure 32: The S_{11} and S_{21} corresponding to the modified GCPW to microstrip line transition

According to the results obtained, the transition has an -1.2dB <S_{21}<-1.04 dB over the frequency range 71GHz to 76 GHz. This result implies that the designed transition

passes on the power from port 1 to port 2 with minimal losses over the frequency range of interest.

WR12 Waveguide Technique:

The design of this feeding technique is based on the design suggested by Kazuyuki Seo et al. [19] for Microstrip to waveguide transition.

In this technique, a rectangular waveguide is used to feed the antenna. A WR12 rectangular waveguide is fed with the power to be radiated. The other end of the WR12 is coupled to a microstrip line, which by itself, feeds the array of patches. The top and bottom view of the rectangular waveguide to Microstrip-line are shown in Figure 33.

The coupling circuit consists of the following parts:

a) A rectangular patch that receives the power from the WR12 and couples it back to the microstrip line.
b) The dielectric material used in the array design.
c) A ground plane that terminates the WR12 and suppresses any radiation.
d) A CPW that transforms into a microstrip line.

The first layer at the other end of the WR12 consists of the rectangular patch. The patch's length is L_1 = 1.02 mm and its width is W_1 = 2.04 mm. The width should be twice as long as the length in order to get a better coupling. Then, the second layer consists of a ground plane that is used to terminate the waveguide. The ground plane has a width and a length greater than the WR12's width and length by approximately λ/4. This extra λ/4 in dimensions servers the purpose of shorting the ground plane to the side walls of the

WR12 hence, connecting the ground planes of the entire design. The microstrip line emerges from the ground plane and feeds the array. Between the two layers, a dielectric material with a relative dielectric constant of $\varepsilon_r = 3.01$ is sandwiched.

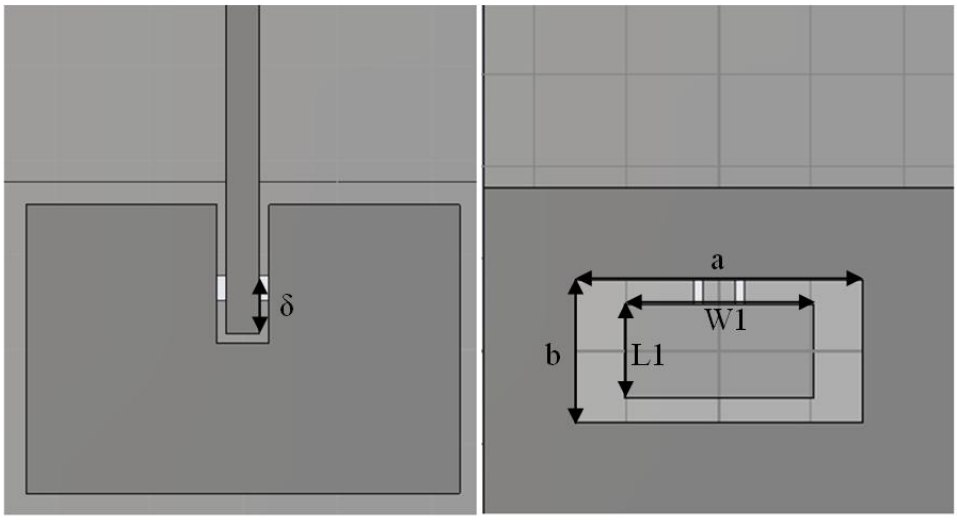

Figure 33: Microstrip to Rectangular Waveguide Transition.

Figure 34 and Table 5 show the different sections of the transition, and the dimensions of the different elements of the transition.

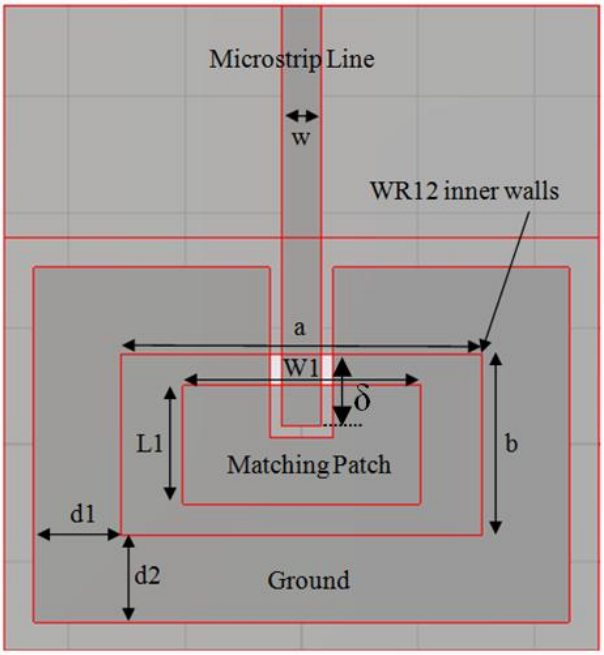

Figure 34: The different elements of the Microstrip to Rectangular Waveguide transition

Name	Dimension (mm)	Description
a	3.1	WR12 cross section width
b	1.55	WR12 cross section length
w	0.35	Microstrip line width
W1	2.04	Matching patch width
L1	2.02	Matching patch length
d1	0.72	Difference in width between ground plane and WR12
d2	0.72	Difference in length between ground plane and WR12
δ	0.35	Length of the Microstrip line intersecting the WR12 aperture

Table 5: The dimensions of the different parts of the Microstrip to Waveguide transition.

Results:

The simulation results show that the S_{21} is greater than -0.6 dB which implies total transmission from port 1 to port 2. Also S_{11} is less than -10 dB on the entire frequency range of interest which means that more than 66.67% of the incident power is transmitted and less than 33.33% is reflected as shown in Figure 35.

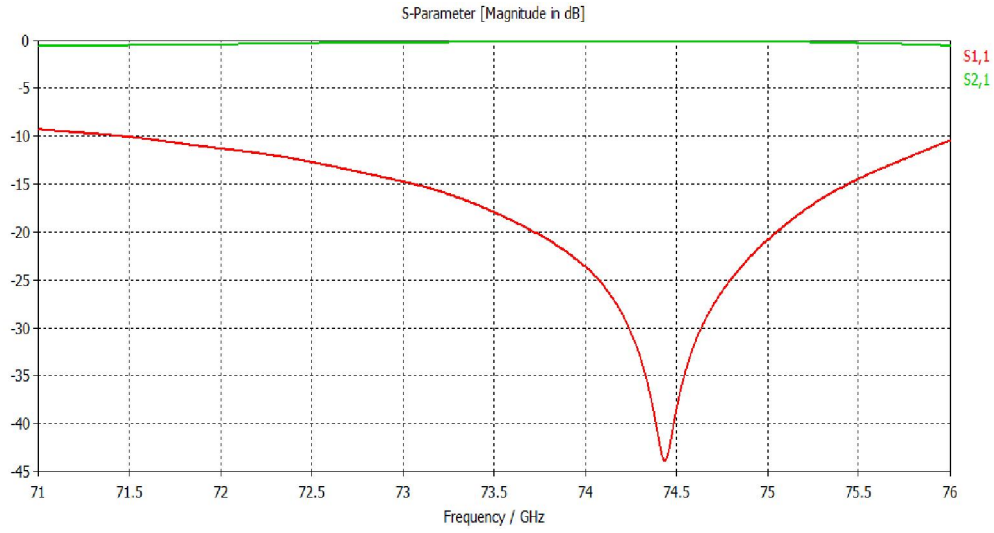

Figure 35: The S11 and S21 of the Microstrip to Waveguide transition.

Comparison of the Two Feeding Techniques:

For a load of 50Ω, the GCPW to Microstrip transition had a wider transmission band of approximately 25 GHz (using the -2dB criterion), whereas the Waveguide to Microstrip transition had a transmission band of approximately 5 GHz.

5.3 Array Design:

An 8x8 array of patches is designed. Two designs are shown with the two different feeding techniques discussed before. A corporate feed is used to feed all the patches with no phase shift, since in our collision avoidance system we need two symmetrical directional beams in order to determine the direction of the obstacle to be avoided. The corporate feed consists of a primary feeding line of $Z_0 = 50\Omega$. This line splits into two parallel lines of $Z_0 = 100\Omega$. Then each of these two lines is matched to another line of $Z_0 = 50\Omega$, by the use of quarter wave transformer of $Z_0 = 70.7\Omega$. Then the 50Ω line splits again in the same way that was previously described.

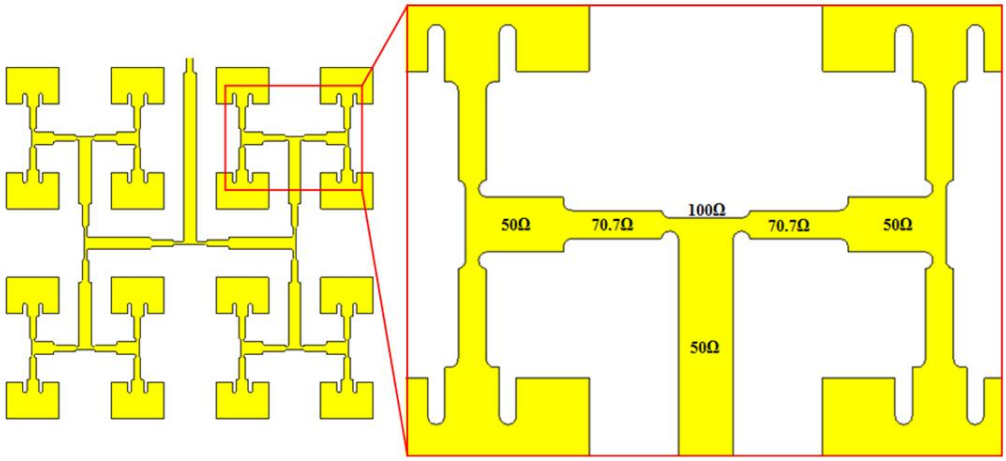

Figure 36: Illustration of the corporate feed used to feed the patches.

For more simulation precision, the thickness of the copper is taken into consideration because its value is not negligible when compared to the effective wavelength λ_r. The circular shape of the etching head is also considered in the modeling

of the patches and the feeding lines in the fabricated design, because the smallest etching tool has a diameter of 0.1mm which is also comparable to the wavelength λ_r.

5.4 Patch array fed using an RF probe:

In Figure 37, the design of the array fed using an RF probe is shown. The patch elements have a length L = 1.04mm and a width W = 1.65mm. The separation between the patches is 1.25 λ_r.

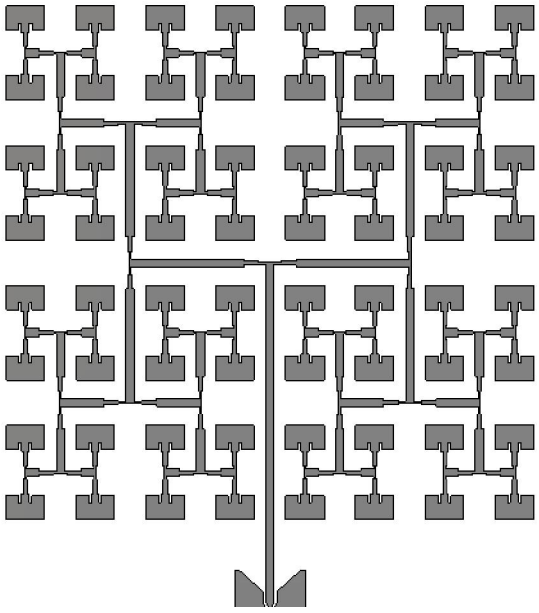

Figure 37: Patch array (8x8) fed using an RF probe.

The antenna simulation is performed using CST Microwave Studio (CST-MWS). The S-parameters, radiation pattern and realized gain of the antenna are discussed.

The antenna S-parameters result is shown in Figure 38. The -10 dB bandwidth of the antenna is approximately 3.75 GHz from 71 -74.75 GHz. The -20 dB bandwidth is1.85GHz from 72.15-74GHz. This bandwidth is considered to account for the losses in the dielectric material. The antenna resonant frequencies are at 72.5 and 73.7 GHz.

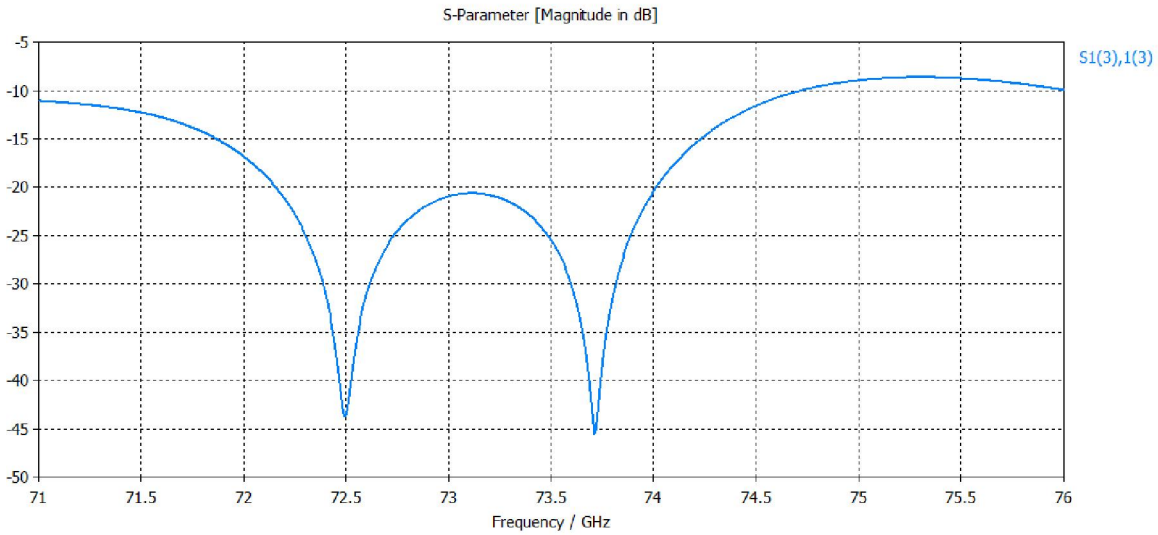

Figure 38: S-Parameters results of the probe fed array.

By examining the gain of the antenna, we realize that the realized gain is around 18.9 dB at 73.5 GHz, as shown in Figure 39. The antenna radiation efficiency is 87% and the total efficiency, which involves the radiation efficiency and the dielectric and conductive material losses is 78%. The efficiency values of the antenna are calculated based on an approximation of the tan(δ) value by using a constant fitting.

According to the resulting 3D radiation pattern, the designed antenna has two main lobes in the plane Φ = 90° with a value of 18.9 dB, as shown in Figure 40. The main lobes direction is ±43° and their 3 dB beamwidth is 12.8°. Some other side lobes with a

side lobe level of -9.5dB are also present. The two main lobes are created by the separation between the patches, which is in our case 1.25 λ_r.

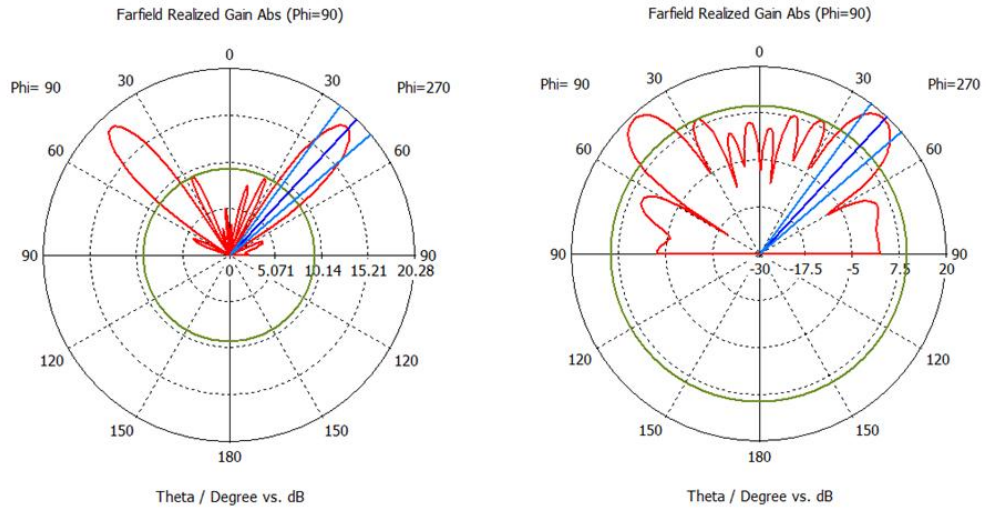

Figure 39: The gain of the array at 73.5 GHz

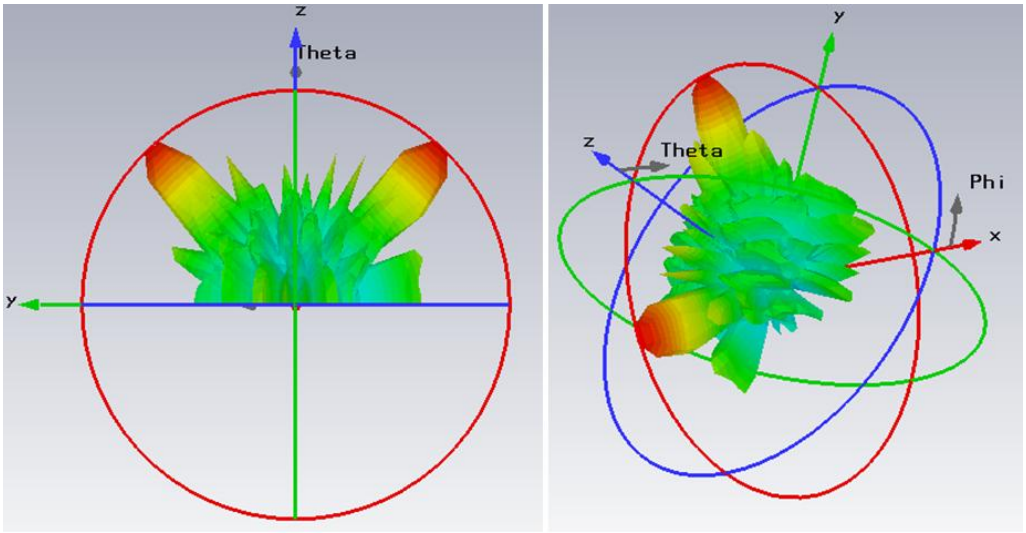

Figure 40: Radiation Pattern of the array at 73.5 GHz.

5.5 Patch array fed using WR12:

Figure 41 shows the design of the array fed through a rectangular waveguide WR12. The patches have the same length as the previously designed array (L = 1.04mm), but have a slightly different width W = 1.5mm. The separation between the elements is still 1.25 λ_r.

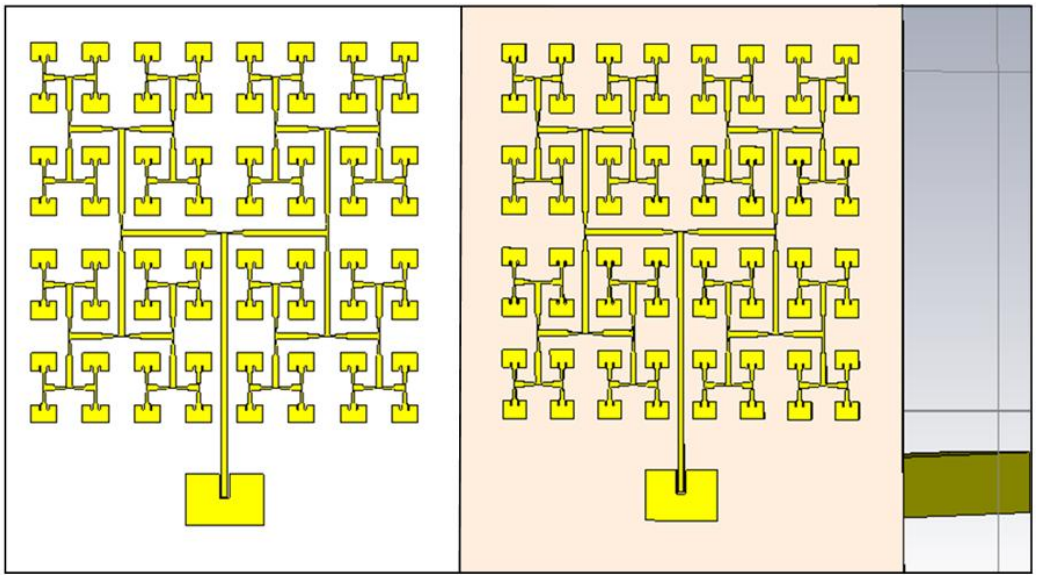

Figure 41: 8x8 Array of patches fed via a WR12 waveguide

This array is simulated using CST and HFSS, to ensure that the design is correct before fabrication. The S-Parameters results and Realized Gain plots are shown in Figure 42 and Figure 43.

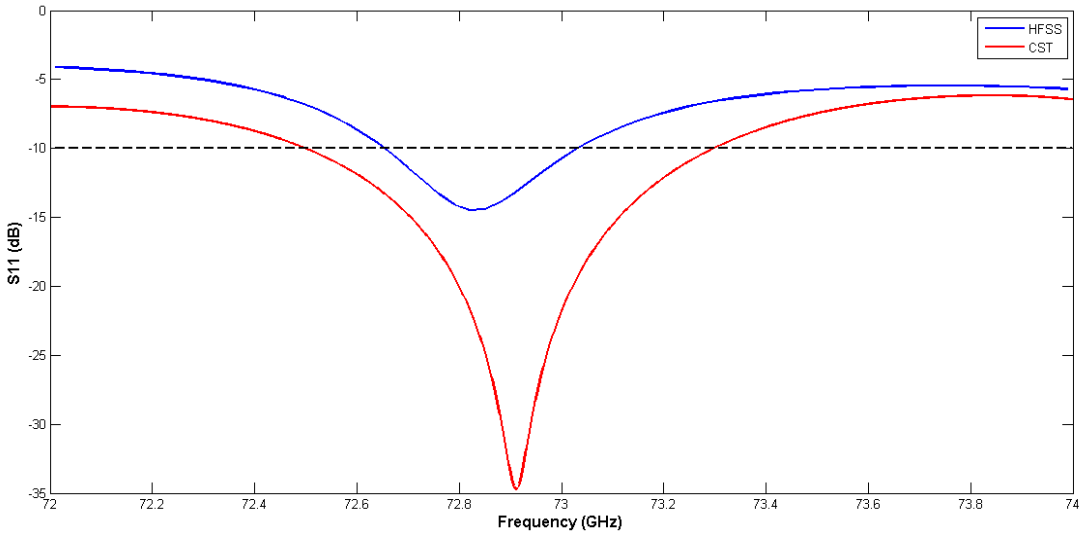

Figure 42: S11 result for the array.

The simulation results, using both softwares, show a resonant frequency between 72.8 GHz and 73GHz. The CST result shows a resonant frequency at 72.9GHz and the HFSS result shows a resonant frequency at 72.85 GHz. The bandwidth of the antenna is, according to CST, equal to 800MHz, while the one obtained in HFSS is 400MHz. Both simulations show that the antenna is able to resonate at a frequency close to 73GHz.

Now by examining the gain calculated by both simulations, we realize that the results are very close. The CST simulation predicts a realized gain of 18dB at 73GHz, and the HFSS simulation predicts a realized gain of 17.3dB. This slight difference between the two might be partially attributed to the approximations done in the calculation of tan(δ), hence, the efficiency of the antenna. The efficiency of the antenna obtained using CST is 87%.

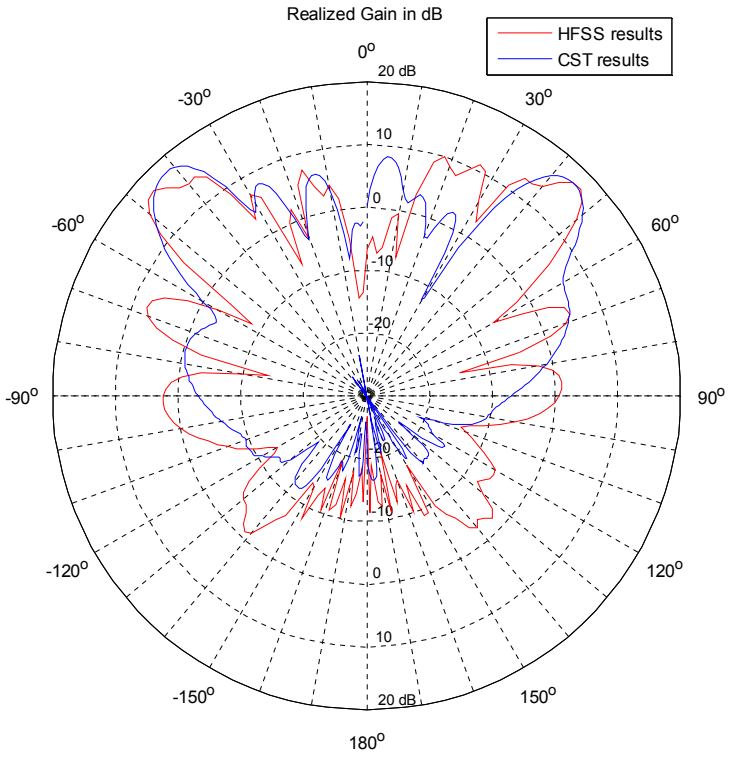

Figure 43: Realized Gain of the antenna at 73GHz.

The radiation pattern of the antenna has two main lobes in the Φ = 90° plane. The two main lobes have a directivity of 19.2dB at 73GHz and they are at angles θ = ±42° with angular width of 12.4°. Other side lobes are apparent in the radiation pattern with a side lobe level of -10.1dB. The results obtained in HFSS are very close to the ones obtained in CST. Figure 44 illustrates the 3D radiation pattern of the antenna.

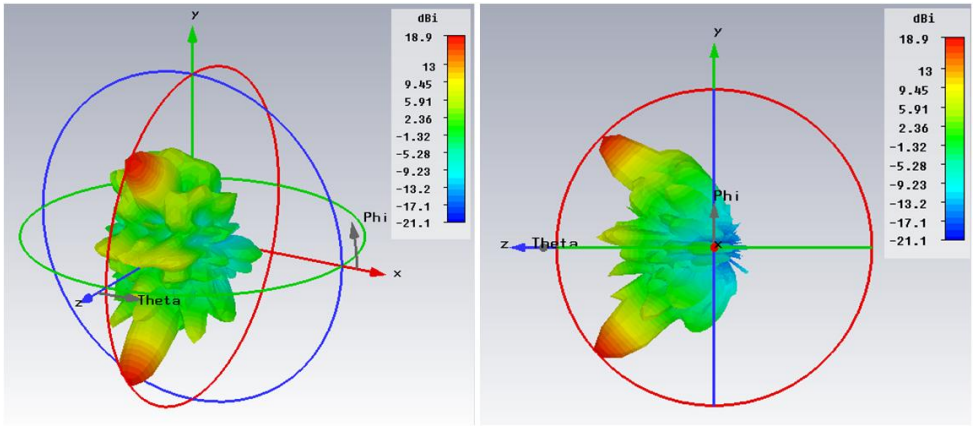

Figure 44: Radiation Pattern of the array fed by a rectangular waveguide

This design is fabricated and tested. Therefore a study of the effect of the etching of the substrate is investigated. The etching causes a decrease in the dielectric thickness only in the areas etched. In this study, the thickness of the substrate under the patches, transmission lines and the transition from waveguide to Microstrip-line is considered the same. The following etching depths of the substrate are considered: 10µm, 20µm and 30µm. The results show a shift in the resonant frequency from 72.9GHz to 73.15GHz with a 10µm depth, 73.7GHz with a 20µm depth and 73.9GHz with a 30µm depth. All of the resulting shifts are acceptable because the frequency of interest is anywhere between 71-76GHz. Figure 45 shows the variations in S11 when the substrate is etched.

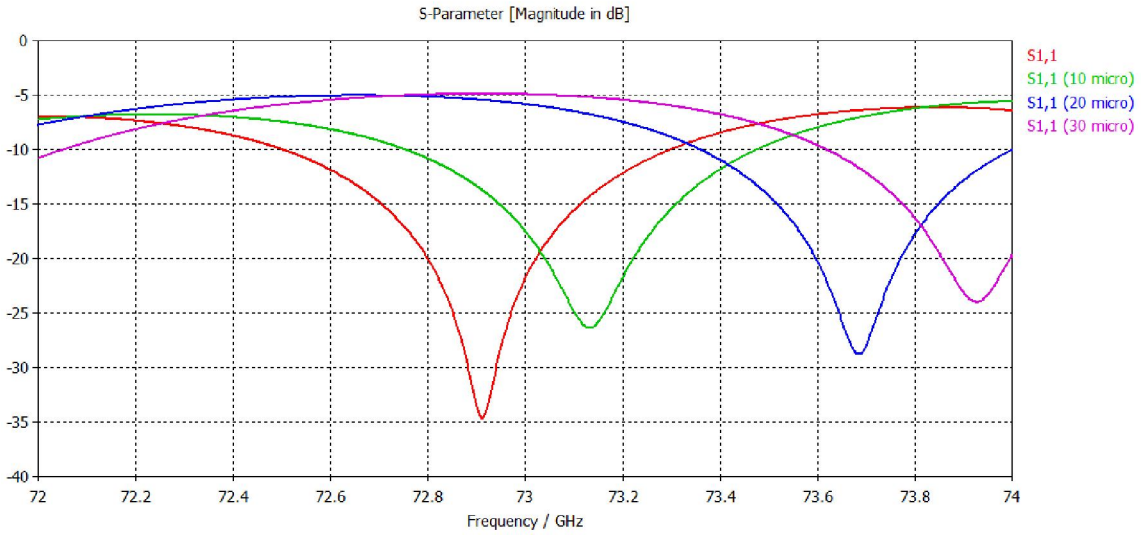

Figure 45: Variations in S11 caused by the etching of the substrate.

Comparison

By comparing the differences between the two designs, it can be realized that the feeding via RF probe resulted in an antenna with a broader bandwidth than in the case of the feeding with WR12 (The bandwidth is 4.6875 broader).

When comparing the other specifications of the two designs, we can conclude that the feeding technique did not affect the gain of the antenna, or the radiation pattern.

5.6 Summary

In this chapter the design of an 8x8 array of patch antennas is discussed. All the design guidelines are explained and two different feeding techniques are proposed. In the next chapter, the fabrication of the antenna and its testing is illustrated.

Chapter 6. Implementation of the Array of Patches

The two arrays fed via RF probe and WR12 are fabricated using the milling machine Protomat S62 from LPKF. The fabrication process for each array took 4 to 6 hours. The calibration of the heads was essential for good fabrication results because the substrate being used is very thin (0.13 mm). The milling heads used in the fabrication are: 0.1mm End Mill, 0.25 mm End Mill (these two are used to etch the layout of the array and the narrow gaps of the design) and 0.4mm End Mill (used to etch the rest of the board).

The array fed via GCPW is shown in Figure 46. The board is 2.8x2.8cm in dimensions. The array fed via WR12 is shown in Figure 47. The board dimensions are 3.2x2.8 cm.

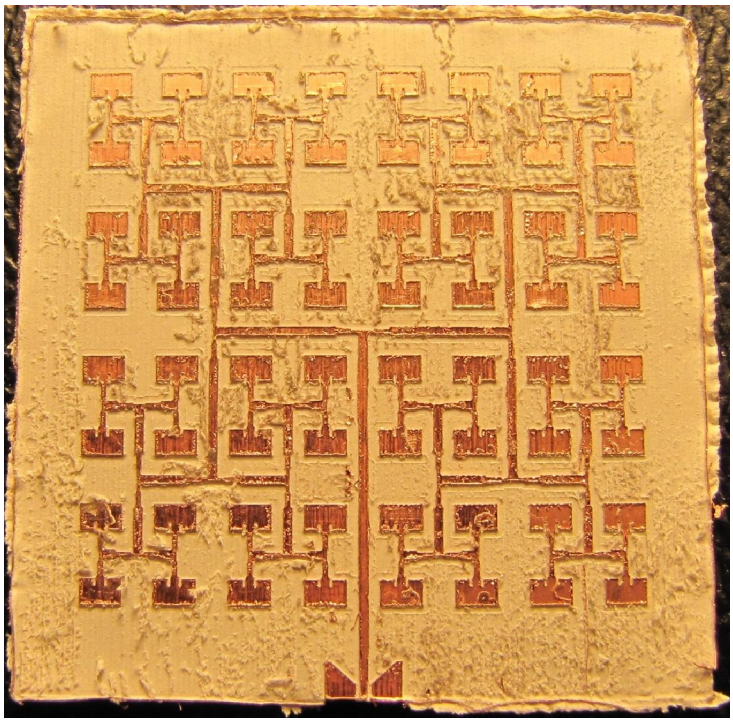

Figure 46: Fabrication of the GCPW fed array.

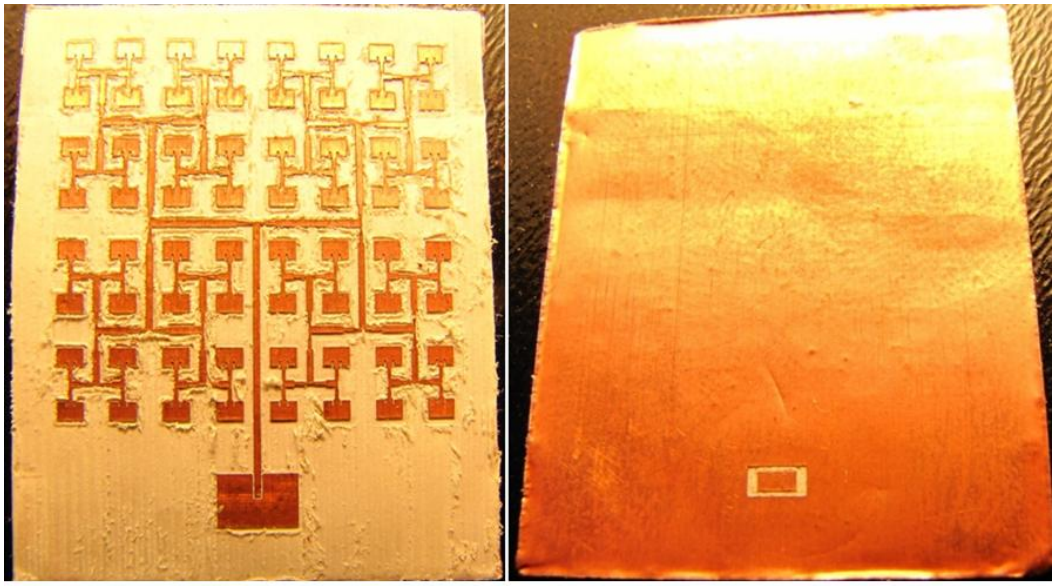

Figure 47: The top and bottom view of the WR12 fed array.

The measurement of the fabricated arrays is not done due to the lack of equipment working at E-band frequencies. For the purpose of proving that the proposed rectangular waveguide technique is working, the design of the array is scaled down to 10 GHz and 34 GHz and the S_{11} was measured.

6.1 10 GHz Array Implementation

The same design of the array of 8x8 elements at 73 GHz is scaled down to 10GHz. The element spacing is kept the same (1.25 λ_r) to keep the same radiation pattern. The number of elements is reduced because of size limitations. The patch width is W = 10.6 mm and the patch length is L = 8.7 mm. The array is fed using WR90 and the transition is modified to match the waveguide to the Microstrip-line.

The design is simulated using CST MWS. Figure 48 shows the simulated array.

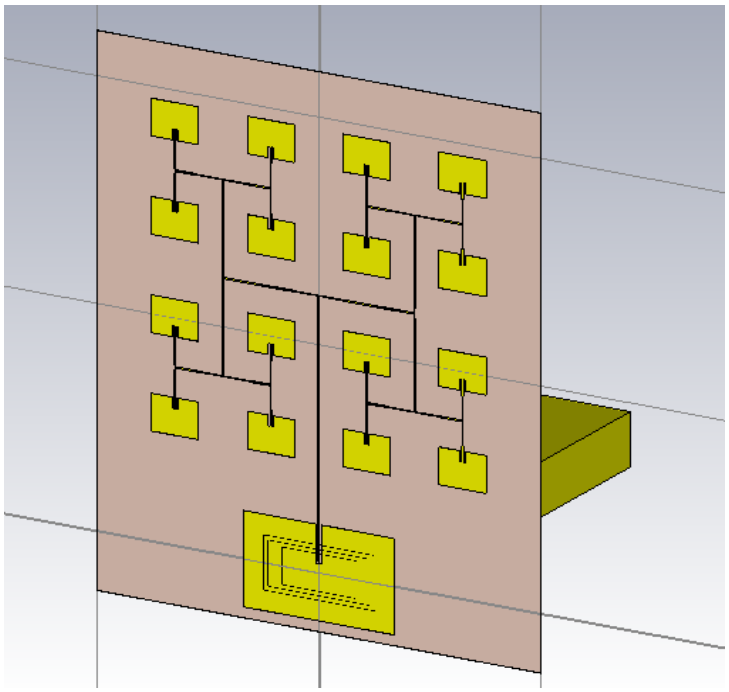

Figure 48: 10 GHz antenna array fed via WR90.

The simulated S-Parameters obtained show that the array has a center resonant frequency at 10.05 GHz and a bandwidth of 180 MHz.

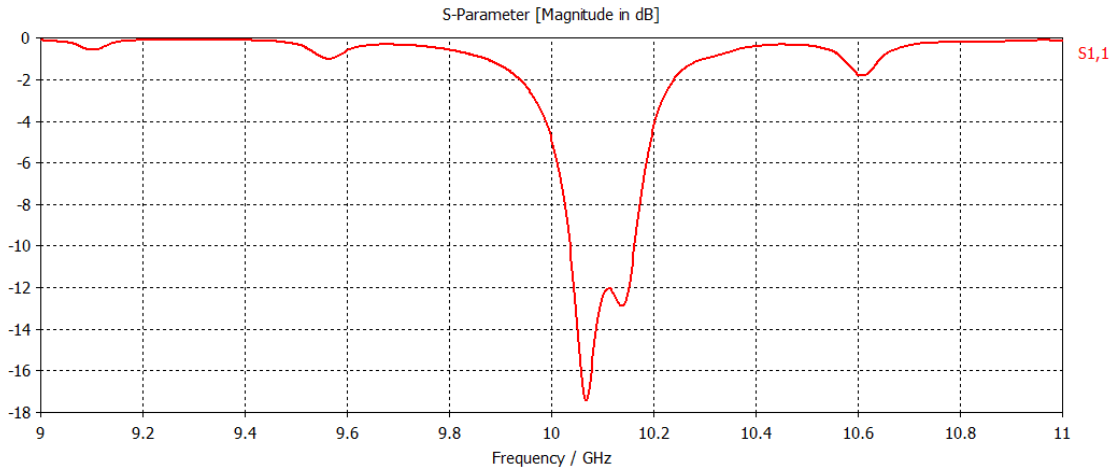

Figure 49: Simulated S11 for the 10 GHz array.

The array is fabricated and the S_{11} is measured in the Antenna Lab at UNM. The measured result show that the fabricated array has a center resonant frequency at 10.04 GHz. Figure 51 superimposes the simulated and measured S_{11} results.

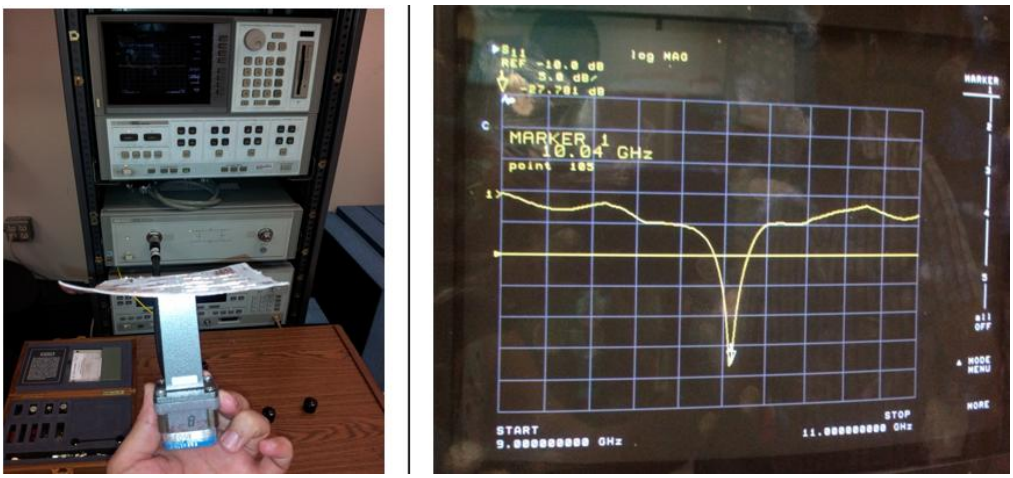

Figure 50: Fabrication and measurement of the 10GHz antenna

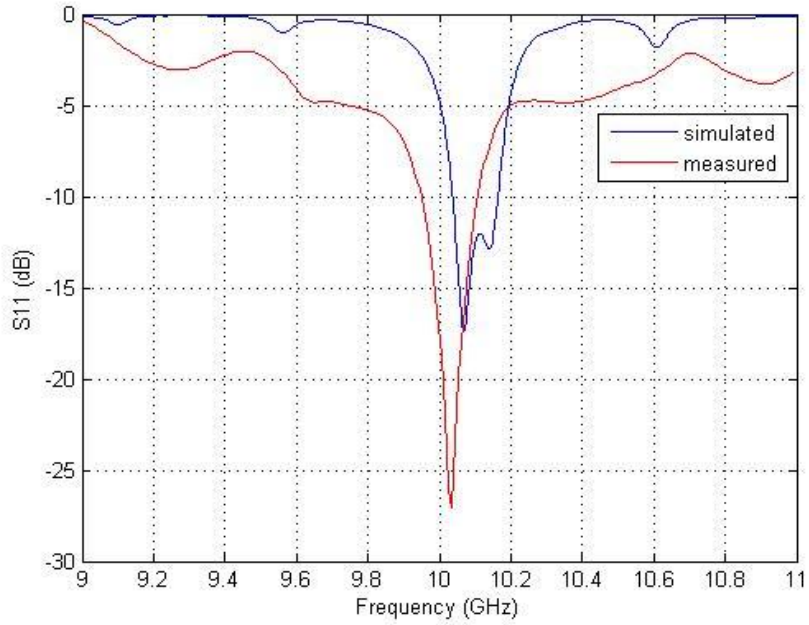

Figure 51: Simulated vs Measured S11 for the 10 GHz antenna.

The shift in the center resonant frequency is due to the etching of the substrate. The bandwidth of the fabricated antenna is 180 MHz which is similar to the simulated array. The simulated result is close to the measured result. The feeding technique is proved to be working at 10 GHz.

6.2 34 GHz Array Implementation

The same design of the array of 8x8 elements at 73 GHz is scaled down to 34 GHz. The element spacing is kept the same (1.25 λ_r) to keep the same radiation pattern. An 8x8 array is designed at 34 GHz. The rectangular patch width is W = 2.58 mm and the patch length is L = 2.38 mm. The array is fed using WR28 and the transition is modified to match the waveguide to the Microstrip-line.

The simulated antenna using CST MWS is shown in Figure 52.

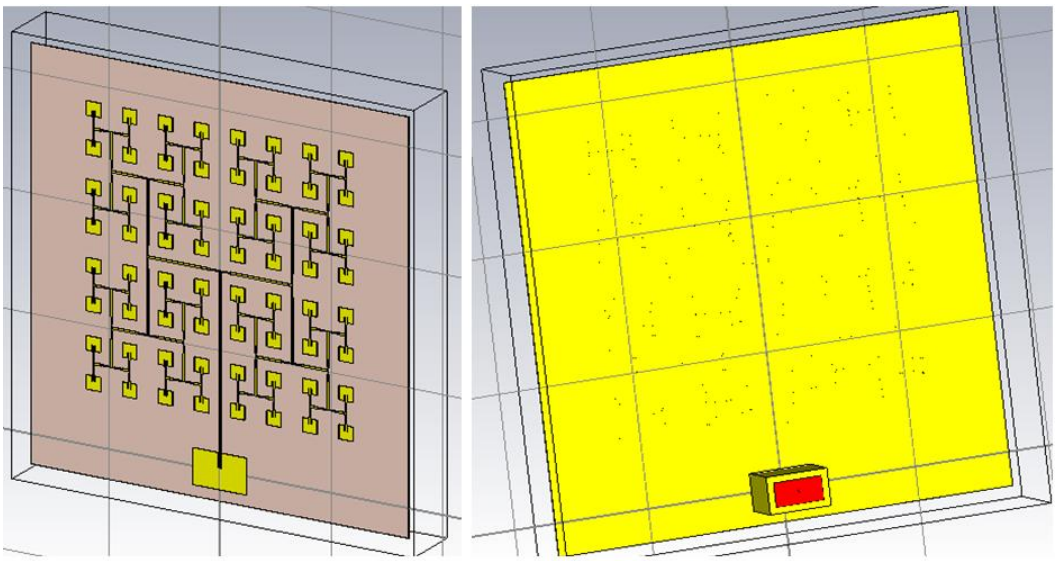

Figure 52: Top and Bottom view of the simulated antenna.

The simulated S-Parameters obtained show that the array has a center resonant frequency at 43.05 GHz and a bandwidth of 150 MHz.

The antenna is then fabricated and the S_{11} is measured as shown in Figure 53 . The measured S_{11} shows a center resonant frequency at 34.01 GHz and an antenna bandwidth of 600 MHz. A comparison between the measured and simulated S_{11} in Figure 54, illustrates a difference in the bandwidth between the two results. The measured bandwidth is wider than the simulated one. The problems in the alignment between the WR28 and the bottom layer of the array caused the bandwidth to be wider than expected by simulation. The center resonant frequencies are approximately the same in both results.

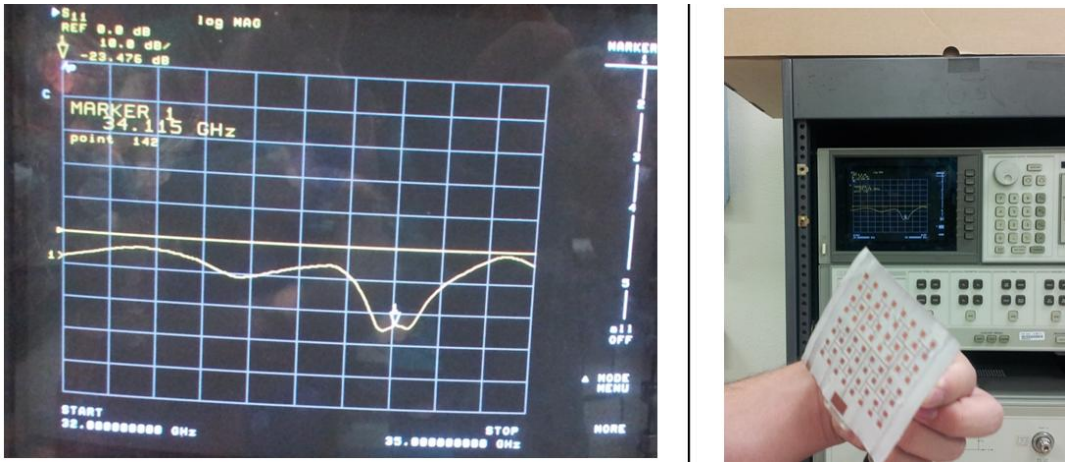

Figure 53: Fabrication and Measurement of the 34 GHz array of rectangular patches.

The results show that the feeding method is also functional at a frequency of 34 GHz or at Ka-band.

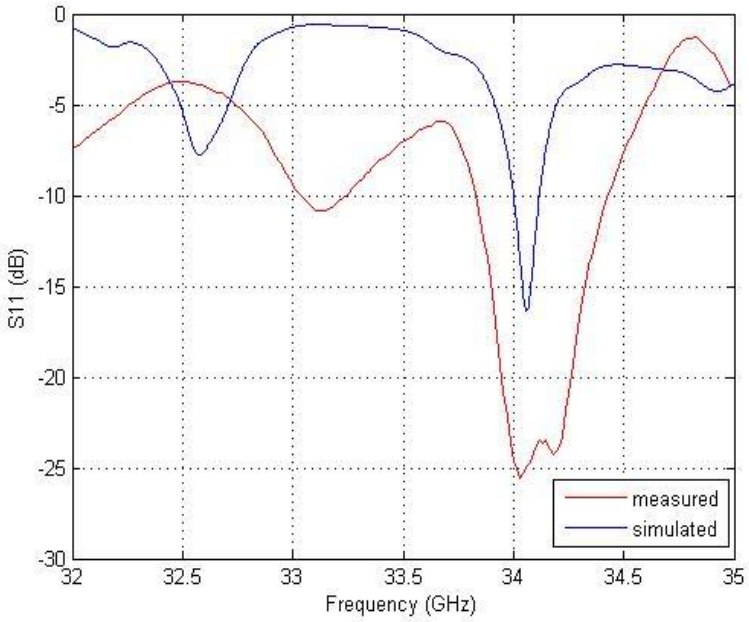

Figure 54: Simulated vs Measured S-parameters

6.3 Summary

Due to the lack of measurement equipments working at E-band, the measurement is done for two rectangular waveguide designs having exactly the same radiation pattern as the 73 GHz but lower frequencies (10 GHz and 34 GHz). The feeding technique proved functional for both frequency bands (X and Ka-band).

Chapter 7. Conclusion and Future Work

7.1 Conclusion

The design of a coherent chaotic oscillator at 100MHz following the model suggested by Corron et al. [2] using analog technologies was proved not possible. The nonlinearities in an RLC oscillator at high frequencies and the delay limitations created major obstacles in the way of achieving that. Even with the use of a more linear device than a BJT, e.g. HBT, the nonlinearities are not totally removed. The delay problem limited the upper frequency of implementing an RF coherent chaotic oscillator to 17MHz using a combination of analog and digital technologies.

The implementation of an array of patches operating at 73GHz is done. Two feeding techniques were suggested. The WR12 feeding technique proved more efficient but created a narrower bandwidth than the one the GCPW transition created. The testing of the rectangular waveguide technique was performed at 10 GHz 34 GHz due to the lack of testing equipments to carry the E-band measurements at UNM.

7.2 Future Work

For the future the following tasks will be addressed:

- The implementation of a coherent chaotic oscillator at 1MHz will be done.
- The study of the use of FPGAs in the generation of the coherent chaotic signal at 100MHz.
- The measurement of the designed and fabricated antennas at 74GHz.

- The design and implementation of novel beam steering techniques using Meta-material or phase shifter will be done.

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